



Three-Channel Multipoint Fast-Mode Plus Differential I²C-Bus Buffer with Hot-Swap Logic

PCA9616PW

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The PCA9616 is a Fast-mode Plus (Fm+) SMBus/I²C-bus buffer that extends the normal single-ended SMBus/I²C-bus through electrically noisy environments using a differential SMBus/I²C-bus (dI²C) physical layer, which is transparent to the SMBus/I²C-bus protocol layer. It consists of three single-ended to differential driver channels for the SCL (serial clock), SDA (serial data), and a third channel useful for INT or other signaling.

Remark: If the third channel is not used, the INT pin (pin 7 of the TSSOP16 package) should not be left disconnected or 'floating' (it may generate incorrect bus signals due to system noise entering this high-impedance node). Tie it to V_{SS}.

The use of differential transmission lines between identical dI²C bus buffers removes electrical noise and common-mode offsets that are present when signal lines must pass between different voltage domains, are bundled with hostile signals, or run adjacent to electrical noise sources, such as high energy power supplies and electric motors.

The SMBus/I²C-bus was conceived as a simple slow speed digital link for short runs, typically on a single PCB or between adjacent PCBs with a common ground connection. Applications that extend the bus length or run long cables require careful design to preserve noise margin and reject interference.

The dI²C-bus buffers were designed to solve these problems and are ideally suited for rugged high noise environments and/or longer cable applications, allow multiple targets, and operate at bus speeds up to 1 MHz clock rate. Cables can be extended to at least three meters (3 m), or longer cable runs at lower clock speeds. The dI²C-bus buffers are compatible with existing SMBus/I²C-bus devices and can drive Standard, Fast-mode, and Fast-mode Plus devices on the single-ended side.

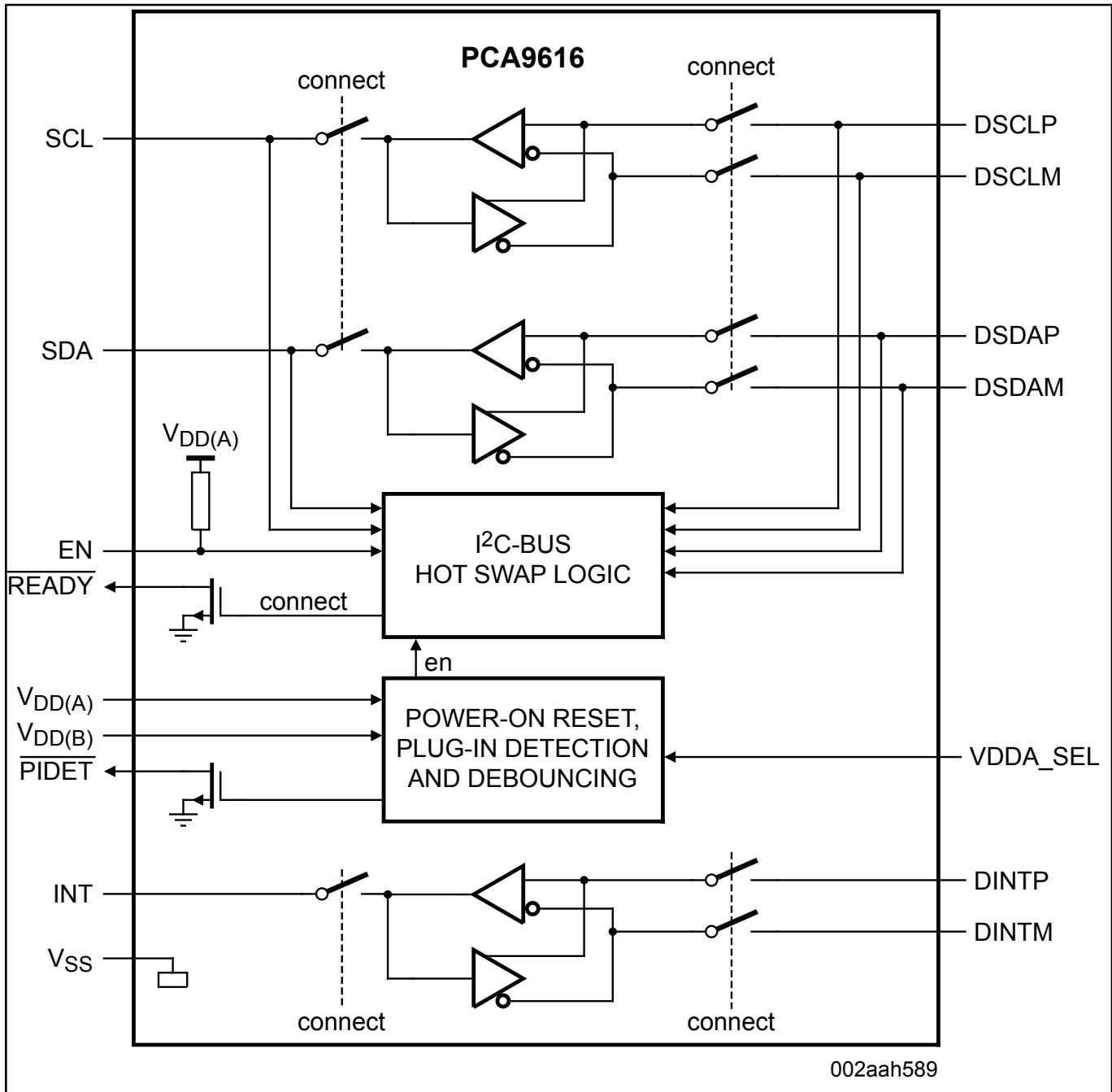
Signal direction is automatic, and requires no external control. To prevent bus latch up, the standard SMBus/I²C-bus side of the bus buffer, the PCA9616 employs static offset, care should be taken when connecting these to other SMBus/I²C-bus buffers that may not operate with static offset.

This device is a bridge between the normal 2-wire single-ended wired-OR SMBus/I²C-bus and the 4-wire dI²C-bus.

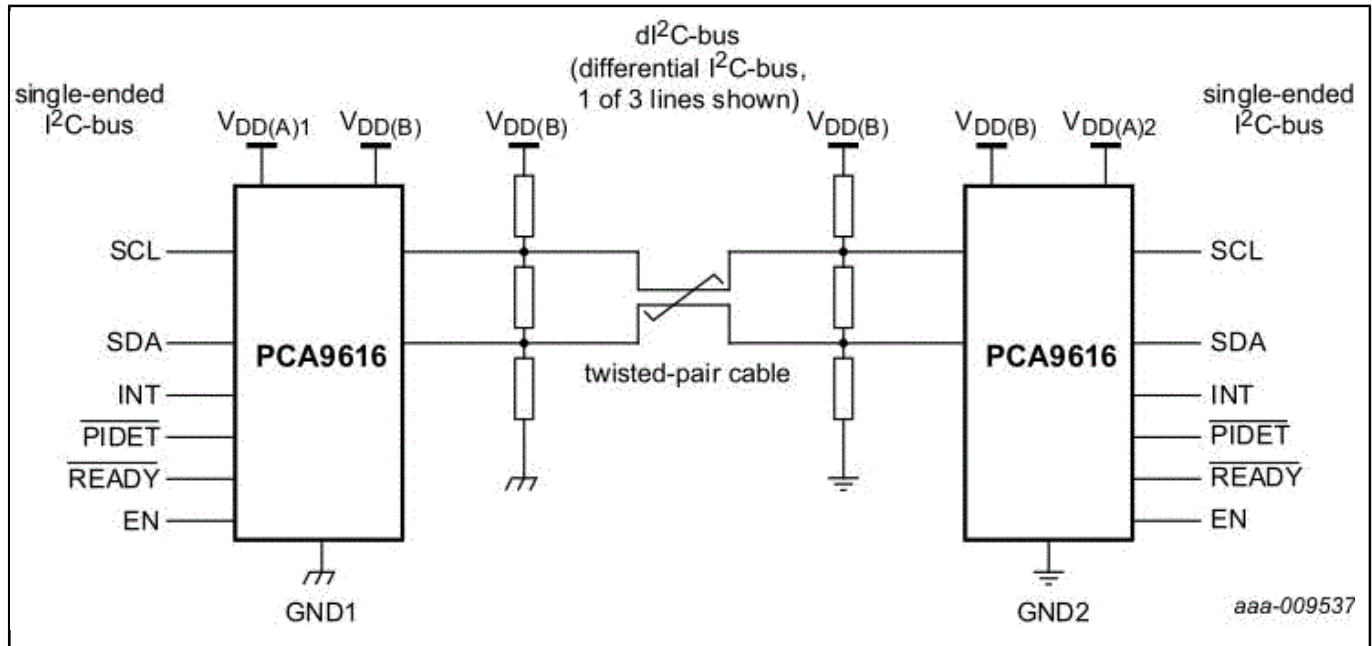
Additional circuitry allows the PCA9616 to be used for 'hot swap' applications, where systems are always on, but require insertion or removal of modules or cards without disruption to existing signals.

The PCA9616 has two supply voltages, V_{DD(A)} and V_{DD(B)}. V_{DD(A)}, the card side supply, only serves as a reference and ranges from 0.8 V to 5.5 V. V_{DD(B)}, the line side supply, serves as the majority supply for circuitry and ranges from 3.0 V to 5.5 V.

PCA9616 Block Diagram Block Diagram



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View additional information for [Three-Channel Multipoint Fast-Mode Plus Differential I²C-Bus Buffer with Hot-Swap Logic](#).

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