Parallel Bus to One-Channel Fm+ and Two-Channel UFm I²C-Bus Controller

PCU9669B

Archived

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The PCU9669 is an advanced single mode I²C-bus controller. It is a fourth generation bus controller designed for data intensive I²C-bus data transfers. It has three independent I²C-bus channels, one of them with data rates up to 1 Mbits/s using the Fast-mode Plus (Fm+) open-drain topology and two with a much larger transmit only transfer rate of up to 5 Mbits/s using the new Ultra Fast-mode (UFm) bus with push-pull topology. Each channel has a generous 4352 byte data buffer which makes the PCU9669 the ideal companion to any CPU that needs to transmit and receive large amounts of serial data with minimal interruptions.

The PCU9669 is a 8-bit parallel-bus to I²C-bus protocol converter. It can be configured to communicate with up to 64 targets in one serial sequence with no intervention from the CPU. The controller also has a sequence loop control feature that allows it to automatically retransmit a stored sequence.
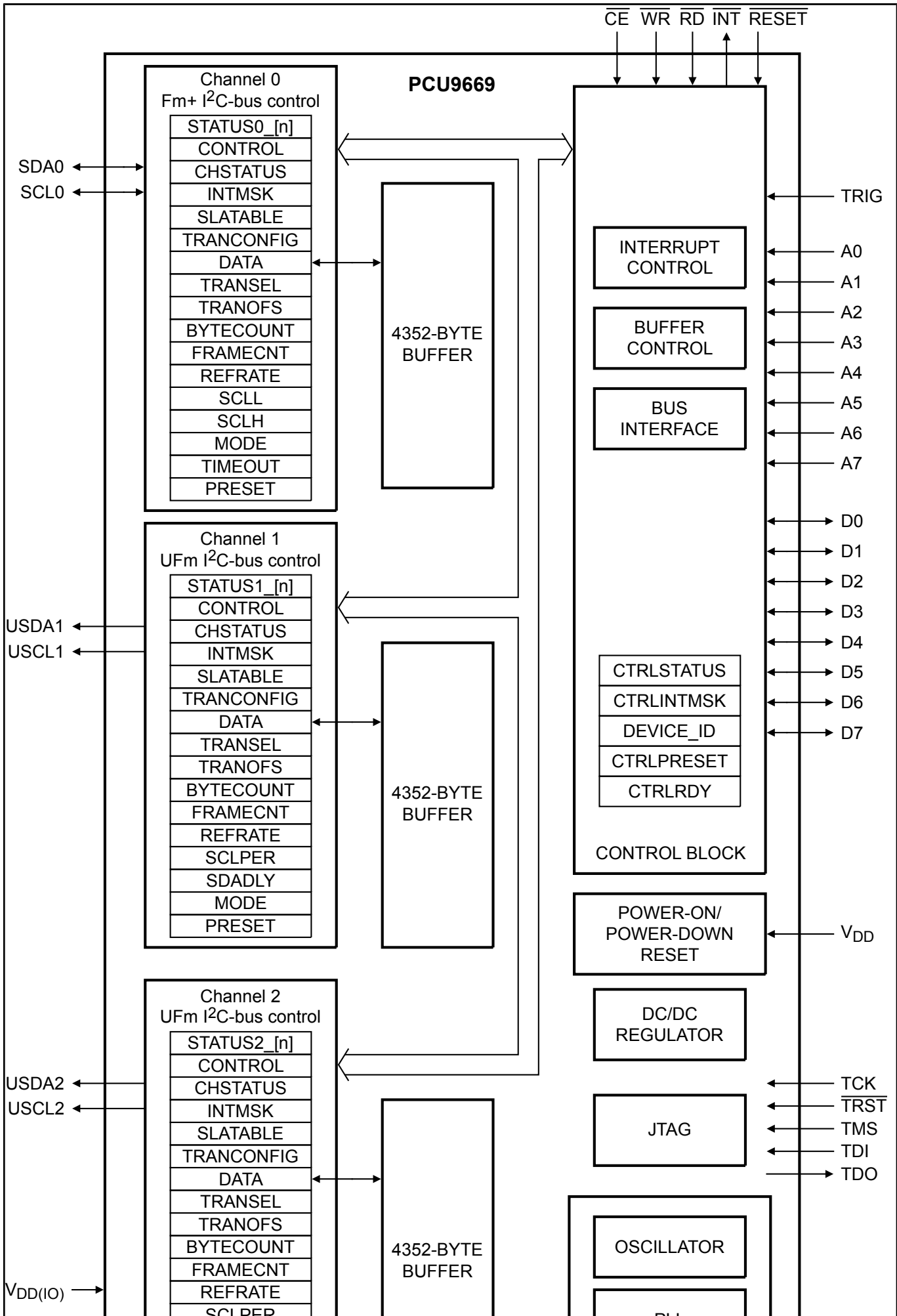
Its onboard oscillator and PLL allow the controller to generate the clocks for the I²C-bus and for the interval timer used in sequence looping. This feature greatly reduces CPU overhead when data refresh is required in fault tolerant applications.

An external trigger input allows data synchronization with external events. The trigger signal controls the rate at which a stored sequence is re-transmitted over the I²C-bus.

Error reporting is handled at the transaction level, channel level, and controller level. A simple interrupt tree and interrupt masks allow further customization of interrupt management.

The controller parallel bus interface runs at 3.3 V and the I²C-bus I/Os logic levels are referenced to a dedicated VDD(IO) input pin with a range of 3.0 V to 5.5 V.

PCU9669 Block Diagram Block Diagram

PCU9669

$\overline{CE}$ $\overline{WR}$ $\overline{RD}$ $\overline{INT}$ $\overline{RESET}$

Channel 0
Fm+ I²C-bus control

- STATUS0_[n]
- CONTROL
- CHSTATUS
- INTMSK
- SLATABLE
- TRANCONFIG
- DATA
- TRANSEL
- TRANOFS
- BYTECOUNT
- FRAMECNT
- REFRATE
- SCLL
- SCLH
- MODE
- TIMEOUT
- PRESET

SDA0
SCL0

4352-BYTE BUFFER

INTERRUPT CONTROL

BUFFER CONTROL

BUS INTERFACE

TRIG
A0
A1
A2
A3
A4
A5
A6
A7

Channel 1
UFm I²C-bus control

- STATUS1_[n]
- CONTROL
- CHSTATUS
- INTMSK
- SLATABLE
- TRANCONFIG
- DATA
- TRANSEL
- TRANOFS
- BYTECOUNT
- FRAMECNT
- REFRATE
- SCLPER
- SDADLY
- MODE
- PRESET

USDA1
USCL1

4352-BYTE BUFFER

D0
D1
D2
D3
D4
D5
D6
D7

- CTRLSTATUS
- CTRLINTMSK
- DEVICE_ID
- CTRLPRESET
- CTRLRDY

CONTROL BLOCK

POWER-ON/ POWER-DOWN RESET

V_{DD}

DC/DC REGULATOR

Channel 2
UFm I²C-bus control

- STATUS2_[n]
- CONTROL
- CHSTATUS
- INTMSK
- SLATABLE
- TRANCONFIG
- DATA
- TRANSEL
- TRANOFS
- BYTECOUNT
- FRAMECNT
- REFRATE
- SCLPER

USDA2
USCL2

4352-BYTE BUFFER

JTAG

TCK
$\overline{TRST}$
TMS
TDI
TDO

OSCILLATOR

$V_{DD(IO)}$

View additional information for Parallel Bus to One-Channel Fm+ and Two-Channel UFm I²C-Bus Controller.

Note: The information on this document is subject to change without notice.