Enhanced Performance HDMI/DVI Level Shifter

PTN3381DBS

Archived

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The PTN3381D is a high-speed level shifter device which converts four lanes of low-swing AC-coupled differential input signals to DVI v1.0 and HDMI v1.4b compliant open-drain current-steering differential output signals, up to 3 Gbit/s to support 36-bit deep color, 3D and 3 Gbit/s modes. Each of these channels provides a level-shifting differential buffer to translate from low-swing AC-coupled differential signaling on the source side, to TMDS-type DC-coupled differential current-mode signaling terminated into 50 to 3.3 V on the sink side. Additionally, the PTN3381D provides a single-ended active buffer for voltage translation of the HPD signal from 5 V on the sink side to 3.3 V on the source side and provides a channel with active buffering and level shifting of the DDC channel (consisting of a clock and a data line) between 3.3 V source-side and 5 V sink-side. The DDC channel is implemented using active I²C-bus buffer technology providing capacitive isolation, redriving and level shifting as well as disablement (isolation between source and sink) of the clock and data lines.

To provide the highest level of integration in external adapter (or: dongle) applications, PTN3381D includes an on-board 5 V DC regulator. Its output is designed to provide the required 5 V power supply to the DVI or HDMI connector, thereby eliminating the need for a separate external regulator. The on-board regulator needs only two external capacitors to operate, and its output is active whenever a valid 3.3 V is applied to the PTN3381D VDD pins.

The low-swing AC-coupled differential input signals to the PTN3381D typically come from a display source with multi-mode I/O, which supports multiple display standards, for example, DisplayPort, HDMI and DVI. While the input differential signals are configured to carry DVI or HDMI coded data, they do not comply with the electrical requirements of the DVI v1.0 or HDMI v1.3a specification. By using PTN3381D, chip set vendors are able to implement such reconfigurable I/Os on multi-mode display source devices, allowing the support of multiple display standards while keeping the number of chip set I/O pins low.

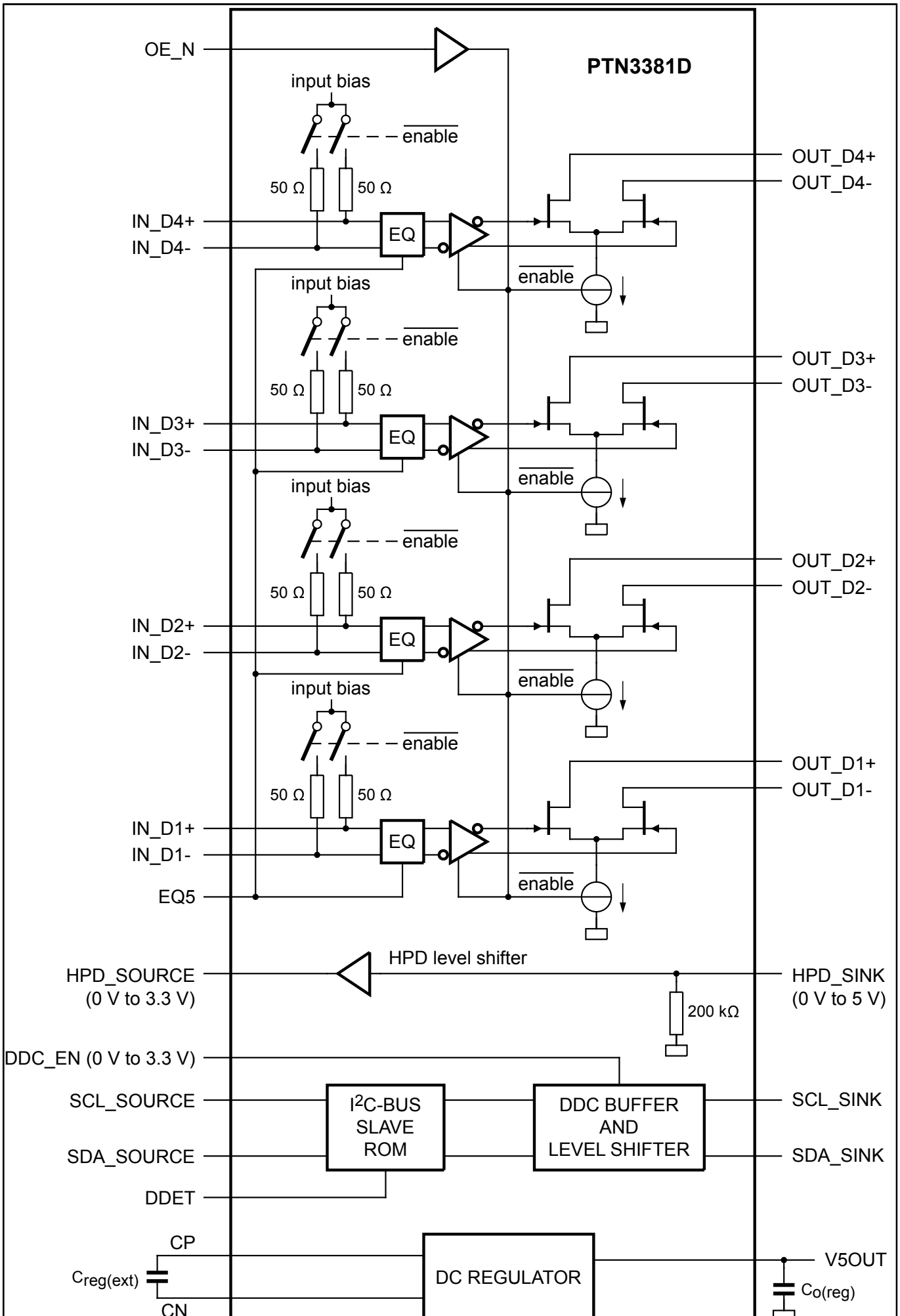
The PTN3381D main high-speed differential lanes feature low-swing self-biasing differential inputs which are compliant to the electrical specifications of DisplayPort Standard v1.2 and/or PCI Express Standard v1.1, and open-drain current-steering differential outputs compliant to DVI v1.0 and HDMI v1.4b electrical specifications.The I²C-bus channel actively buffers as well as level-translates the DDC signals for optimal capacitive isolation. Its I²C-bus control block also provides for optional software HDMI dongle detect by issuing a predetermined code sequence

upon a read command to an I²C-bus specified address. The PTN3381D also supports power-saving modes in order to minimize current consumption when no display is active or connected.

The PTN3381D is a fully featured HDMI as well as DVI level shifter. It is functionally equivalent to PTN3361D but provides an onboard 5 V regulator. The PTN3381D supersedes PTN3381B, and provides a better high speed performance with a programmable equalizer.

PTN3381D is powered from a single 3.3 V power supply consuming a small amount of power (230 mW typical with no load at 5 V regulator) and is offered in a 48-terminal HVQFN48 package.

PTN3381D Block Diagram Block Diagram


PTN3381D
OE_N
input bias
enable
50 Ω
50 Ω
IN_D4+
IN_D4-
EQ
OUT_D4+
OUT_D4-
IN_D3+
IN_D3-
OUT_D3+
OUT_D3-
IN_D2+
IN_D2-
OUT_D2+
OUT_D2-
IN_D1+
IN_D1-
OUT_D1+
OUT_D1-
EQ5
HPD level shifter
HPD_SOURCE
(0 V to 3.3 V)
HPD_SINK
(0 V to 5 V)
200 kΩ
DDC_EN (0 V to 3.3 V)
SCL_SOURCE
SDA_SOURCE
I2C-BUS
SLAVE
ROM
DDC BUFFER
AND
LEVEL SHIFTER
SCL_SINK
SDA_SINK
DDET
CP
Creg(ext)
CN
DC REGULATOR
V5OUT
Co(reg)

View additional information for Enhanced Performance HDMI/DVI Level Shifter.

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