APPLICATION NOTE

Start up behaviour of the UAA3220TS crystal oscillator

AN00085

Philips
Semiconductors

PHILIPS

Abstract

This report describes the start-up behaviour of the UAA3220TS crystal oscillator. The general physical basics of the crystal resonator as well as important characteristics of the oscillator circuit are described. Modifications of the circuit and hints are presented to improve the oscillator start-up behaviour when using crystal resonators with a larger motional resistance than specified in [1].

APPLICATION NOTE

Start up behaviour of the UAA3220TS crystal oscillator

AN00085

Author(s):
Stephan de Zeeuw

Philips Semiconductors
Systems Laboratory Hamburg
Germany

Keywords

UHF/VHF single-chip receiver
Crystal resonator
Negative impedance model

Number of pages : 23

Date: 2000-12-07

Summary

The application of the UAA3220TS crystal oscillator has been described in [2]. This oscillator is based on a Colpitts configuration employing a crystal resonator as specified in [1]. Experimental results revealed that crystals according to the above given specification are expensive. It is therefore desired to relax the given crystal specification with respect to certain parameters, e.g. the motional resistance, which in return may have impacts on the oscillator start up behaviour.

This report describes the design limits when changing the crystal specification and how to properly design the oscillator regarding oscillator start up behaviour.

An introduction is given in the first chapter describing possible problems when relaxing the crystal specification. The second section describes important physical basics of the crystal resonator. Furthermore, the negative impedance model is introduced as an equivalent electrical circuit for an oscillator circuit. Section 3 describes the active part of the UAA3220TS crystal oscillator. A simulation model is presented which is used to illustrate certain oscillator parameters. Section 4 focuses on the important oscillator start up parameter, the oscillation margin, and how to improve this parameter. General design hints are given in the last chapter.

Please note that all figures and results presented in this paper are based on linear simulations employing nominal component values only and may vary as a result of device spreads, component tolerances or temperature.

For a detailed description of the IC characteristic please refer to [1]. Detailed application support is given in [2].

Contents

1. INTRODUCTION

The integrated circuit UAA3220TS is a single–chip superheterodyne receiver. The high frequency carrier (e.g. 315, 433.92 or 868.35 MHz) is down-converted to the intermediate frequency of typical 10.7 MHz by means of the local oscillator (LO) signal.

The UAA3220TS has been designed to employ a crystal oscillator and frequency multiplication to generate the local oscillator signal. The base of this design was the crystal specification as given in the data sheet ([1]):

$R_M \leq 20$ Ohm @ (1 nW $\leq P_{crystal} \leq$ 1 mW)
$C_0 \leq$ 6 pF
$C_L =$ 6 pF
Third overtone

The crystal frequency can range from 33.8 MHz up to 95.31 MHz depending on the multiplication factors employed in the crystal oscillator output stage as well as in the multiplier tank circuit.

Experimental results revealed that crystals according to the above given specification are expensive, especially when SMD type packaging is necessary. As a result it is desired to relax this specification.

On the other side, relaxing the given crystal requirements may have impacts on the oscillator start-up. Here, the most important parameter is the oscillation margin, which describes the relation between the oscillator gain and its losses at start up of oscillation. In case, this margin is smaller than one the oscillator may not operate and inhibits the receiver function.

Using different oscillator configurations (e.g. Butler emitter follower circuit or circuits using an external oscillator transistor) or modifying the existing oscillator circuit are possible solutions.

This report describes the possible design limits when changing the crystal specification and how to properly design the oscillator regarding oscillation margin. Furthermore, measures are given to improve the given crystal oscillator circuit with respect to this parameter.

Throughout this report simulation results are used to illustrate the described parameters. Linear conditions are assumed for all simulations, which are only valid at start up of the oscillator. Hence, non-linear and steady state parameters of the oscillator respectively are not considered.

2. GENERAL

2.1 Crystal resonator basics

Figure 1 gives the simplified equivalent circuit for a crystal resonator at its operating frequency:

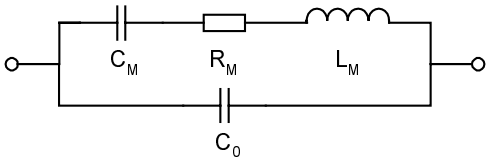

Figure 1: Crystal resonator equivalent circuit

The motional elements C_M, L_M and R_M define the main series resonance of the resonator near which the crystal is intended to operate. The capacitance C_0 describes the static capacitance being present between the terminals of the crystal. C_0 and the motional elements form an additional parallel resonant circuit. Based on this equivalent model of the resonator the following characteristic resonance frequencies can be defined assumed that R_M = 0 Ohm (see [3]):

- Series resonance frequency: $f_s = \frac{1}{2\pi\sqrt{L_M C_M}}$
- Parallel resonance frequency: $f_p = \frac{1}{2\pi\sqrt{L_M \frac{C_M C_0}{C_M + C_0}}} = f_s\sqrt{1+\frac{C_M}{C_0}}$

In the practical case of a lossy crystal, the resistance R_M shifts both resonance frequencies to slightly higher values: the "resonance frequency" $f_r \sim f_s$ and the "anti-resonance frequency" $f_a \sim f_p$.

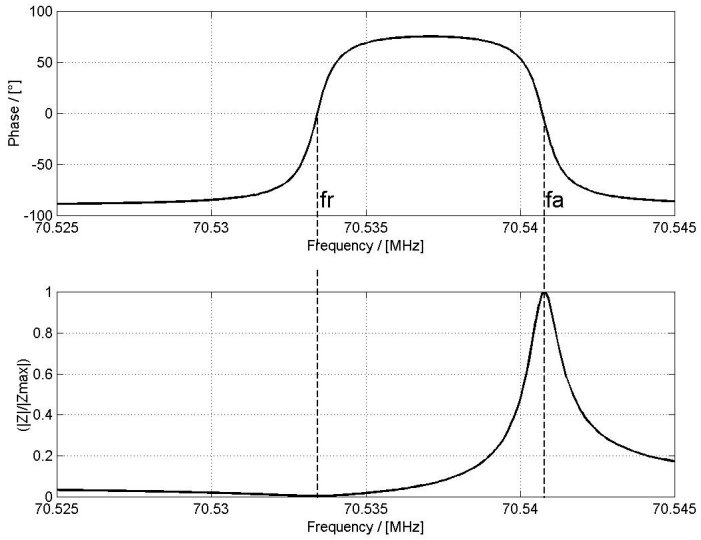

Figure 2: Typical frequency characteristic of a crystal resonator

Figure 2 depicts the typical frequency characteristic (phase and magnitude) of a crystal resonator. For frequencies below f_r and above f_a respectively, the device behaves capacitive. In the small frequency range between f_r and f_a the crystal impedance is inductive. For this reason operation of the crystal with at a well-defined frequency is only possible within this region. In addition, crystal-based oscillators are operated at and near the resonance frequency f_r respectively where the crystal offers the lowest impedance.

At the resonance frequency f_r the crystal reactance is zero and the effective resistance value is close to the value of the motional resistance R_M. To compensate for circuit and PCB capacitance variations, an external load capacitance C_L is used in certain oscillator circuits. Under this condition the crystal operates at the load resonance frequency f_L, with

$$f_L = f_s \sqrt{1 + \frac{C_M}{C_0 + C_L}},$$

being higher than the resonance frequency f_r but lower than f_a (see [3]). At f_L the crystal impedance is inductive and thus the device can be regarded as a high quality inductor L_{XTAL}. Furthermore, the motional resistance R_M is transformed to a higher effective crystal resistance, R_L, with

$$R_L = R_M \left(1 + \frac{C_0}{C_L}\right)^2$$

Ideally, the motional resistance R_M of a crystal resonator should be independent of any variation in drive level or temperature. In practice, crystals show a drive level dependency (DLD) of the motional resistance. Since oscillation starts up from noise level, the respective crystal drive level is very low and the actual value of R_M can be larger than the nominal one. DLD has been observed to be strongly dependent on ageing, temperature as well as on the crystal resonator design (e.g. package) and production respectively. Another spurious increase of the motional resistance value R_M might also be observed at certain temperature spots within the operating temperature range (temperature dips). Both effects have to be taken into account when designing the oscillator.

The load capacitance C_L is used to adjust the crystal frequency throughout the production process and is given in the resonator specification. On the other hand the actual value of C_L is determined by the external circuitry. Providing a different load capacitance to the crystal than specified results in a shifted oscillation frequency and changed effective crystal resistance also.

Small values of the static capacitance C_0 are desirable to keep the effective crystal resistance R_L as small as possible.

The equivalent circuit of a crystal operating at the load resonance frequency f_L can be given as depicted in Figure 3.

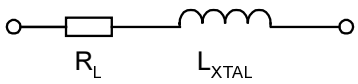

Figure 3: Equivalent circuit of a crystal operating at f_L

2.2 Negative resistance model and oscillation margin

The negative resistance model divides an oscillator circuit into two one-port elements: the passive crystal resonator and the remaining active part of the oscillator (in the following called amplifier). Point A in Figure 4 as well in successive figures characterises the division between amplifier and resonator. According to this approach, the following equivalent electrical circuit can be given:

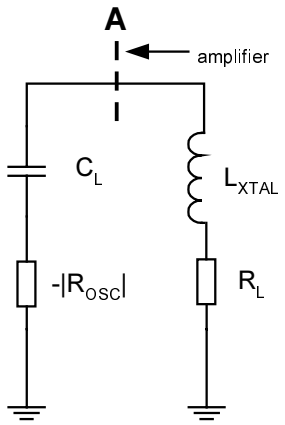

Figure 4: Negative resistance model of an oscillator

R_{OSC} is defined as the gain of the amplifier and is negative whereas C_L represents the amplifier's capacitive reactance. R_L and L_{XTAL} have been introduced in chapter 2.1 and describe the crystal resonator. Oscillation starts up from noise level when

$$-X_L = X_{XTAL}$$

$$Oscillation\,Margin = \frac{-R_{OSC}}{R_{L,\max}} \geq 1$$

$R_{L,max}$ denotes the maximum effective resistance assuming the maximum specified value for R_M and C_0. In case the second relation, the so-called oscillation margin, is smaller than 1, oscillation does not start up. For example, assuming a crystal oscillator with R_M = 30 Ohm, C_0 = 6 pF and C_L = 6 pF a gain of at least $|R_{OSC}| \geq 120$ Ohm has to be provided to achieve a margin value of 1. Furthermore, due to DLD and temperature dips effects, it is recommended to design crystal oscillators with a margin of 2…3 (see [3]).

As oscillation builds up, the amplifier operation becomes non-linear and its gain decreases until it merely compensates for losses in the oscillator circuit (unity gain):

$$\left|\tilde{R}_{OSC}\right| = R_L$$

Under steady state condition the resonance frequency might also be shifted slightly due to transistor saturation effects.

3. UAA3220TS OSCILLATOR AMPLIFIER

3.1 General description

The UAA3220TS employs a Colpitts crystal oscillator with on-chip transistors as given in Figure 5.

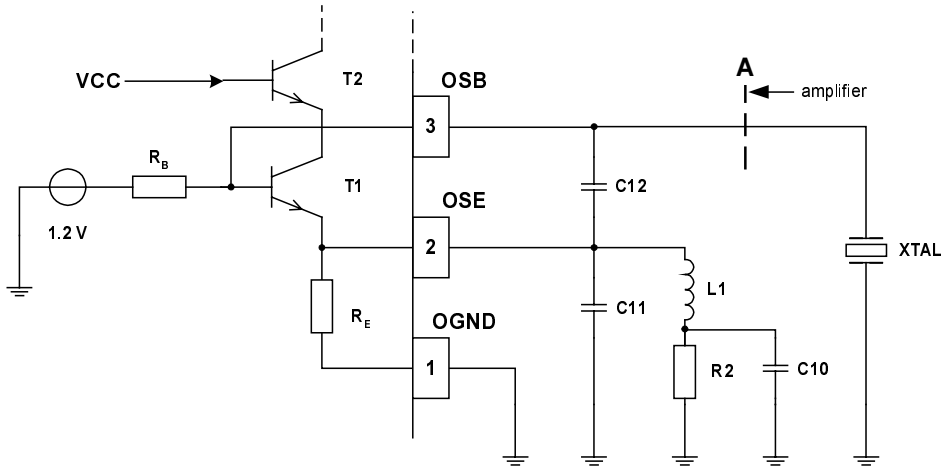

Figure 5: UAA3220TS crystal oscillator configuration

The on-chip transistor operates in common-collector configuration by means of a following cascode stage. An internal base resistor, R_B = 19.2k, and the parallel combination of an internal emitter resistor, R_E = 8.15k, and R2 set the biasing of the oscillator.

C10 compensates the inverse feedback of the emitter resistors at the oscillation frequency.

The oscillator is operated with a third overtone mode crystal. To prevent the crystal resonator oscillating at the fundamental frequency, L1 in parallel to C11 is used. L1 is chosen so that the resonance frequency of the parallel combination L1-C11 is below the desired oscillation frequency, f_{3rd}, but above the fundamental mode. Hence, the combination L1-C11 is inductive at the fundamental mode and oscillation is inhibited. At f_{3rd} L1 decreases the value of C11 to $C11_{eff}$.

$$C11_{eff} = C11 - \frac{1}{\omega_{3rd} L1}$$

As a result the following condition can be given for the emitter inductance L1:

$$\frac{1}{\omega_{3rd}{}^2 C11} < L1 < \frac{9}{\omega_{3rd}{}^2 C11}$$

C12 and $C11_{eff}$ together with parasitic IC and PCB capacitances form the load capacitance C_L being presented to the crystal resonator. The amplifier parameters, its gain R_{OSC} and capacitance C_L, can be determined at point A in Figure 5.

3.2 Linear simulation model

The following examples are based on a simulation model created with the Agilent ADS1.3 CAE tool (see Figure 6). The simulation component UAA3220_int_LO incorporates the internal circuit and parasitics of the UAA3220TS integrated circuit. Furthermore, external parasitic capacitances and inductances as measured in the actual used set-up are taken into account. L_emitter and R_emitter represent L1 and R2 (see Figure 5) respectively. The values of C11, C12, L1 and R2 have been used as variable parameters.

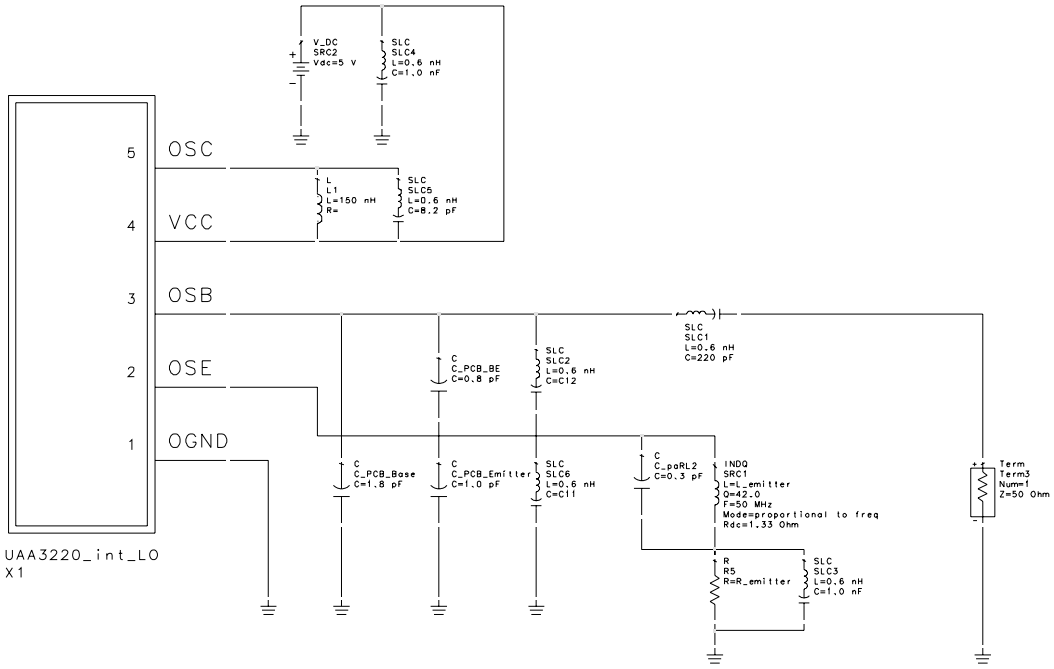

Figure 6: Simulation model of actual measured crystal oscillator

Since this report deals with the start up behaviour of the UAA3220TS, investigations have been restricted to linear small-signal simulations. 2-port S-parameter files characterising the internal UAA3220TS oscillator circuitry for defined values of the emitter resistance R2 are available on demand.

3.3 Amplifier gain and load capacitance

Figure 7 up to Figure 10 illustrate the behaviour of the UAA3220TS amplifier gain, R_{OSC}, and load capacitance, C_L, versus the capacitance values of C11 and C12. These simulation results are based on the following assumptions:

- 33,8100 MHz (f_{RX}= 315,00 MHz with m_1=3, m_2=3), L1 = 1800 nH, R2 = 1.2 kOhm
- 50,7167 MHz (f_{RX}= 315,00 MHz with m_1=2, m_2=3), L1 = 1200 nH, R2 = 1.2 kOhm
- 70.5367 MHz (f_{RX}= 433,92 MHz with m_1=2, m_2=3), L1 = 560 nH, R2 = 1.2 kOhm

L1 has been calculated according to chapter 3.1.

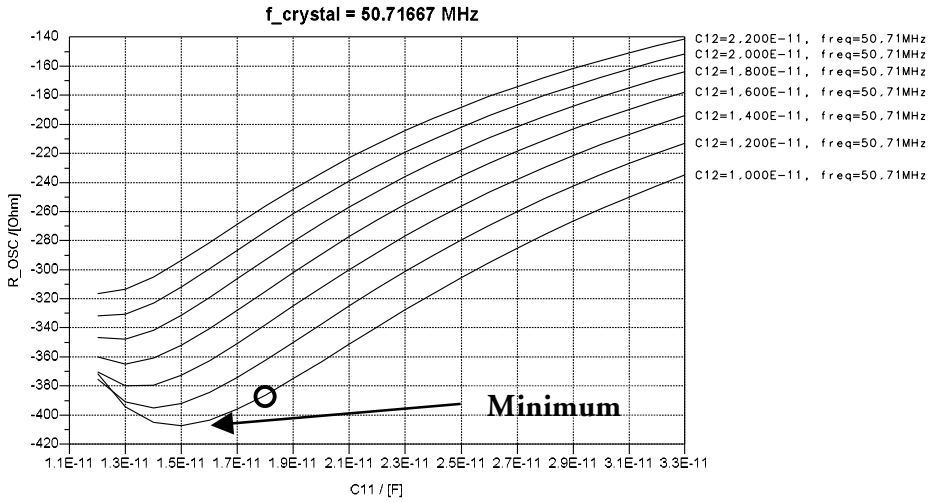

Figure 7: Simulated gain at 50.71167 MHz (L1 = 1.2 mH, R2 = 1.2 kOhm)

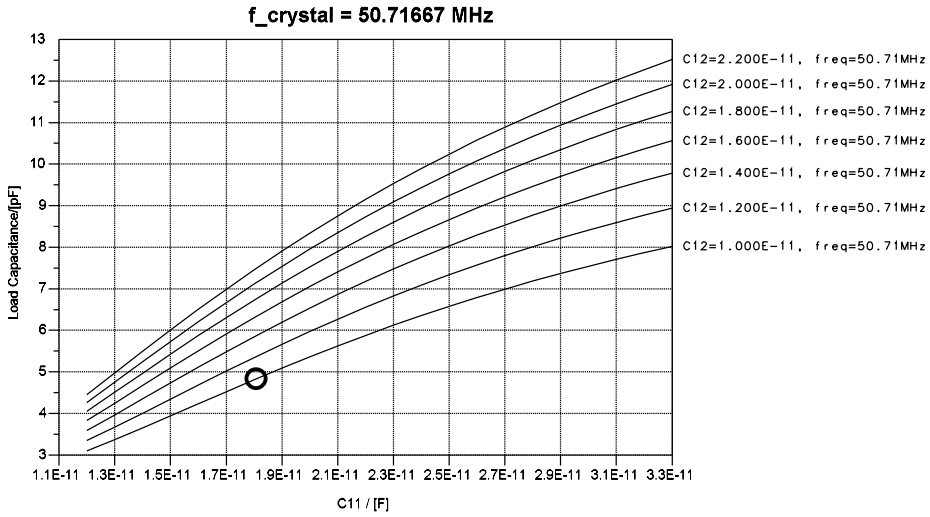

Figure 8: Simulated load capacitance at 50.71167 MHz (L1 = 1.2 mH, R2 = 1.2 kOhm)

For a given value of the emitter resistor R2 and operating frequency the amplifier gain reaches a minimum at a certain combination of C11 and C12. On the other hand, using this combination the load capacitance C_L has only a low value. The example in Figure 7 shows a gain of about –380 Ohm for C11 = 18 pF and C12 =10 pF, offering an overall load capacitance C_L of about 4.8 pF. This example will be used in the following chapters also.

Furthermore, Figure 7, Figure 9 and Figure 10 show that the amplifier gain strongly depends on the employed oscillation frequency. Regarding crystal oscillator behaviour it is thus recommendable to use low crystal frequencies and multiplication factors $m_1 = m_2 = 3$.

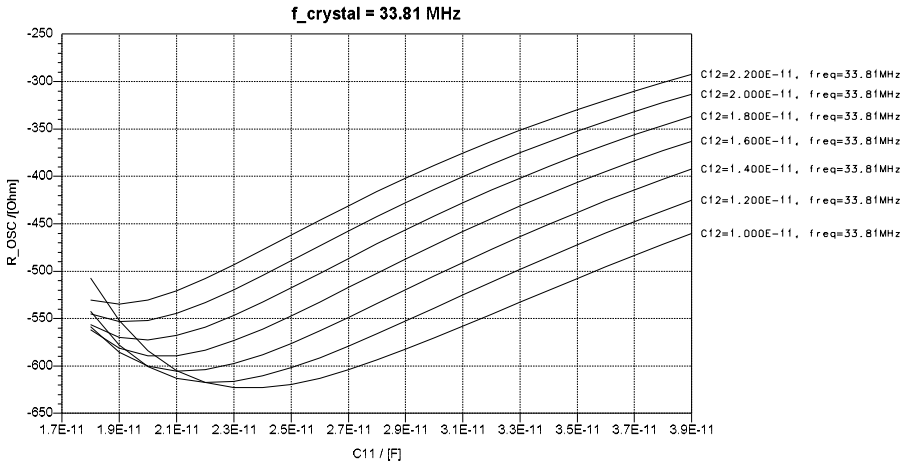

Figure 9: Simulated gain at 33.81 MHz (L1 = 1.8 mH, R2 = 1.2 kOhm)

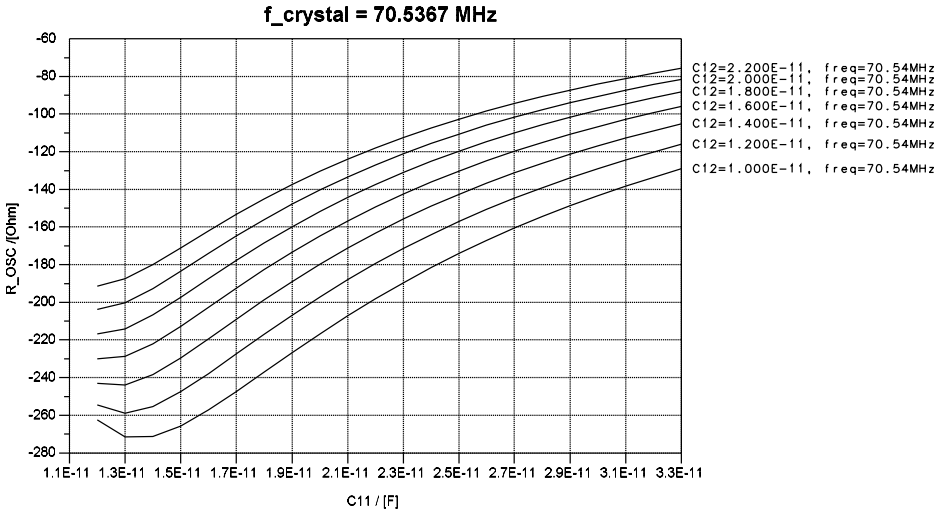

Figure 10: Simulated gain at 70.5367 MHz (L1 = 560 nH, R2 = 1.2 kOhm)

The value of R2 determines the collector current flowing through the oscillator transistor. The higher the collector current the higher the transit frequency and the current gain of the transistor respectively (up to a certain limit). As a result the amplifier gain increases but the load capacitance decreases.

Figure 11 and Figure 12 illustrate this behaviour at a crystal frequency of 50.7167 MHz with L1 = 1.2 mH and C12 = 10 pF. For example, choosing C11 = 18 pF and changing the emitter resistance from 1.2 kOhm down to 680 Ohm the amplifier gain can be improved from –380 Ohm to –455 Ohms. The load capacitance value simultaneously decreases from about 4.8 pF down to 3.8 pF.

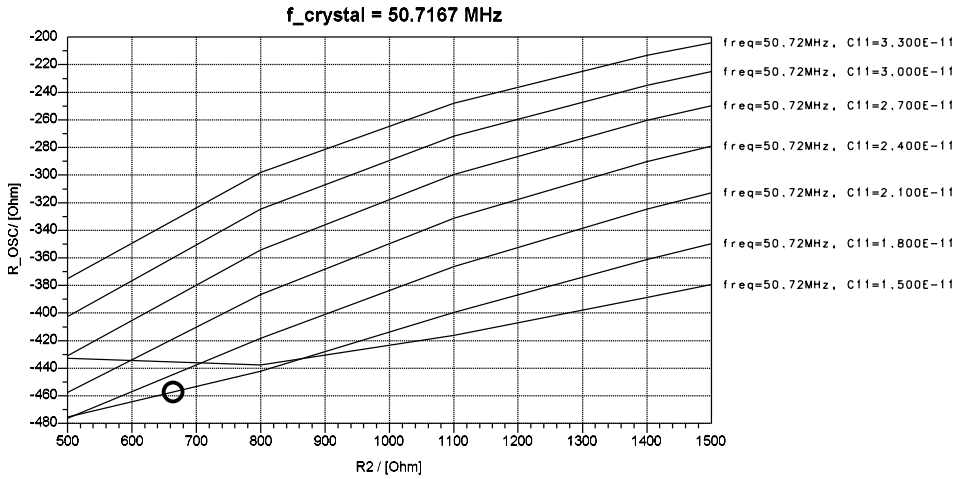

Figure 11: Simulated gain at 50.71167 MHz (L1 = 1.2 mH, C12 = 10 pF)

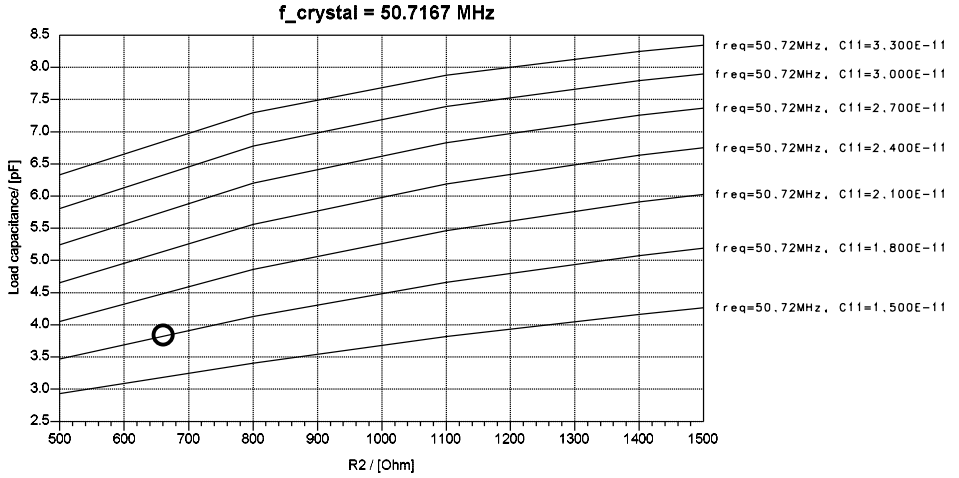

Figure 12: Simulated load capacitance at 50.71167 MHz (L1 = 1.2 mH, C12 = 10 pF)

Please note that the amplifier gain does not necessarily increase for all combinations of R2, C11 and C12. Depending on the actual component values and biasing condition of the oscillator, the transistor impedance matching conditions may not be ideally fulfilled anymore and the amplifier gain may decrease.

3.4 Measurement of amplifier parameters

The amplifier gain and load capacitance depend on various parameters: the values of the external components as given in Figure 5 (C11, C12, L1, R2 and C10), the actual PCB layout and its parasitic impedances. For this reason, the given simulation examples can not be used for the oscillator design generally. To optimise the crystal oscillator start-up behaviour the actual amplifier configuration has to be measured.

During this measurement an impedance/network analyser (e.g. HP4195A) replaces the crystal in the actual circuit (see Figure 13). The measurement instrument and the amplifier circuit have to be de-coupled with a capacitor offering low impedance at the measuring frequency. In order to measure the amplifier and the internal transistor within its linear operating range it is very important to apply only small drive to the amplifier (less than –10 dBm).

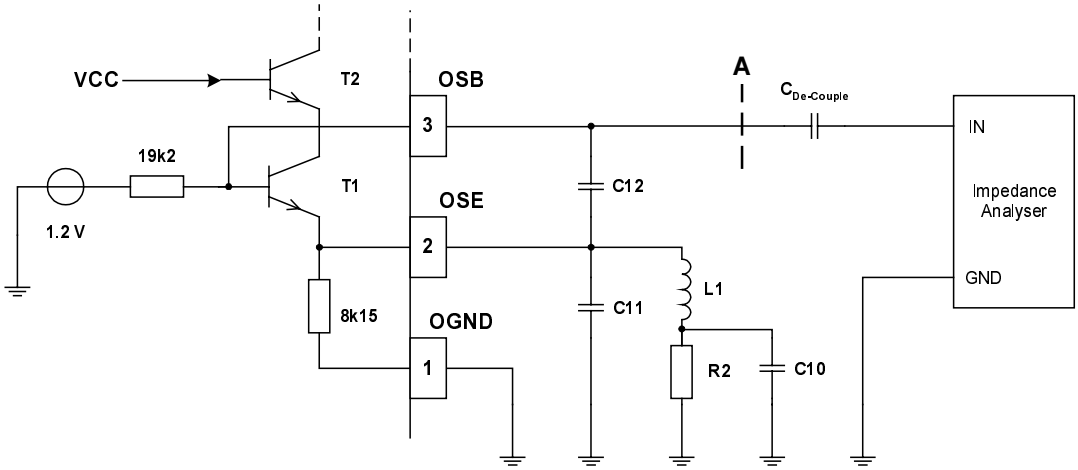

Figure 13: Amplifier measurement setup

Meaningful measurements with respect to the negative impedance model should be made at point A.

4. OSCILLATION MARGIN

4.1 Standard UAA3220TS crystal oscillator

The oscillation margin has been introduced in chapter 2.2 and can be given as follows:

$$Oscillation\ Margin = \frac{-R_{OSC}}{R_{L,\max}} = \frac{-R_{OSC}}{R_{M,\max}\left(1+\frac{C_0}{C_L}\right)^2}$$

This relationship has to be larger than one. In order to take care of DLD and temperature dip effects respectively an oscillation margin of 2 up to 3 should be chosen (see [3]).

For a given crystal resonator, with $R_{M,max}$ and C_0, the oscillation margin can only be improved when the load capacitance and the amplifier gain are chosen as large as possible. The examples as given in Figure 7 and Figure 8 show that these goals cannot be achieved simultaneously: the amplifier reaches its maximum gain only at low load capacitances values and vice versa.

Figure 14 depicts the simulated oscillation margin for a UAA3220TS crystal oscillator employing an emitter resistor R2 = 1.2 kOhm and an emitter inductance L1 = 1.2 mH. The crystal assumed has a maximum motional resistance $R_{M,max}$ = 30 Ohm and a static capacitance of C_0 = 6 pF.

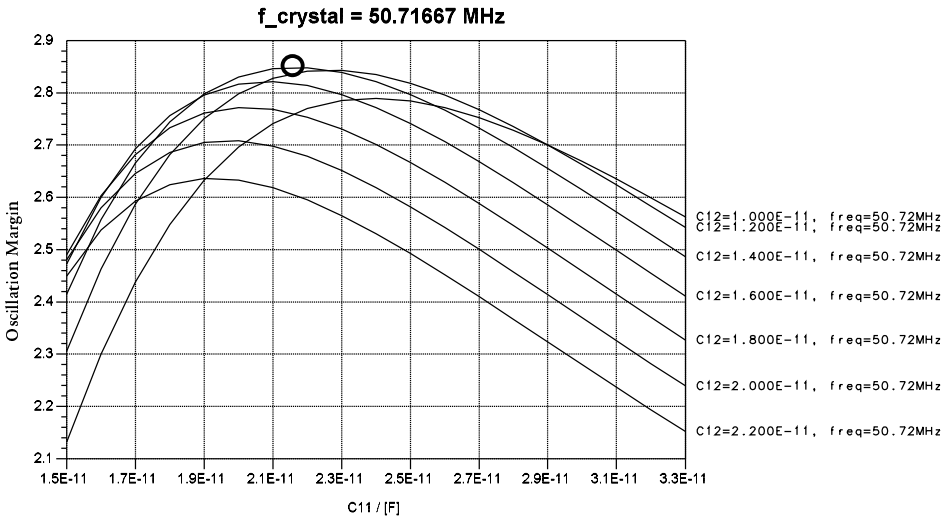

Figure 14: Simulated oscillation margin at 50.71167 MHz (L1 = 1.2 mH, R2 = 1.2 kOhm, C_0 = 6 pF, $R_{M,max}$ = 30 Ohm)

The optimum oscillation margin is reached for C11= 22 pF and C12 = 14 pF. This result is in contrast to the maximum amplifier gain achieved for C11 = 18 pF and C12 = 10 pF as shown in Figure 7. This is due to the fact that the load capacitance C_L has a quadratic influence on the oscillation margin compared to the linear one of the amplifier gain R_{OSC}.

Changing the values of R2, L1, $R_{M,max}$ and C_0 result in a different combination of C11 and C12 for the optimum oscillation margin. The same example as depicted in Figure 14 is used in Figure 15 but with a changed emitter resistor value R2 = 680 Ohm. A maximum oscillation margin of about 3.3 is reached for C11= 25 pF and C12 = 18 pF.

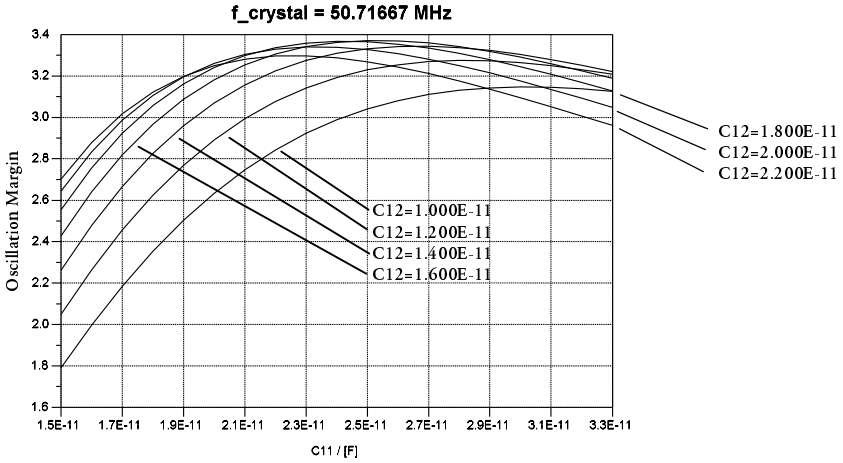

Figure 15: : Simulated oscillation margin at 50.71167 MHz (L1 = 1.2 mH, R2 = 680 Ohm, C_0 = 6 pF, $R_{M,max}$ = 30 Ohm)

Since the oscillation margin depends on several factors (C11, C12, R2, L1, C10, IC and PCB parasitics, etc.), its value has to be determined for each individual design.

The following table gives the simulated maximum motional resistance $R_{M,max}$ for different crystal frequencies and emitter resistors R2 in order to reach a nominal oscillation margin of 2. Please note that the value of the static capacitance C_0 has been set to 6 pF; lower values increase the oscillation margin accordingly. Furthermore, component tolerances and temperature effects respectively have not been taken into account. For this reason, the given values shall only be used as rough guideline at the beginning of the oscillator design.

Crystal frequency [MHz] / L1 [nH]	$R_{M,max}$	
	R2 = 680 Ohm	R2 = 1200 Ohm
33,9100 / 1800	50	50
50,7167 / 1200	45	40
70,5367 / 560	30	25
95,2944 / 330	20	-

Table 1: Simulated possible maximum $R_{M,max}$ for an oscillation margin of 2 (C_0=6pF)

4.2 Cancellation of the static capacitance C_0

Chapter 4.1 has shown that the oscillation margin for the standard UAA3220TS crystal oscillator is limited. Besides improving the actual used crystal specification and/or increasing the oscillator current the following circuit can be used to improve the oscillation margin:

The oscillation margin strongly depends on the value of the static capacitance C_0 (see chapter 4.1). Employing the extended circuit as given in Figure 16 partly compensates its influence.

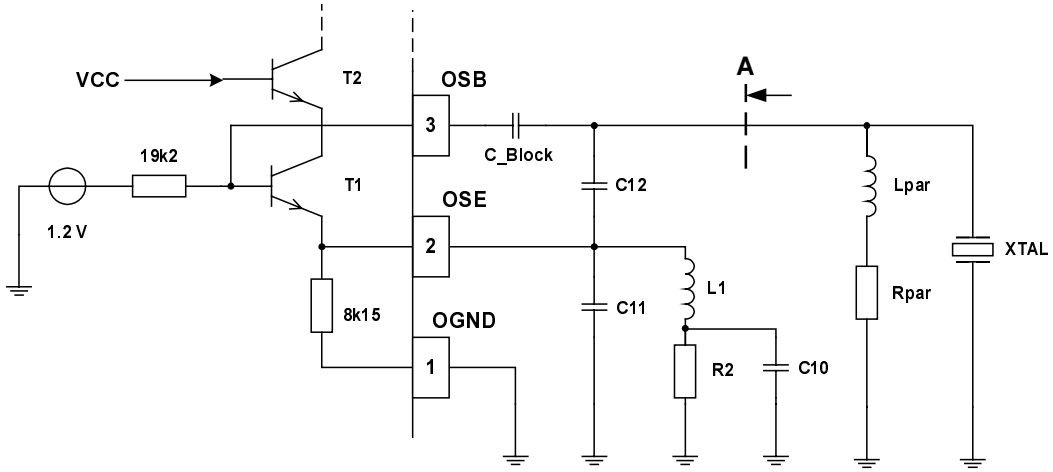

Figure 16: Cancellation of the static capacitance C_0

The inductance Lpar is chosen to resonate with the static capacitance C_0 at the crystal frequency, f_{3rd}, and hence can be calculated to

$$Lpar = \frac{1}{\omega_{3rd}{}^2 C_0}$$

In practice, standard component featuring tolerances are employed and the resonance frequency of the parallel combination C_0 - Lpar differs from the crystal resonance frequency. Nevertheless, the static capacitance C_0 is compensated partly and the transformed crystal resistance, R_L, is reduced.

Since most crystal specifications give the maximum value of the static capacitance C_0 it is recommendable to ascertain its typical value for calculation of Lpar. Furthermore Lpar should be chosen as close to the calculated value as possible and have only small tolerances (recommended 2 %).

The drawback of inserting Lpar is the introduction of a spurious resonant mode. The parallel combination of the inductance Lpar and the crystal behaves inductive below its resonance frequency. Together with C_L this inductance forms a series resonance circuit having a high quality factor. The additional resistor Rpar in series to Lpar reduces the quality factor of this combination and shall suppress the unwanted resonance mode. Since the series combination of Lpar and Rpar provide a DC path to pin 3 /OSB, C_Block is used to maintain the internal biasing of the oscillator transistor.

Since several resonance circuits configurations exist within the oscillator circuit and the amplifier gain and load capacitance strongly depend on the employed component values, it is recommended to use CAE tools for proper determination of the value for Rpar. Simulation can be done as follows:

The amplifier and resonator are divided at point A in Figure 16 and their respective impedances, $Z_{amplifier}$ and $Z_{resonator}$, are simulated separately over a frequency range from DC up to about twice the crystal frequency. Calculation of the following expression allows to proof whether the spurious resonance mode is suppressed sufficiently:

$$Z_{oscillator} = real(Z_{resonator}) + real(Z_{amplifier}) + j * \left[imag(Z_{amplifier}) + imag(Z_{resonator}) \right]$$

$Z_{oscillator}$ is normalised by real ($Z_{resonator}$) to $z_{oscillator}$:

$$z_{oscillator} = \frac{Z_{oscillator}}{real(Z_{resonator})}$$

The real part of $z_{oscillator}$ can be written as

$$real(z_{oscillator}) = 1 - Oscillation\ Margin$$

and the imaginary part expresses the normalised reactance of the overall oscillator circuit. Hence, oscillation starts up when

$$real(z_{oscillator}) \leq 0 \quad \text{and} \quad imag(z_{oscillator}) = 0$$

When $z_{oscillator}$ is plotted in a polar form diagram oscillation points can easily be found: The requirement for the reactance to be zero indicates that those points have to lie on the horizontal co-ordinate. The real part requirement further limits the oscillation possibilities; the points must lie on the left half of the horizontal co-ordinate.

Rpar has to be chosen so that the oscillation condition is only fulfilled at the crystal resonance frequency.

Assuming a standard crystal oscillator circuit operating at about 70.5367 MHz with $R_{M,max}$ = 30 Ohm, C_0 = 4.8 pF, C11 = 20 pF, C12 = 10 pF, R2= 1.2 kOhm and L1 = 560 nH a nominal oscillation margin of about 2.2 can be reached. Employing an inductance of Lpar= 1 µH in series with a resistor of Rpar = 68 Ohm to compensate the static capacitance the oscillation margin is improved to about 3.0 and the spurious resonance mode is suppressed sufficiently (see Figure 17). Please note that this example does not take any component tolerances or temperature effects into account.

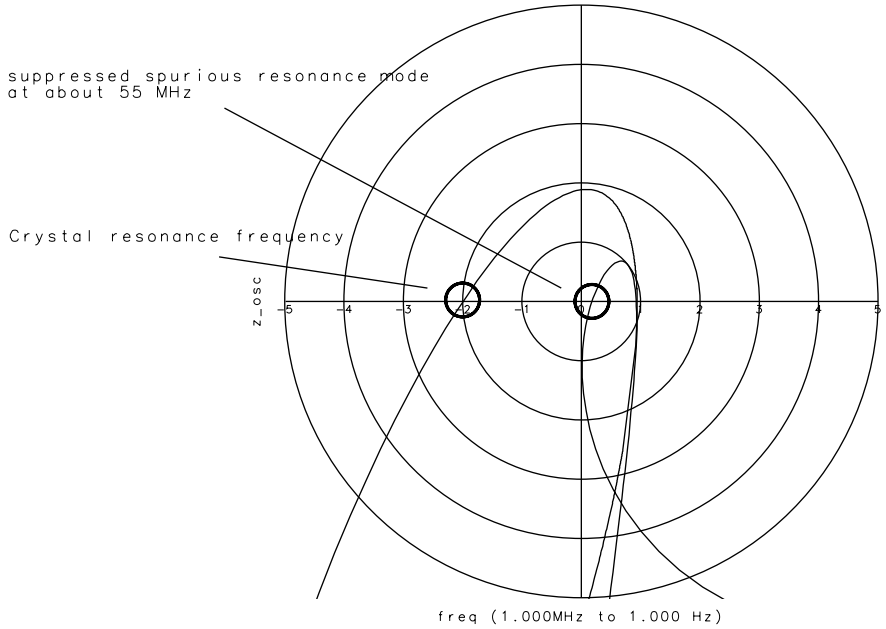

Figure 17: Polar plot for example crystal with Lpar = 1 µH, Rpar = 68 Ohm

Although Rpar adds damping to the oscillator circuit the oscillation margin can generally be improved by about 0.6 to 0.8. Note that due to the insertion of Lpar and Rpar the oscillation frequency is slightly shifted.

5. DESIGN HINTS

In the following hints are given to find the optimum possible oscillation margin throughout the design of the UAA3220TS crystal oscillator. As recommended in [3] the oscillation margin should be in the range from 2 to 3! In case a smaller minimum margin is defined for the actual oscillator design, it is recommendable to specify the crystal drive level dependency also. Furthermore, oscillation margin component tolerances and temperature effects have to taken into account.

1. Table 1 gives a rough indication for a first crystal specification with respect to crystal frequency and maximum motional resistance. The motional resistance has to be specified at a drive level of at most 50 µW to 100 µW (see also Appendix A). Please keep in mind that the static capacitance has a strong influence on the oscillation margin and that the actual circuit determines the load capacitance.
2. Chose the value of the emitter resistance R2 according to the maximum allowed receiver current. The oscillator transistor current should not be larger than 1 mA and its quiescent value can be estimated as follows:

$$ICC_0 \approx \frac{0.38\,V}{\left(R_E \,\|R2\right)} \quad \Rightarrow \quad R2 > 400\,\Omega$$

   Please note that due to non-linear effects the final transistor DC-current is slightly higher.
3. Chose the value of the emitter inductance L1 according to the actual crystal frequency (e.g. see chapter 3.3).
4. Measure the amplifier gain and load capacitance as described in chapter 3.4 for different combinations of C11 and C12.
5. Calculate the oscillation margin (see chapter 4.1) with respect to the actual chosen crystal specification (typical and maximum value of C_0, $R_{M,max}$).

In case the calculated oscillation margin is not sufficient, the crystal specification has to be adapted and step 5 to be repeated. Furthermore, the extended circuit as given in chapter 4.2 (cancellation of the static capacitance) can be used to improve the oscillation margin. Note that simulation tools should be used additionally to avoid spurious oscillation.

Generally, tight tolerated components (smaller than +/- 5%) should be used to keep the influence of component tolerances as small as possible. Especially, all inductive components should have tolerances of about +/- 2%. Design guides regarding the PCB layout can be found in [2]. Please note that the PCB layout should avoid any additional parallel capacitance to the crystal resonator which would add to its static capacitance C_0.

Although this report only describes the start-up behaviour of the crystal oscillator it has to be kept in mind that enough drive level is provided to the input of the multiplier (see [2]).

6. REFERENCES

[1] Data Sheet UAA3220TS, Frequency Shift Keying (FSK)/Amplitude Shift Keying (ASK) receiver; 1998 Nov 26

[2] Application Note: UAA3220TS, AN98104; 1998 November 18

[3] Das große Quarzkochbuch; Bernd Neubig & Wolfgang Briese; Feldkirchen: Franzis-Verlag, 1997; ISBN 3-7723-5853-5,
see also the internet link: www.telequartz.de

APPENDIX A: DETERMINATION OF THE OSCILLATOR DRIVE LEVEL

In order to determine the actual drive level applied to crystal resonator the magnitude of the crystal voltage at the operating frequency, $V_{crystal}$, (at point A in e.g. Figure 5) has to be measured.

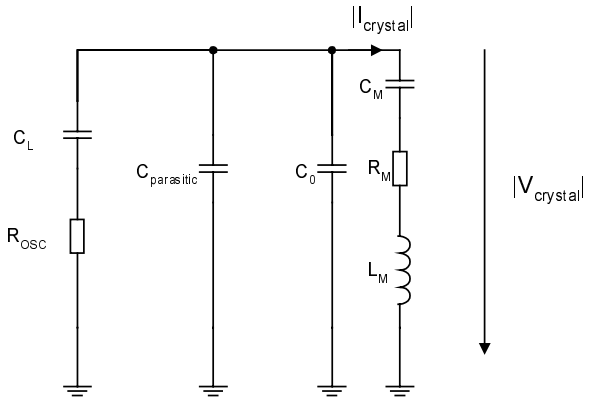

Figure 18: Measurement of crystal drive level

The magnitude of the current through the crystal, $I_{crystal}$, can be calculated to:

$$\left|I_{crystal}\right| = \frac{\left|V_{crystal}\right|}{\left|R_M + j\left(\omega L_M - \frac{1}{\omega C_M}\right)\right|}$$

Hence, the crystal drive level results to

$$P_{crystal} = \left|I_{crystal}\right|^2 \cdot R_M = \frac{R_M \left|V_{crystal}\right|^2}{{R_M}^2 + \left(\omega L_M - \frac{1}{\omega C_M}\right)^2}$$

ω denotes the angular frequency at which $|V_{crystal}|$ is measured.