# AN11189

## BGX7101 evaluation board application note

**Rev. 2.0 — 26 April 2012** **Application note**

### Document information

| Info | Content |
|---|---|
| **Keywords** | BGX7101, I/Q modulator, EVB, IP3, CP1, NF, PCB |
| **Abstract** | This application note describes the BGX7101 evaluation board (EVB) design and its performance. BGX7101 is an I/Q modulator designed for base station applications. This EVB includes the 50 Ω standard SMA connectors for ease of evaluation. |

### Revision history

| Rev | Date | Description |
|---|---|---|
| 1.0 | 20120413 | Initial version |
| 2.0 | 20120426 | Product Description: updated typical voltage gain value<br>Introduction: updated |

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# 1. Introduction

The evaluation board (EVB) described in this document allows evaluating the BGX7101.

This document provides the EVB circuit schematic, the bill of materials of the board, the information about PCB technology and its artwork, list of equipments for a typical test set-up required to evaluate the device. For typical test results, please see the data sheet.

# 2. Product Description

The BGX7101 is a high linearity I/Q modulator and provides 6 dB of typical voltage gain, 11.5 dBm of 1 dB output compression point ($OCP_{1dB}$) and 27 dBm typical outputs $IP3_O$. BGX7101 has 100 Ω differentials I/Q input termination internally. Thanks to its flexible input $V_{i(cm)}$ feature, any common mode voltage value between 0.25 V up to 3.3 V can be acceptable for similar RF performances.

The device could be used in a frequency band extension down to 400 MHz and up to 4 GHz.

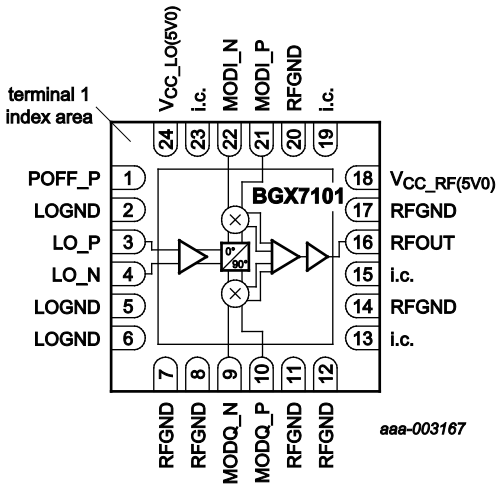



Fig 1. **Pin description**

Its high level of integration enables easy application usage and reduced BOM. Dedicated power OFF/ON pin permits to switch ON or OFF the device. In addition, multiple supply and ground pins allow for independent supply domains to improve the isolation between blocks.

# 3. EVB Circuit Description

The evaluation board was built on a 25 mil, 4 layers PCB using FR4 based technology and is illustrated in Fig.2 associated with its schematic in Fig.3.

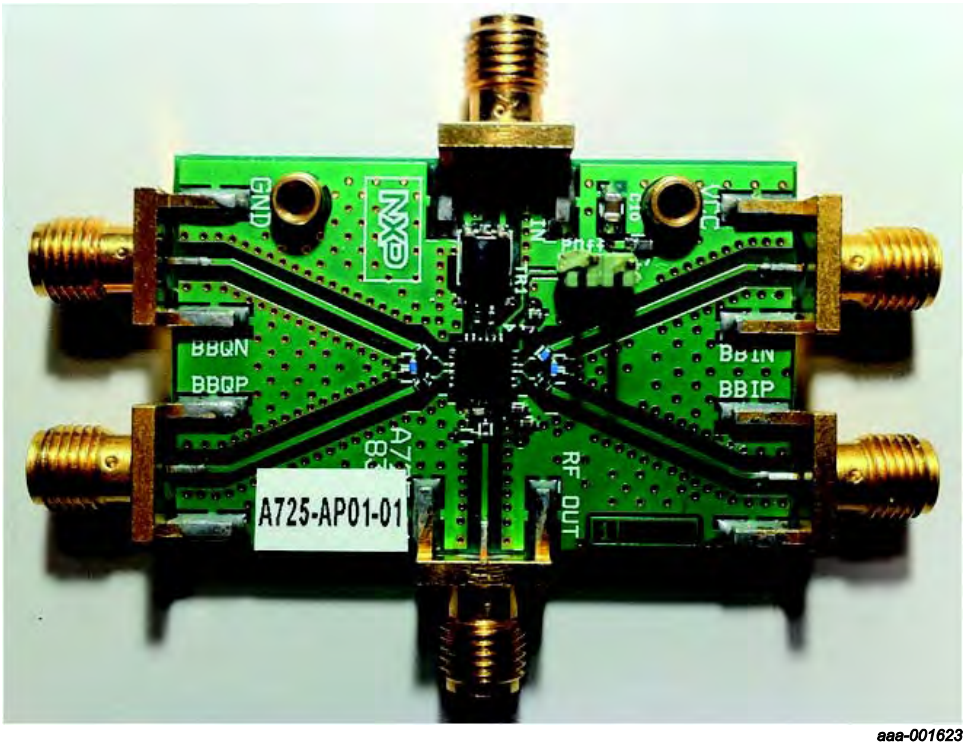



Fig 2. **Evaluation board**

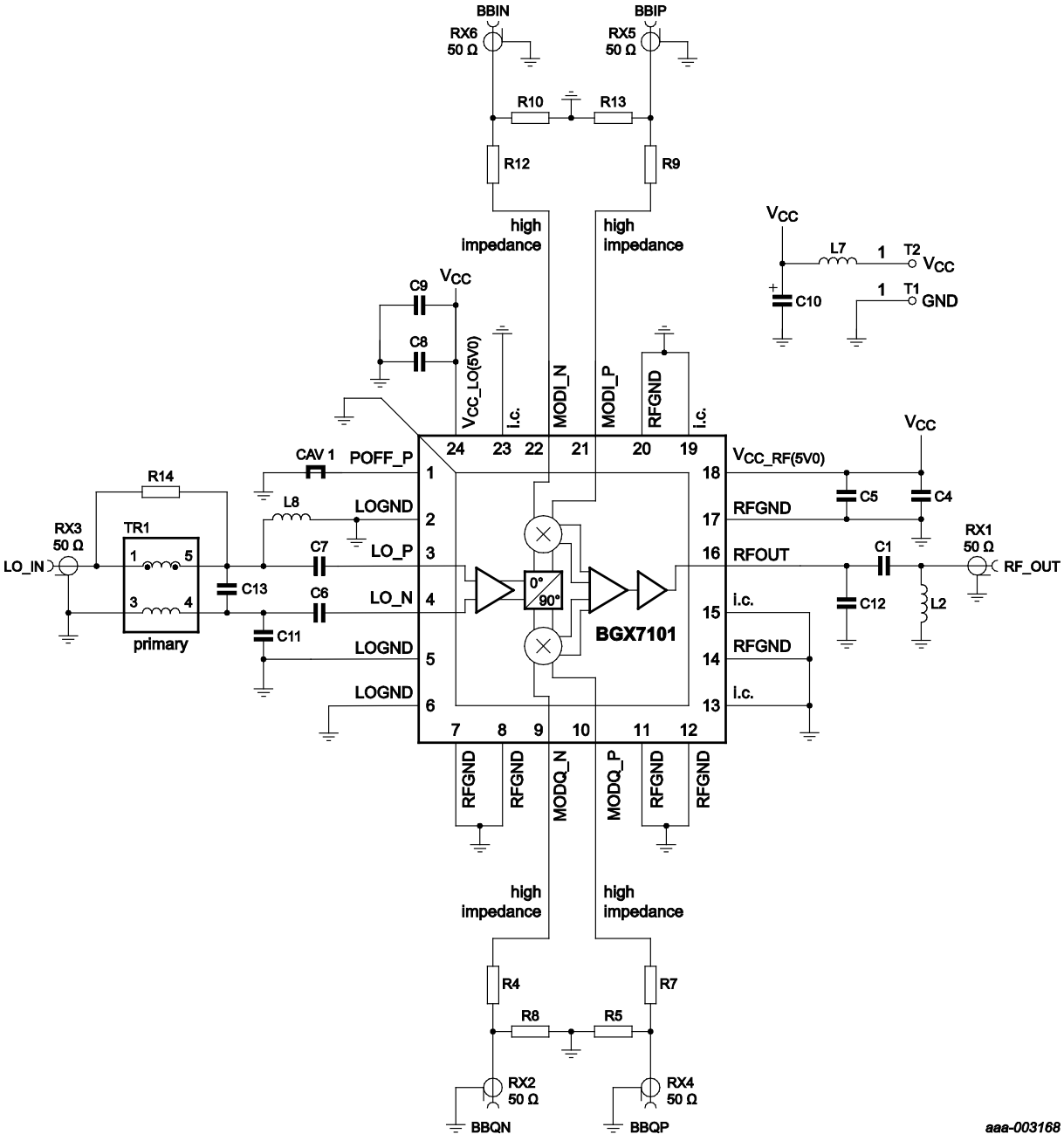



Fig 3. **Evaluation board schematic**

Two LO configuration options available, resulting two bills of material:

1. LO differential (use RF transformer to apply LO in differential between LO_N and LO_P)
2. LO single (LO source connected to LO_P using matching surface mount component, LO_N connected to ground using a DC bypass capacitor)

Choice depends on performances to be achieved.

LO differential mode will be chosen to improve Image suppression and IP2. Whereas LO single mode will be chosen to improve LO leakage.

### Bill Of Material (BOM) of BGX7101 EVB – LO differential

| Reference | Part | Description | Package | Vendors | Qty | Values |
|---|---|---|---|---|---|---|
| T1, T2 | 2 mm 200 – 52 Banana Plug | supply connector | | Multi Contact | 2 | |
| RX1, RX2, RX3, RX4, RX5, RX6 | 142-0701-851 | SMA connector, 50 Ω | | Emerson/Johnson | 6 | |
| L7 | BLM18SG700TN1D | ferrite bead | 0603 | Murata | 1 | |
| C10 | | capacitor | 0805 | Murata | 1 | 4.7 µF / 16 V |
| CAV1 | 2.54 mm header 2 ways | Poff drive | | Samtec | 1 | |
| C6, C7 | COG | capacitor | 0402 | Murata | 2 | 18 pF |
| C4, C9 | COG | capacitor | 0402 | Murata | 2 | 100 nF |
| C1 | COG | capacitor | 0403 | Murata | 1 | 39 pF |
| C5, C8 | COG | capacitor | 0402 | Murata | 2 | 22 pF |
| C12 | GJM1555C1HR70WB01 | capacitor | 0402 | Murata | 1 | 0.8 pF |
| C13 | GJM1555C1HR30WB01 | capacitor | 0402 | Murata | 1 | 0.3 pF |
| C11 | NC | | | | | |
| L2, L8 | NC | | | | | |
| TR1 | TC1-1-43A+ | LO transformer | AT224 – 1A | Mini-circuits | 1 | |
| R4, R7, R9, R12 | | resistor | 0402 | Murata | 4 | 0 Ω |
| R5, R8, R10, R13, R14 | NC | | | | | |
| U1 | BGX7101 | I/Q modulator | HVQFN24 (SOT616 – 3) | NXP | 1 | |

### Bill Of Material (BOM) of BGX7101 EVB – LO single

| Reference | Part | Description | Package | Vendors | Qty | Values |
|---|---|---|---|---|---|---|
| T1, T2 | 2 mm 200 – 52 Banana Plug | supply connector | | Multi Contact | 2 | |
| RX1, RX2, RX3, RX4, RX5, RX6 | 142-0701-851 | SMA connector, 50 Ω | | Emerson/Johnson | 6 | |
| L7 | BLM18SG700TN1D | ferrite bead | 0603 | Murata | 1 | |
| C10 | | capacitor | 0805 | Murata | 1 | 4.7 µF / 16 V |
| CAV1 | 2.54 mm header 2 ways | Poff drive | | Samtec | 1 | |
| C7, C11 | COG | capacitor | 0402 | Murata | 2 | 12 pF |
| C4, C9 | COG | capacitor | 0402 | Murata | 2 | 100 nF |
| C1 | COG | capacitor | 0402 | Murata | 1 | 39 pF |
| C5, C8 | COG | capacitor | 0402 | Murata | 2 | 22 pF |
| C12 | GJM1555C1HR70WB01 | capacitor | 0402 | Murata | 1 | 0.8 pF |
| L2 | NC | | | | | |
| L8 | | inductor | 0402 | Murata | 1 | |
| C13 | NC | | | | | |
| TR1 | NC | | | | | |
| R4, R7, R9, R12, R14, C6 | | resistor | 0402 | Murata | 6 | 0 Ω |
| R5, R8, R10, R13 | NC | | | | | |
| U1 | BGX7101 | I/Q modulator | HVQFN24 (SOT616 – 3) | NXP | 1 | |

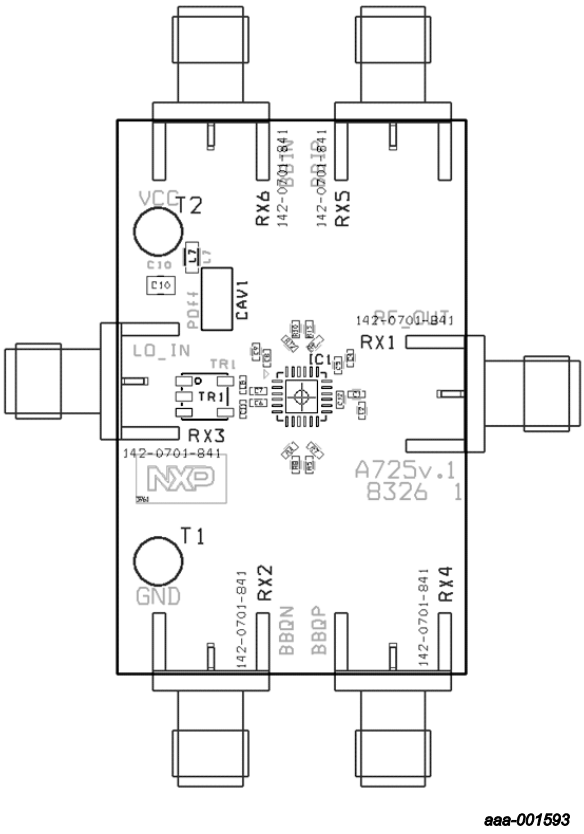



Fig 4. **Evaluation board component placement**

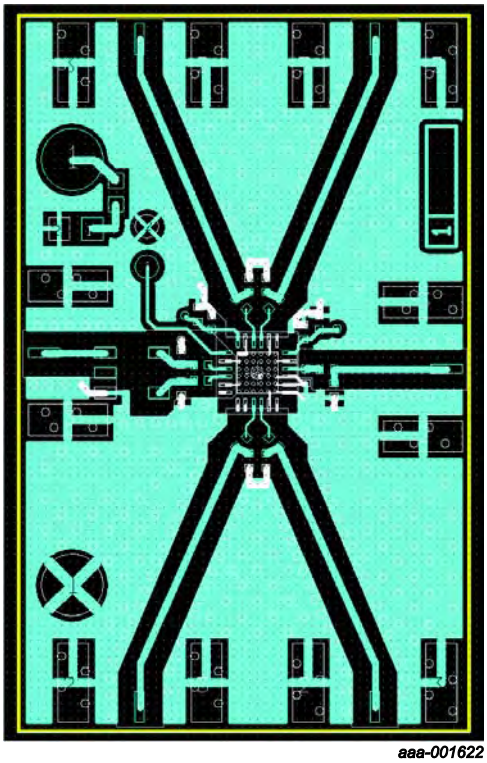



Fig 5. **Evaluation board top layer PCB layout**

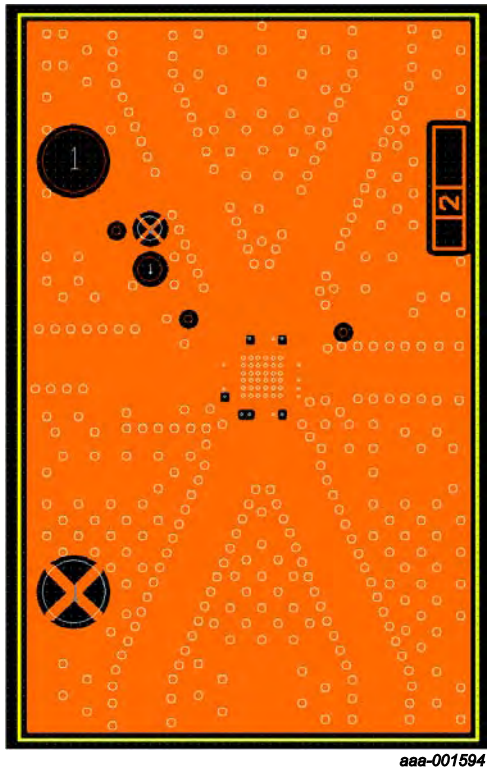



Fig 6. **Evaluation board inner layer_1 PCB layout**

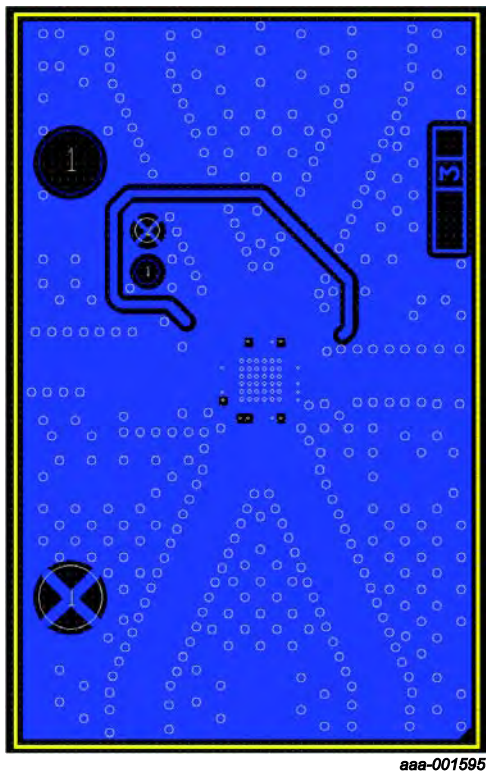



Fig 7. **Evaluation board inner layer_2 PCB layout**

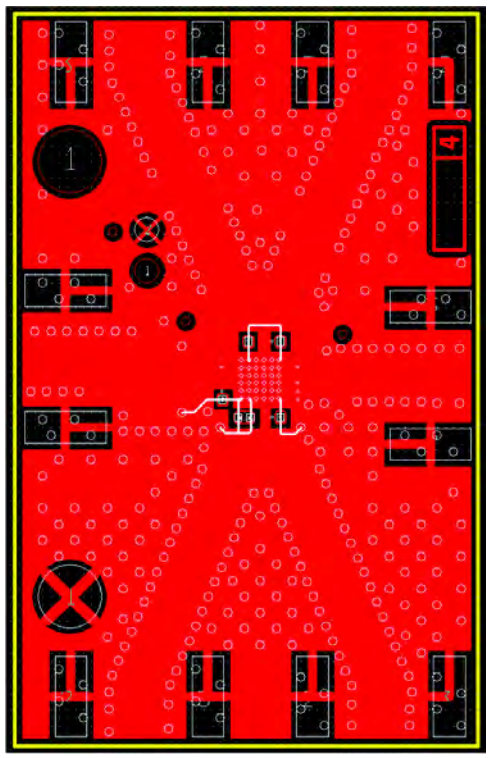
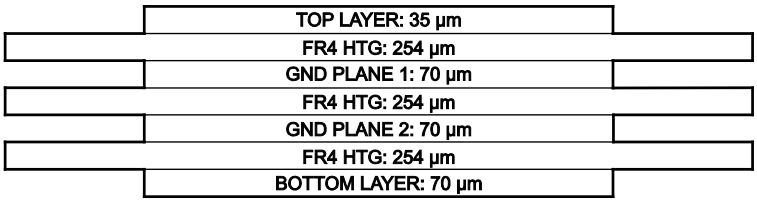



Fig 8. **Evaluation board bottom layer PCB layout**




(1) Etching class: Class5 standard.
(2) Minimum copper conductor with: 150 µm.
(3) Minimum conductor spacing: 150 µm.
(4) Ni-Au (Cobalt) finishing: 3 µm - 25 µm of nickel and 0.1 µm – 1.5 µm of gold.
(5) Board dimension: 45.5 mm x 28.75 mm.
(6) Solder mask both sides green color.
(7) Silkscreen on top layer white color.
(8) Finished thickness: 1 mm +/- 10 %.
(9) Top layer 460 µm traces are controlled impedance, 50 Ω lines.

Fig 9. **Evaluation board PCB technology**

# 4. Test Setup

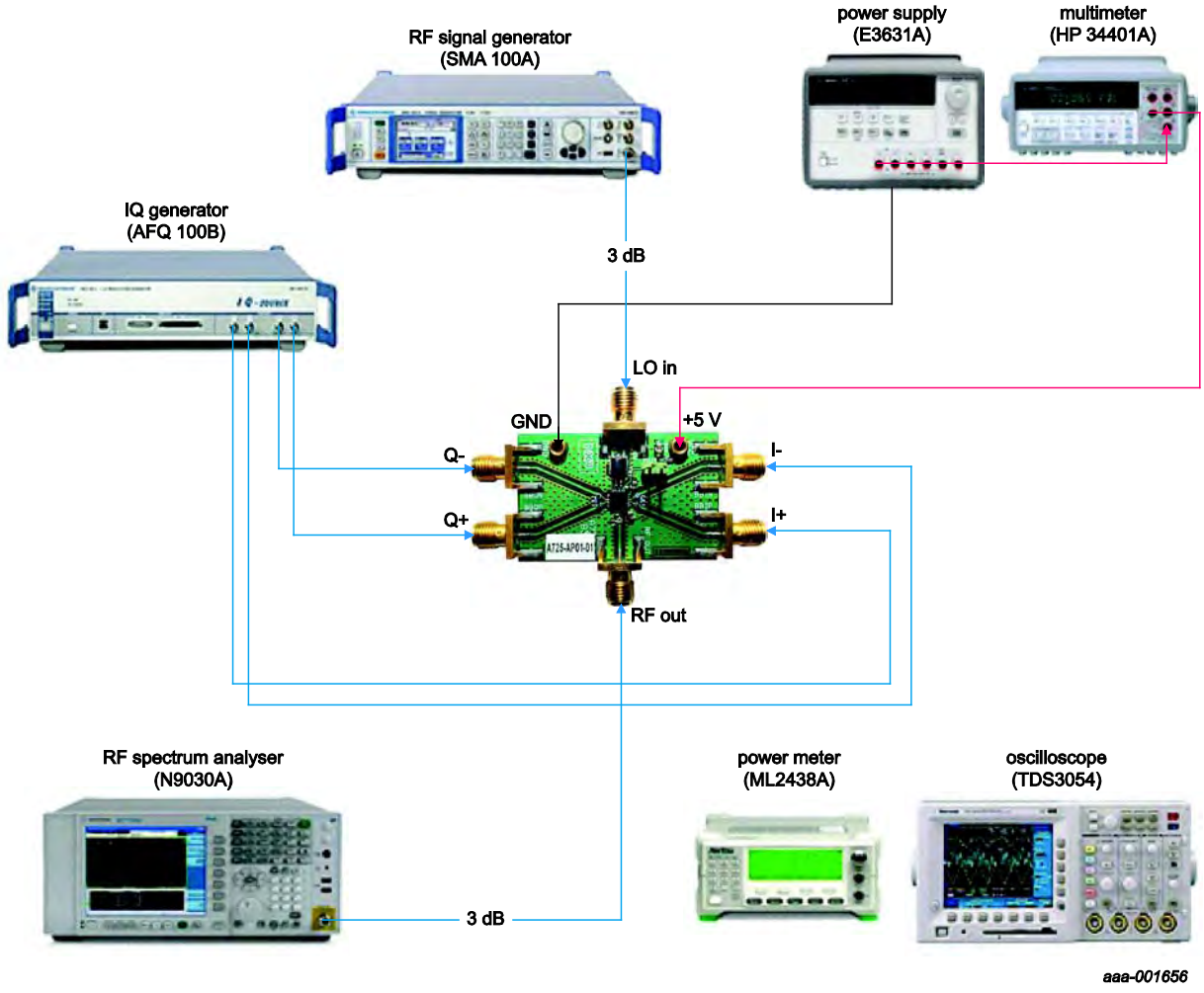



Fig 10. **Test setup block diagram**

# 5. Quick Start

The BGX7101 EVB kit is fully assembled and factory tested.

***Test Equipment Required***

Fig 10 shows the equipment required to verify the operation of the BGX7101 EVB kit. It is intended as a guide only, and some substitutions are possible.

***Connections***

This section provides a step-by-step guide to testing the basic functionality of the EVB kit. As a general precaution to prevent damaging the outputs by driving high-VSWR loads, **do not turn on DC power or RF signal generators until all connections are made:**

1. Connect 3 dB pads to the DUT ends of each RF signal generators and SMA cables (RF OUT / LO IN). This padding improves VSWR, and reduces the errors due to mismatch.
2. Measure loss in 3 dB pads and cables. Use this loss as an offset in all output power/gain calculations.
3. Disable all RF signal sources.
4. Connect the signal sources to the appropriate SMA inputs.
5. Set the LO and IF signal generators according to the following:
   - IF AWG signal source: 1 V (p-p) differential into DUT at 5 MHz
   - LO signal source: 0dBm into DUT at 1960 MHz

   ($f_{RF}$ = 1965 MHz)
6. Set the DC supply to +5.0 V and set a current limit around 250 mA. Connect supplies to the EVB kit through the ammeter. Turn on the supply.

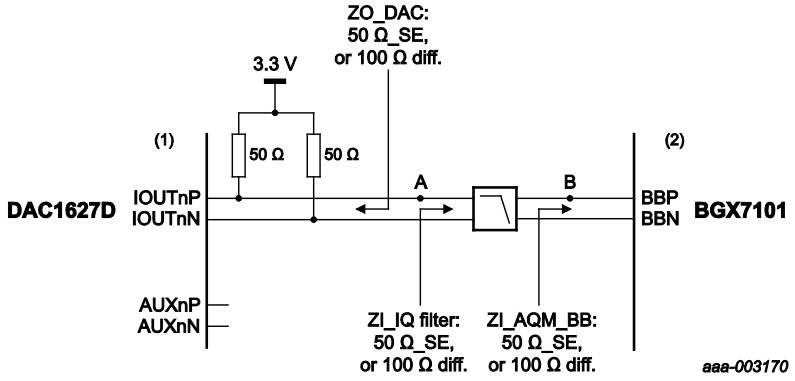
   Readjust the supply to get +5.0 V at the EVB kit. There will be a voltage drop across the ammeter when the mixer is drawing current.
7. Enable the LO and the IF sources.

## 6. DC Interface between DAC1627D1G25 and BGX7101

The DAC1627D1G25 is a 16-bit dual-channel digital-to-analog converter (DAC) with selectable 2x, 4x and 8x interpolating filters optimized for multi-carrier and broad band wireless transmitters at sample rates up to 1.25 Gsps. Supplied from 3.3 V and 1.8 V power sources, it integrates a differential scalable output current up to 31.8 mA. The mixer frequency is set by a high resolution 40-bit Numerically Controlled Oscillator (NCO). High resolution internal gain, phase and offset control provide outstanding image and LO rejection at the system analog modulator output. An inverse (sin x)/x function ensures controlled flatness at the DAC output. The LVDS DDR receiver interface allows a high data bandwidth (312.5 Msps) at the input.

When the system operation requires to keep the DC component of the complex spectrum which is the case for the zero-IF (direct up conversion) transmitters, the interface between DAC1627D1G25 and BGX7101 must be DC coupled. In that case, the offset compensation for LO cancellation can be handled by making use of the digital offset control in the DAC.

## 6.1 DC Interface utilization




(1) IOUTnP/IOUTnN (with n = A or B); $V_{o(cm)}$ = 2.8 V; $V_{o(diff)(p-p)}$ = 1 V.

(2) BBP/BBN; $V_{i(cm)}$ = 2.8 V; $V_{o(diff)(p-p)}$ = 1 V; offset correction via signal path (IOUTnP/IOUTnN (with n = A or B)).

Fig 11. **Example of DC interface with $V_{i(cm)}$ of 2.8V**

## 6.2 Recommendations about DC interface network:

As well as the LVDS parallel interface feature of the DAC1627D1G25, the flexibility of the BGX7101 in terms of common mode I,Q input dc voltage levels (0.25 V ~3.3 V) and its finite input impedance (100 Ω) simplifies the complete transmit chain application and enables the further integration.

We advice to use the digital offset control in the DAC (through the signal/modulation chain) which needs only a pull-up resistor (50 Ω)) per DAC output (Fig.11). In that case, a small amount of DAC dynamic should be reserved for the offset control purpose.

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