NXP Semiconductors
Application Note

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i.MX 6SLL Power Consumption Measurement

Contents

1 Introduction

This application note helps the user to design power management systems.Through several use cases,this report illustrates current drain measurements of the i.MX 6SLL system-on-chip (SoC), taken on the NXP EVK board. The reader will be enabled to choose the appropriate power supply domains for the i.MX 6SLL SoC and become familiar with the expected SoC power indifferent scenarios.

NOTE

Since the data presented in this application note is based on empirical measurements on a small sample size, the results presented are not guaranteed.

2 Overview of i.MX 6SLL Voltage Supplies

The i.MX 6SLL SoC has several power supply domains (voltage supply rails) and several internal power domains. Figure 1shows the connectivity of these supply rails and the distribution of the internal power domains.

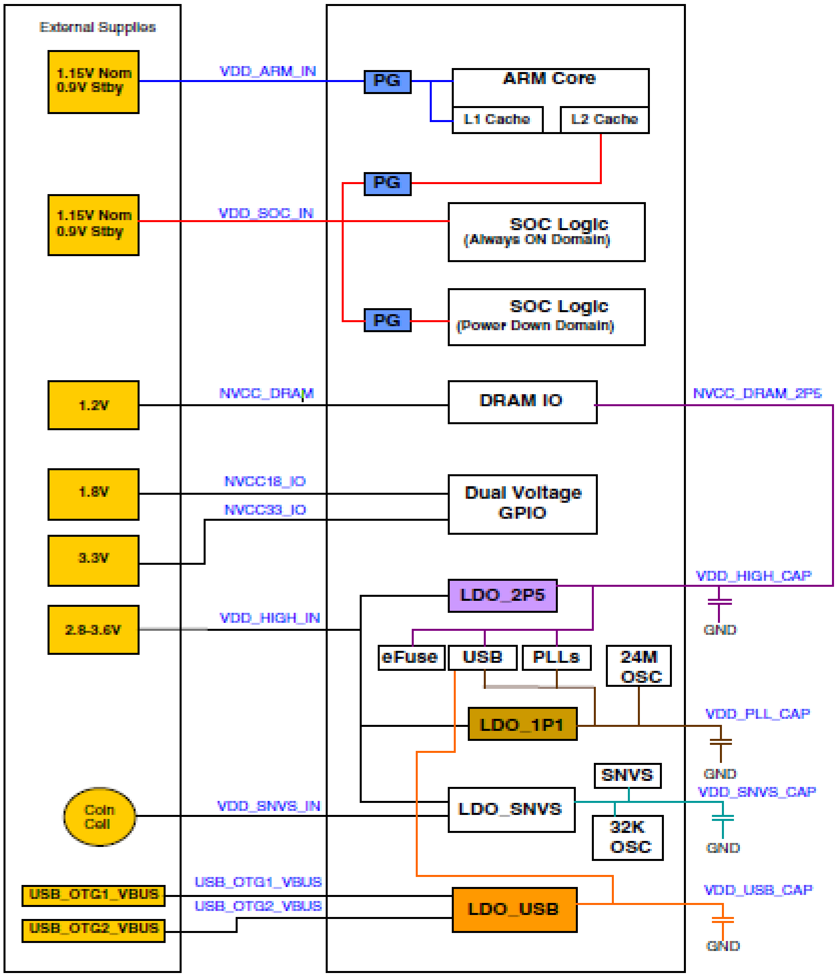

Figure 1. i.MX6SLL Power System

NOTE

See the i.MX 6SLL datasheet, for the recommended operating conditions of each supply rail and for a detailed description of the groups of I/Os (pins) each I/O voltage supply powers. For more details regarding the i.MX 6SLL power rails, see Power Management Unit (PMU) chapter in the i.MX 6SLL Applications Processors Reference Manual IMX6SLLRM

3 Internal Power Measurement of the i.MX 6SLL Processor

Several use cases (described in Section 4, “Use Cases and Measurement Results”) are run on theEVKboard. The measurements are taken mainly for the following power supply domains—VDDARM_IN, which is the ARM platform’s supply, VDDSOC_IN, which is the peripheral supply,VDDHIGH_IN, which is the source of PLLs, DDR pre-drives, PHYs,and some other circuitries.These supply domains consume the majority of the internal power of the processor.Forthe relevant use cases, the power of additional supply domains is added.However, the power of these supply domains does not depend on specific use cases, but whether these modules are used or not. The power consumption of SNVS is comparatively negligible except in Deep SleepMode.

The NVCC_*power consumption depends primarily on the board level configuration and the components. Therefore, it is not included in the i.MX 6SLL internal power analysis.The power of NVCC_DRAM is added for reference.

The powerconsumption forthese supplies,in different use cases,is provided in Table 1 through Table 3.

NOTE

Unless stated otherwise, all the measurements are done on typical process silicon, at room temperature (26 °C approximately).

3.1 Hardware and Software Used

The software versions used for the measurement are asfollows:

- Linux version used: Linux BSP version 4.1.15-2.1.0GA based on Linux kernel version 4.1.15
- The board used for the measurements is the MCIMX6SLL-EVK board.
- The measurements were performed using Agilent 34410A 6 ½ Digit Multimeter.

3.2 Measuring Points on the NXP EVK Board

Power data was collected on four major rails identified from the schematics of the platform, using 2 methodologies for measuring and calculating current on the respective rails.

For three rails (VDD_SOC_IN, VDD_HIGH_IN, LPDDR3_I/O+NVCC) shunts were removed and Ammeter was instrumented in series for respective rail. Final power data is calculated as the average of multiple samples/second collected by DMM multiplied with the rail's voltage.

For VDD_ARM_IN the default shunt resistor was removed and a calibrated 0.025 Ω shunt resistor value with 1% tolerance was setup for calculating current on the respective rail. The current is obtained by measuring the average voltage drop over the shunt resistor and dividingitbyitsvalue . Final power data is calculated as the product of calculated current and rail voltage.

Recommendation: Do not use the default shunt resistors found on the platform when measuring voltage drops; setup new shunt resistors with defined parameters values for measuring voltage drops!

Themeasuringpointsforthevarioussupplydomainsareasfollows:

- VDD_SOC_IN—The SOC domain current is measured on R783
  - VDD_ARM_IN—The ARM domain current is measured on R58
  - VDD_HIGH_IN—The VDDHIGH domain current is measured on R65
  - LPDDR3 I/O + NVCC —The current in this domain includes the NVCC_DRAM current and the overall current of the on-board LPDDR3 memory devices. The current in this domain is measured on R1919 .

4 Use Cases and Measurement Results

The main use cases and subtypes, which form the benchmarks for the i.MX 6SLL internal power measurements

on the EVK Platform, can be found at the following sections.

4.1 Low Power Mode Use Cases

4.1.1 Use Case 1— Deep Sleep Mode (DSM)

This mode is named as Dormant mode or Suspend to RA,in the Linux BSP.This is thelowest possible power state where external supplies are stillon.

Measurementcondition:

- CPU is power gated
- DDR is put in self refresh by SW, DDR IO isdisabled
- High-speed peripherals are power gated
- LDO_2P5 and LDO_1P1 are shut off
- 24 MHz XTAL is off, 24 MHz RCOSC is off
- All PLL are power down
- All clocks are shut off, only except 32 kHz RTC
- In this mode, no current flow is caused by external resistiveloads

Table 1 shows the measurement results when this use case is applied on the i.MX 6SLL processor.

Table 1. DSM Measurement Results

SupplyDomain	**Voltage(V)**	**4.1.15-2.1.0-GA_RC4**	
		P(mW)	**I(mA)**
VDD_ARM_IN	0.977	0	0
VDD_SOC_IN	0.98	0.4 15	0.4 24
VDD_HIGH_IN +NVCC33_IO	3.144	2.130	0.677
Total Power (exclude NVCC_DRAM +LPDDR3)	—	**2.545**	—
NVCC_DRAM + LPDDR3	1.205	3.134	2.6007
TotalPower	—	5.679	—

NOTE

For additional details on this use case and settings, see Section 6,"Use Cases Configuration and UsageGuidelines."

4.1.2 Use Case 2—Low Power Idle Mode

Measurementcondition:

- CPU is power gated
- DDR is put in self refresh by SW, DDR IO is disabled
- High-speed peripherals are clock gated, but remain powered
- LDO_2P5 and LDO_1P1 are set to weak mode
- 24 MHz XTAL is off, 24 MHz Hz RCOSC used as clock source
- All PLL are power down

This use case simulates the situation when the device is left idle for some time and the display isturned off after the timerexpires.

Table 2 shows the measurement results when this use case is applied on the i.MX 6SLL processor.

Table 2. Low Power Idle Mode Measurement Results

SupplyDomain	Voltage(V)	4.1.15-2.1.0-GA_RC4	
		P(mW)	I(mA)
VDD_ARM_IN	0.951	0.248	0.261
VDD_SOC_IN	0.94 6	2.082	2.201
VDD_HIGH_IN +NVCC33_IO	3.1 12	3.340	1.073
Total Power (exclude NVCC_DRAM +LPDDR3)	—	**5.669**	—
NVCC_DRAM + LPDDR3	1.197	4.059	3.391
TotalPower	—	9.728	—

NOTE

For additional details on this use case and settings, see Section 6, “Use Cases Configuration and Usage Guidelines.”

4.2 Application Use Cases

4.2.1 MP3 Audio Playback

Measurementcondition:

1. MP3 (MPEG-1 audio layer 3) decoding is done by ARM.
2. Audio playback is run through SSI (serial synchronous interface).
3. The stream used was an encoded mp3 file with 128 Kbps_44 kHz_.mp3 copied to and played from the SD (secure digital) card.

Table 3 shows the measurement results when this use case is applied on the i.MX 6SLL processor.

Table 3. MP3 Audio Playback Measurement Results

SupplyDomain	Voltage(V)	4.1.15-2.1.0-GA_RC4,CPU_FREQ=400MHz, governor=conservative	
		P(mW)	I(mA)
VDD_ARM_IN	0.979	18.500	18.906
VDD_SOC_IN	1.17	34.673	29.635
VDD_HIGH_IN +NVCC33_IO	3.111	35.491	11.408
Total Power (exclude NVCC_DRAM +LPDDR3)	—	**88.663**	—
NVCC_DRAM + LPDDR3	1.197	37.653	31.456
TotalPower	—	126.317	—

NOTE

For additional details on this use case and settings, see Section 6, "Use Cases Configuration and Usage Guidelines."

4.3 Dhrystone benchmark

Dhrystone is a synthetic benchmark used to measure the integer computational performance of processors and compilers. The small size of the Dhrystone benchmark allows it to fit into the L1 cahe and minimizes accesses to the L2 cache and DDR.

4.3.1 Use case: Dhrystone benchmark on ARM Cortex®-A9

In this use case, the Dhrystone test is performed by the ARM Cortex-A9 core.vThe following table shows the measurement results when this use case is applied on the i.MX 6SLL processor.

Table 4. Dhrystone benchmark measurement results on Cortex-A9 (ARM @ 996 MHz)

SupplyDomain	Voltage(V)	4.1.15-2.1.0-GA_RC4,CPU_FREQ=996MHz, governor=user_space	
		P(mW)	I(mA)
VDD_ARM_IN	1.278	471.923	369.267
VDD_SOC_IN	1.271	72.589	57.112
VDD_HIGH_IN +NVCC33_IO	3.111	32.111	10.322
Total Power (exclude NVCC_DRAM +LPDDR3)	—	**576.623**	—
NVCC_DRAM + LPDDR3	1.197	7.169	5.989
TotalPower	—	583.792	—

5 Reducing Power Consumption

The overall system power consumption depends on both software optimization and how the system hardware is implemented. Below is a list of suggestions that may help reduce system power. Some of these are already implemented in Linux BSP. Further optimizations can be done on the individual customer's system.

NOTE

Further power optimizations are planned for future BSP releases. See the NXP website to obtain the latest BSP release.

- Apply clock gating whenever clocks or modules are not used, by configuring CCGR registers in the Clock Controller Module (CCM).
- Reduce the number of operating PLLs: applicable mainly in Audio Playback mode or Idle modes.
- Core DVFS and system bus scaling: applying DVFS for ARM and scaling the frequencies of the

AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of the VDDARM and VDDSOC

domains. However, due to the reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memories. This trade-off needs to be taken into

account for each mode, to quantify the overall effect on system power.

- Put the i.MX 6 S LL into low-power modes (WAIT, STOP) whenever possible. See Chapter “Clock Controller

Module (CCM)”of the i.MX 6SLL Applications Processor Reference Manual (document IMX6SLLRM) for details.

- DDR interface optimization:
  - Use careful board routing of the DDR memories, maintaining PCB trace lengths as short as possible.
  - Use as reduced an ODT (On-Die Termination) setting as possible. The termination used greatly influences the power consumption of the DDR interface pins.
  - Use the proper output driver impedance for DDR interface pins that provide good impedance matching. Select the lowest possible drive strength that provides the required performance, in order to reduce current through DDR I/O pins.
  - Choose onboard resistors so the least amount of current is wasted. For example, when selecting impedance matching resistors between CLK and CLK_B .
  - When possible, in lower performance use cases, switching to DLL Off mode allows for greatly reducing DDR frequency. This disables or reduces termination, and it reduces the drive strength. Thus, power consumption of the DDR interface pins could be significantly reduced.
  - Float the i.MX 6 S LL LP DDR interface pins (set to high Z) when LP DDR memory is in Self-Refresh mode, and keep DDR_SDCKE0 and DDR_SDCKE1 at low value. If DDR_SDCKE0 and DDR_SDCKE1 are kept at low value by using external pull-down resistors, make sure there is onboard termination on these pins during this mode.
  - If possible (depending on system stability), configure DDR input pins to CMOS mode, instead of Differential mode. This can be done by clearing the DDR_INPUT bit in the corresponding registers in IOMUXC. This setting is mostly recommended when operating at low frequencies, such as in DLL Off mode.
  - Use of DDR memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

The various steps involved in floating the i.MX 6 S LL DDR interface pins are shown below.

NOTE

All the programming steps below are performed when the code is running from the internal RAM rather than from the DDR memory. The code is non-cacheable.

5.1 Steps to be performed before entering Suspend (Deep-Sleep mode):

1. Read the power saving status in MMDC in the MAPSR register (automatic power saving is enabled) to make sure that DDR is in Self-Refresh.
2. Do the following:
   a. If there is no onboard termination for DDR control and the address bus, set the DSE (drive strength selection, in IOMUXC) for all DDR IF I/O to 0 (High Z), except for CKE0 and CKE1.

   b. If the DDR control and address bus have onboard termination resistors connected to VTT, such as in the case where SODIMM is used:

      - Option 1

        As per 2a, keep SDCKE0/1 active, this causes some extra current from the pins sharing the same DSE control in IOMUXC_SW_PAD_CTL_GRP_CTLDS register. The pins are DRAM_CS0, DRAM_CS1, DRAM_SDBA2, DRAM_SDCKE0, DRAM_SDCKE1, and DRAM_SDWE.
      - Option 2 (requires onboard pull down resistors on DRARM_SDCKE0/1 pins)

- Set the supply of the termination resistor to be floated (this can be done through pins with GPIO capability).
- Set the DSE (drive strength selection, in IOMUXC) for all DDR IF I/O to 0 (High Z).

3. Go into the Suspend mode.

5.2 Steps to be performed after exiting Suspend:

1. Restore all the settings for the DDR I/O to the required values.
2. The system proceeds to Run mode.

NOTE

If the system can ensure there are no masters accessing the DDR, the following may be applied to other scenarios besides Deep-Sleep mode: DDR pins can be floated in the same manner, even when Suspend is not entered, and DDR can be manually put into Self-Refresh to save power. This happens when the CPU is not running, or it is running from the internal RAM.

6 Use Case Configuration and Usage Guidelines

6.1 Deep-Sleep mode

In this use case all clocks and PLLs are turned off except the 32 kHz clock which is for system wake up.

1. Boot up Linux OS image.
2. Run below command to let system enter DSM mode:

   echo mem > /sys/power/state
3. Measure the power and record result.

6.2 Low Power Idle mode

6.2.1 Low Power Idle mode: clock configuration

Table 5. Low Power Idle mode clock configuration

Clock Name	Frequency (MHz)
AXI	24 MHz
AHB	3 MHz
CPU	0 MHz
MMDC P0	1 MHz

6.2.2 Low Power Idle mode: PLL configuration

Table 6. Low Power Idle mode PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	0 MHz
PLL2—System Bus PLL	0 MHz
pll2 396m pfd	0 MHz
pll2 352m pfd	0 MHz
pll2 594m pfd	0 MHz
pll2 198m pfd	0 MHz
PLL3—OTG USB PLL	0 MHz
pll3 508m pfd	0 MHz
pll3 454m pfd	0 MHz
pll3 720m pfd	0 MHz
pll3 540m pfd	0 MHz
PLL4—Audio PLL	0 MHz
PLL5—Video PLL	0 MHz
PLL6—ENET PLL	0 MHz
PLL7—Host USB PLL	0 MHz

6.2.3 Low Power Idle mode: system setup

Disconnect everything except the SD.

1. Boot up Linux image with "*x11=false uart_from_osc* "in cmdline.
2. Run the following script to let the system enter powersave governor:

3.
   ```
   #!/bin/bash
           echo 8 > /proc/sys/kernel/printk
           ifconfig eth0 down
           ifconfig eth1 down
           echo powersave > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
           echo 1 > /sys/class/graphics/fb0/blank
   ```
4. Measure the power and record the result.

6.3 MP3 Audio Playback

6.3.1 MP3 Audio playback: clock configuration

Table 7. Maximum power clock configuration

Clock Name	Frequency(MHz)
AXI	24MHz
AHB	24 MHz
CPU	396 MHz
MMDC CH0	100MHz

6.3.2 MP3 Audio playback: PLL configuration

Table 8. Maximum power PLL configuration

PLL Name	Frequency(MHz)
PLL1—System PLL	0
PLL2—System Bus PLL	528 MHz
pll2 396m pfd2	396 MHz
pll2 352m pfd0	0
pll2 594m pfd1	0
pll2 198m pfd	0
PLL3—OTG USB PLL	480 MHz
pll3 508m pfd	0
pll3 454m pfd	454 MHz
pll3 720m pfd	720 MHz
pll3 540m pfd	0
PLL4—Audio PLL	0
PLL5—Video PLL	649 MHz
PLL6—ENET PLL	500 MHz
PLL7—Host USB PLL	0

6.3.3 MP3 Audio playback—system setup

- SD boot
- Connect LCD panel

6.3.4 MP3 Audio playback—steps

1. Boot up Linux image with*“$mmcargs enable_wait_mode=on*"
2. Run the following script to let the system enter *conservative* governor
3.
```
#!/bin/sh
        echo 1 > /sys/class/graphics/fb0/blank
        echo 1 > /sys/class/graphics/fb1/blank
echo 1 > /sys/class/graphics/fb2/blank
echo 1 > /sys/class/graphics/fb3/blank
ifconfig eth0 down
cpufreq-set -u 396000
cpufreq-set -g conservative
cpufreq-info
```

4. Play audio:

```
pacmd set-default-sink 1;while [ 1 ];
do gplay-1.0 ./128kbps_44khz_s_mp3.mp3;done;
```

5. Measure the power and record the result.

6.4 Dhrystone on Cortex-A9

6.4.1 Dhrystone on Cortex-A9: clock configuration

Table 9. Dhrystone clock configuration

Clock Name	Frequency(MHz)
AXI	264 MHz
AHB	132 MHz
CPU	996MHz
MMDC p0	396 MHz

6.4.2 Dhrystone on Cortex-A9: PLL configuration

Table 10. Dhrystone PLL configuration

PLL Name	Frequency(MHz)
PLL1—System PLL	0
PLL2—System Bus PLL	528 MHz
pll2 396m pfd2	396 MHz
pll2 352m pfd0	0
pll2 594m pfd1	0
pll2 198m	0
PLL3—OTG USB PLL	480 MHz
pll3 508m pfd2	0
pll3 454m pfd3	454 MHz
pll3 720m pfd0	0
pll3 540m pfd1	0

Table continues on the next page...

Table 10. Dhrystone PLL configuration (continued)

PLL4—Audio PLL	0
PLL5—Video PLL	0
PLL6—ENET PLL	0
PLL7—Host USB PLL	0

6.4.3 Dhrystone on Cortex-A9: system setup

- SD boot
- Connect LCD panel

6.4.4 Dhrystone on Cortex-A9: steps

1. Boot up the Linux image and boot the board to the SD rootfs
2. Run the following script to measure at 528 MHz or 800MHz:

```
#!/bin/sh
ifconfig eth0 down
ifconfig eth1 down
echo 1 > /sys/class/graphics/fb0/blank;
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor;
echo 996000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed;
```

3. Run dry2 and measure:

```
while true; do dry2; done
```

4. Measure the power and record the result.

7 Revision History

Table 11. Revision history

Rev.Number	Date	Substantive Change(s)
Rev. 0	6/2017	Initial public release.

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