

i.MX 8M Mini to i.MX 8M Nano Design Compatibility Guide

Hardware Product Design Focus

1. Introduction

The 8M Nano was designed to be a subset of the 8M Mini, with a few added features to enhance the device. This guide provides an overview of how to design a product using the i.MX 8M Mini when the final product will utilize an i.MX 8M Nano.

This guide focuses on the hardware features and requirements to ensure a smooth transition between the two application processors.

This can also be expanded to product families that extend new customer features by upgrading from an i.MX 8M Nano to an i.MX 8M Mini, while maintaining production costs by utilizing the same product PCB design within the product family.

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2. Feature comparison

Table 1 provides a quick feature comparison of the i.MX 8M Mini and i.MX 8M Nano. This is intended as a quick introduction to the devices. Refer to the device datasheet for a full description.

Table 1. Quick Feature Comparison

Feature	i.MX 8M Mini	i.MX 8M Nano
Main CPU	4x A53 @ 1.8 GHz OD	4x A53 @ 1.5 GHz OD
Microcontroller	M4	M7
DDR	32x / 16x LPDDR4-3000 DDR4-2400 DDR3L-1600	16x / 8x LPDDR4-3200 DDR4-2400 DDR3L-1600
Memory	8-bit NAND Interface (3x) eMMC 5.1 (3x) SPI NOR FlexSPI with XIP	8-bit NAND Interface (3x) eMMC 5.1 (3x) SPI NOR FlexSPI with XIP
GPU	GCNanoUltra + GC320	GC7000UL
VPU	1080p60 VP9 Profile 0, 2 (10-bit) 1080p60 HEVC/H.265 Decoder 1080p60 AVC/H.264 Decoder 1080p60 VP8 1080p60 AVC/H.264 Encoder 1080p60 VP8 TrustZone support	None
Display	LCDIF Display Controller 4 Lane MIPI DSI	LCDIF Display Controller 4 Lane MIPI DSI
Camera	4 Lane MIPI CSI	4 Lane MIPI CSI
Synchronous Audio Interface (SAI) modules	5x SAI Modules (SAI1) 8 TX & 8 RX (SAI2) 2 TX & 2 RX (SAI3) 2 TX & 2 RX (SAI5) 4 TX & 4 RX (SAI6) 1 TX & 1 RX	5x SAI Modules --- (SAI2) 2 TX & 2 RX (SAI3) 2 TX & 2 RX (SAI5) 4 TX & 4 RX (SAI6) 1 TX & 1 RX (SAI7) 1 TX & 1 RX
Audio (additional)	S/PDIF 8-Channel Pulse Density Modulation (PDM) input --- 384 KHz sampling	S/PDIF 8-Channel Pulse Density Modulation (PDM) input ASRC 768 KHz sampling
Connectivity	--- PCIe (2x) USB 2.0 (3x) uSDHC (1x) Gigabit Ethernet (4x) UART (4x) I2C (3x) ECSPi	--- (1x) USB 2.0 (3x) uSDHC (1x) Gigabit Ethernet (4x) UART (4x) I2C (3x) ECSPi
Package	14 x 14 mm 486-pin BGA, 0.5 mm pitch	14 x 14 mm 486-pin BGA, 0.5 mm pitch

3. i.MX 8M Mini to Nano audio compatibility

As shown in the comparison table (Table 1), the audio feature sets are different between the 8M Mini and 8M Nano. However, it is possible to create a prototype design with an 8M Mini and target the 8M Nano for production.

Table 2. 8M Mini and 8M Nano Audio Port Configuration

Port	8M Mini	8M Nano	Compatibility	Comments
SAI1	8-Tx/8-Rx	Not Available	No	Mini only, Nano SAI1 pins are No Connections
SAI2	2-Tx/2-Rx	2-Tx/2-Rx	Compatible	Nano includes additional capabilities
SAI3	2-Tx/2-Rx	2-Tx/2-Rx	Compatible	Nano includes additional capabilities
SAI5	4-Tx/4-Rx	4-Tx/4-Rx	Compatible	
SAI6	1-Tx/1-Rx	1-Tx/1-Rx	No	SAI6 is multiplexed behind SAI1 pins on the MINI
SAI7	Not Available	1-Tx/1-Rx	No	Nano only
SPDIF	1-Tx/1-Rx	1-Tx/1-Rx	Compatible	
PDM	Up to 8-Mics	Up to 8-Mics	Compatible	Must use SAI5 pins with IOMUX Alt 4

3.1. One-Lane I2S interface

As shown in Table 2, SAI2 and SAI3 are best considered as 1-Tx/1-Rx for compatibility solutions.

3.2. Two-Lane I2S interface

For Two-lane I2S implementations, the data channels for RX and TX need to be on the same SAI interface. The 8M Mini does not support the internal SAI synchronization to use SAI2 and SAI3 together as Four-lane Tx or Rx (or both).

The ASRC module was added to the 8M Nano which provides the SAI synchronization between the modules.

For design compatibility, the alternate pin multiplexing of the SAI5 module is key to the flexibility:

- SAI5 pins can support 4-Rx or 1-Tx/1-Rx with IOMUX Alt 0 and Alt 3
- SAI2 pins can support SAI5 4-Tx with IOMUX Alt 1
- SAI3 pins can support SAI5 4-Rx with IOMUX Alt 2

3.3. PDM inputs

For compatibility, the PDM interface, on the 8M Nano, is only accessible as an alternate function of the SAI5 pins (Alt 4). Suggested configurations for PDM compatibility are listed in [Table 3](#) and [Table 4](#).

Table 3. Two PDM Microphones

Mini & Nano Pin	IOMUX Alt0	IOMUX Alt 3	IOMUX Alt 4	Description
SAI5_RXC			PDM.CLK	Microphone Clock
SAI5_RXD0			PDM.BIT[0]	Mic data for 2 microphones
SAI5_RXD1		SAI5.TX_SYNC		SAI5 1-Lane Tx
SAI5_RXD2		SAI5.TX_BCLK		SAI5 1-Lane Tx
SAI5_RXD3		SAI5.TX_DATA[0]		SAI5 1-Lane Tx
SAI5_MCLK	SAI5_MCLK			SAI5 1-Lane Tx

Table 4. Three to eight PDM Microphones

Mini & Nano Pin	IOMUX Alt0	IOMUX Alt 3	IOMUX Alt 4	Description
SAI5_RXC			PDM.CLK	Microphone Clock
SAI5_RXD0			PDM.BIT[0]	Mic data for 2 microphones
SAI5_RXD1			PDM.BIT[1]	Mic data for 2 microphones
SAI5_RXD2			PDM.BIT[2]	Mic data for 2 microphones
SAI5_RXD3			PDM.BIT[3]	Mic data for 2 microphones

3.4. Audio compatibility summary

It is possible to prototype many configurations of audio products using i.MX 8M Mini before the i.MX 8M Nano is available. There is pin compatibility, but it is not 100 % due to the reduced pin count and functionality of the 8M Nano device. For compatibility:

- Do not use SAI1
- PDM inputs are only available on the SAI5 primary pins
- SAI2 supports an alternate function which can be used for SAI5 4-lane Tx
- SAI3 supports an alternate function which can be used for SAI5 4-lane Rx
- Three MCLK I/Os are available with extensive routing capabilities within the SoC
 - Two Frac-N audio PLLs are supported by both 8M Mini and 8M Nano

This description is focused on compatibility between the 8M Mini and 8M Nano. Both devices have unique capabilities that are not described within this document.

4. Key differences for hardware design

The Feature Comparison table ([Table 1](#)) provides a quick insight into the functional blocks that changed between the two devices. The next sections focus on key differences between the i.MX 8M Mini and i.MX 8M Nano that affect the HW PCB design. These are:

- Peripherals per device
- DDR memory interface

- Boot Selections
- IOMUX Selections
- Power Supplies
- PMIC Part Number
- On-die Resistors
- Enter Boundary-scan Mode
- JTAG_TMS recommendation

The following sections provide an in-depth discussion of how to manage the HW differences between the i.MX 8M Mini and i.MX 8M Nano devices.

4.1. Signal terminations

The differences in peripherals per device are not discussed at length. The Feature Comparison table and the package pin sections quickly highlight the differences between the devices. Since the package and pinout between the 8M Mini and 8M Nano are the same, your HW design can utilize all the features of both devices. However, when an 8M Nano is placed on the PCB, then your design must provide signal terminations for peripherals that are not implemented.

PCIe, for example, is not implemented on the 8M Nano. Your design should provide manufacturing options for resistor terminations on the PCIe signals. It is not good design practice to allow floating PCB traces. With proper terminations, the same PCB can use PCIe with an 8M Mini installed or non-PCIe with an 8M Nano installed.

4.2. DDR interface

The i.MX 8M Mini provides a programmable DDR data bus width, x16 or x32. The i.MX 8M Nano only supports DDR x16 or x8. Thus, the HW designer must understand the final product requirements. If the final target is the 8M Nano device, then the DDR bus should be designed as x16. This way, both processors will be functional on the PCB.

An alternate option is to use a x32 DDR memory package within the design. Then only one half of the memory will be used with an 8M Nano processor is installed.

The DDR controller within both the 8M Mini and 8M Nano devices uses the DRAM_DQ[15:0] pins when a x16 memory interface is selected. For the 8M Nano, the DRAM_DQ[31:16], DRAM_DM[3:2], DRAM_DQS2_[N:P], and DRAM_DQS3[N:P] pins are no connects within the 14x14 BGA package.

For 8M Nano PCB designs, these pins are normally only connected to a pad on the PCB, not board routing attachments. It is not preferable to have dangling DDR address and control signals when a x16 memory is de-populated.

4.2.1. LPDDR4 x16 packages

The JEDEC standard package for LPDDR4 is a x32 memory. The memory interface and operation can be thought of as two x16 memory dies in a single package. The address and control signals are

duplicated in each x16 data half. This is ideal for scalability from 8M Mini to 8M Nano as discussed in previous sections.

The x16 LPDDR4 memory package would only utilize the “A” side of the memory interface, while the “B” side will be package no connects. It is envisioned that this memory package would be the same between x16 and x32 devices.

When designing for LPDDR4 x16 and x32 memories, ensure that DRAM_DATA[15:0] is connected to the “A” side of the memory package. This allows both the 8M Mini and 8M Nano to utilize the scalability of future memory packages. During HW development, the x32 memory can be used with the 8M Nano, though only the “A” side of the memory will be functional in this setup.

4.3. Boot Mode controls

The HW boot mode controls are implemented differently between the 8M Mini and 8M Nano devices, with the same resulting functional boot operation. The 8M devices provide two boot control methods: production fuses, or prototype via GPIO.

NOTE

This document is not intended to supersede the device data sheets or reference manuals. Those documents define the modes and operation of the device. This guide is intended to build upon those documents.

4.3.1. Boot Mode fuses

The fuse maps for the 8M Mini and 8M Nano are similar but not the same. Consult the fuse maps for each device to ensure compatibility.

4.3.2. Boot ROM differences

The 8M Nano Boot ROM is different from the 8M Mini. Consult the Reference Manuals for both the 8M Mini and 8M Nano for your specific boot device selection.

4.3.3. GPIO Boot control

All i.MX 8M devices provide a boot control option for using GPIO pins to define the boot source or method. The GPIO Boot control is intended for hardware development and provides boot control flexibility.

The difference in the target PCB design for an 8M Mini or an 8M Nano is in the GPIO pins used to select a specific boot mode. As shown above in the Feature Comparison Table, the i.MX 8M Nano did not implement the SAI1 pins and functions. These pins are not connected to the 8M Nano package. For the 8M Mini, the SAI1 pins were utilized as the Boot Mode Selection pins. This required the 8M Nano to implement a different Boot Mode Selection. The table below compares the Boot Mode Selection between the devices.

The boot features of the 8M Mini were not removed on the 8M Nano, they just require you to burn fuse bits and boot from the internal fuses. One example might be booting from SD1. The feature is available on the 8M Nano although it is not selectable from the Boot Mode pins on an unprogrammed device.

Refer to the 8M Nano Reference Manual for all the available boot options and features supported using the internal fuse map.

The following table provides the 8M Mini pin settings to emulate an un-fused 8M Nano Boot Function. As described above, the SAI1 pins on the 8M Mini are used to select the specific Boot Function and features. This will allow your design to boot the same for both devices, assuming no fuses are burned.

CAUTION

The 8M Nano supports a boot feature for a NAND memory with 512 pages in a block. The 8M Mini only supports NAND devices up to 256 pages in a block. This is `BOOT_MODE [3:0] = 0101` on the 8M Nano.

Table 5. i.MX 8M Mini Setup for 8M Nano Boot Functions

8M Mini Pins / 8M Nano Pins	i.MX 8M Mini and i.MX 8M Nano Boot Function							
	Boot from Internal Fuses	USB Serial Downloader	USDHC3 Boot (eMMC boot only, SD3 8-bit)	USDHC2 Boot (SD boot only, SD2)	NAND Boot (8-bit single device 256 page)	Flex SPI Boot (3B Read)	Flex SPI Boot (Hyperflash 3.3V)	ECSPI Boot (ECSP11, ECSP11_SS0, 24-bit)
TEST_MODE / BOOT_MODE3	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 0	0 / 1
JTAG_TRST_B / BOOT_MODE2	X / 0	X / 0	X / 0	X / 0	X / 1	X / 1	X / 1	X / 0
BOOT_MODE1 / BOOT_MODE1	0 / 0	0 / 0	1 / 1	1 / 1	1 / 0	1 / 1	1 / 1	1 / 0
BOOT_MODE0 / BOOT_MODE0	0 / 0	1 / 1	0 / 0	0 / 1	0 / 0	0 / 0	0 / 1	0 / 0
8M Mini Only Pins								
SAI1_TXD7 (BOOT_CFG[15])	X	X	0	0	0	0	0	0
SAI1_TXD6 (BOOT_CFG[14])	X	X	0	0	0	1	1	1
SAI1_TXD5 (BOOT_CFG[13])	X	X	1	0	1	0	0	1
SAI1_TXD4 (BOOT_CFG[12])	X	X	0	1	1	0	0	0
SAI1_TXD3 (BOOT_CFG[11])	X	X	1	0	1	0	0	0
SAI1_TXD2 (BOOT_CFG[10])	X	X	0	1	1	0	0	0
SAI1_TXD1 (BOOT_CFG[9])	X	X	1	1	0	0	1	0
SAI1_TXD0 (BOOT_CFG[8])	X	X	0	0	0	0	1	0
SAI1_RXD7 (BOOT_CFG[7])	X	X	0	0	0	0	0	0
SAI1_RXD6 (BOOT_CFG[6])	X	X	0	0	1	0	0	X
SAI1_RXD5 (BOOT_CFG[5])	X	X	1	0	0	0	0	X
SAI1_RXD4 (BOOT_CFG[4])	X	X	0	1	0	0	0	X
SAI1_RXD3 (BOOT_CFG[3])	X	X	0	0	0	0	0	X
SAI1_RXD2 (BOOT_CFG[2])	X	X	0	0	0	0	0	X
SAI1_RXD1 (BOOT_CFG[1])	X	X	1	1	0	0	0	X
SAI1_RXD0 (BOOT_CFG[0])	X	X	1	1	0	0	0	X

As shown in [Table 5](#), the 8M Nano device re-purposed two existing pins of the 8M Mini: TEST_MODE and JTAG_TRST_B. Both pins exist at the same BGA pin location on each device but are renamed and re-purposed for Boot Mode selection.

The TEST_MODE pin on the 8M Mini was used to select the Factory Test mode. For normal usage, this pin has always been connected to GROUND. For the 8M Nano device, the TEST_MODE pin has been changed to BOOT_MODE3. Unless you plan to use ECSPI booting, you can tie the TEST_MODE / BOOT_MODE3 to GROUND for both implementations.

The JTAG_TRST_B pin on the 8M Mini was connected to the SJTAG module and performed a TAP reset within the SJTAG logic. The JTAG debuggers currently available have dropped this signal requirement. The ARM 10-pin JTAG connector does not support this JTAG signal. Since this signal was already part of the signal fanout of the BGA and was not actively required, it was the prime candidate for conversion to BOOT_MODE2 pin.

For 8M Mini to 8M Nano design conversions, it is recommended to add an additional resistor to the 8M Mini design. It should be connected to the JTAG_TRST_B pin and tied (high or low) for your planned Boot Mode selection when prototyping with the 8M Nano device. If you intend to plan for multiple modes, then two resistors will be required: one tied high and one tied low. For the 8M Mini design, this new selection would be de-populated since this device contains an internal PU resistor. If you implement the two-resistor option, you could place a weak pull-up (~47K) for both designs and then use a solder short, zero-ohm, external logic, jumper, or switch to sink the BOOT_MODE2 line as required.

CAUTION

Connecting the JTAG_TRST_B pin to a logic LOW level will inhibit use of the JTAG interface on i.MX 8M Mini. The JTAG_TRST_B pin is an optional active-low reset for the SJTAG logic. Refer to the IEEE 1149.x standard for a full definition of the signal operation within JTAG.

4.3.4. S/W Impacts of Boot Mode differences

For boot operation compatibly between the 8M Mini and 8M Nano, it is suggested to configure the SAI1 GPIO settings as intended for the 8M Nano boot selection. Thus, your boot SW will operate the same between both devices. It will ensure a quick and smooth transition to the 8M Nano implementation.

Refer to the device reference manuals for the full definition of each Boot Mode configuration.

4.4. IOMUX differences

For the i.MX devices, the IOMUX refers to the module that multiplexes each IO pin. This programmable module provides SW selection of multiple IO features on each of the IO pins. These are well defined within the device reference manuals.

The 8M Nano is a reduced peripheral subset of the 8M Mini. An easy example is the removal of the PCIe peripheral. Even though the 8M Nano is a reduced subset, the IOMUX added new IO selections. Thus, the 8M Nano provides new features that are not available on the 8M Mini. When designing for dual 8M usage, you should design to the 8M Mini IOMUX. This ensures that the IO features will be available on both the 8M Mini and 8M Nano. The table below highlights these changes.

- The shaded **RED** text indicates selections that were deleted on the 8M Nano.
- The normal text indicates functional options to are new on the 8M Nano and not available on the 8M Mini.

Table 6. Different IOMUX Selections in the 8M Nano

i.MX 8M Pins	0	Alt1	Alt2	Alt3	Alt4	5	Alt6
BOOT_MODE2		I2C1_SCL					
BOOT_MODE3		I2C1_SDA					
GPIO1_IO08			PWM1_OUT				
GPIO1_IO09			PWM2_OUT				
GPIO1_IO10			PWM3_OUT				
GPIO1_IO11		PWM2_OUT					
GPIO1_IO14		USB2_OTG_PWR					
GPIO1_IO15		USB2_OTG_OC					
ENET_MDC			SAI6_TX_DATA[0]	PDM_BIT[3]	SPDIF_OUT		USDHC3_STROBE
ENET_MDIO			SAI6_TX_SYNC	PDM_BIT[2]	SPDIF_IN		USDHC3_DATA5
ENET_TD3			SAI6_TX_BCLK	PDM_BIT[1]	SPDIF_EXT_CLK		USDHC3_DATA6
ENET_TD2			SAI6_RX_DATA[0]	PDM_BIT[3]			USDHC3_DATA7
ENET_TD1			SAI6_RX_SYNC	PDM_BIT[2]			USDHC3_CD_B
ENET_TD0			SAI6_RX_BCLK	PDM_BIT[1]			USDHC3_WP
ENET_TX_CTL			SAI6_MCLK				USDHC3_DATA0
ENET_TXC			SAI7_TX_DATA[0]				USDHC3_DATA1
ENET_RX_CTL			SAI7_TX_SYNC	PDM_BIT[3]			USDHC3_DATA2
ENET_RXC			SAI7_TX_BCLK	PDM_BIT[2]			USDHC3_DATA3
ENET_RD0			SAI7_RX_DATA[0]	PDM_BIT[1]			USDHC3_DATA4
ENET_RD1			SAI7_RX_SYNC	PDM_BIT[0]			USDHC3_RESET_B
ENET_RD2			SAI7_RX_BCLK	PDM_CLK			USDHC3_CLK
ENET_RD3			SAI7_MCLK	SPDIF_IN			USDHC3_CMD
SD1_CLK		ENET_MDC			UART1_TX		
SD1_CMD		ENET_MDIO			UART1_RX		
SD1_DATA0		ENET_RGMII_TD1			UART1_RTS_B		
SD1_DATA1		ENET_RGMII_TD0			UART1_CTS_B		
SD1_DATA2		ENET_RGMII_RD0			UART2_TX		
SD1_DATA3		ENET_RGMII_RD1			UART2_RX		
SD1_DATA4		ENET_RGMII_TX_CTL		I2C1_SCL	UART2_RTS_B		
SD1_DATA5		ENET_TX_ER		I2C1_SDA	UART2_CTS_B		
SD1_DATA6		ENET_RGMII_RX_CTL		I2C2_SCL	UART3_TX		
SD1_DATA7		ENET_RX_ER		I2C2_SDA	UART3_RX		
SD1_RESET_B		INPUT=ENET_TX_CLK OUTPUT= ENET_REF_CLK_ROOT		I2C3_SCL	UART3_RTS_B		
SD1_STROBE				I2C3_SDA	UART3_CTS_B		
SD2_CLK		SAI5_RX_SYNC	ECSPI2_SCLK	UART4_RX	SAI5_MCLK		
SD2_CMD		SAI5_RX_BCLK	ECSPI2_MOSI	UART4_TX	PDM_CLK		
SD2_DATA0		SAI5_RX_DATA[0]	I2C4_SDA	UART2_RX	PDM_BIT[0]		
SD2_DATA1		SAI5_TX_SYNC	I2C4_SCL	UART2_TX	PDM_BIT[1]		
SD2_DATA2		SAI5_TX_BCLK	ECSPI2_SS0	SPDIF_OUT	PDM_BIT[2]		
SD2_DATA3		SAI5_TX_DATA[0]	ECSPI2_MISO	SPDIF_IN	PDM_BIT[3]		
SD2_WP							CORESIGHT_EVENTI

Table 6. Different IOMUX Selections in the 8M Nano

i.MX 8M Pins	0	Alt1	Alt2	Alt3	Alt4	5	Alt6
NAND_ALE				PDM_BIT [0]	UART3_RX		CORESIGHT_TRACE_CLK
NAND_CE0_B				PDM_BIT [1]	UART3_TX		CORESIGHT_TRACE_CTL
NAND_CE1_B				PDM_BIT [0]	I2C4_SCL		CORESIGHT_TRACE[0]
NAND_CE2_B				PDM_BIT [1]	I2C4_SDA		CORESIGHT_TRACE[1]
NAND_CE3_B				PDM_BIT [2]	I2C3_SDA		CORESIGHT_TRACE[2]
NAND_CLE							CORESIGHT_TRACE[3]
NAND_DATA00				PDM_BIT [2]	UART4_RX		CORESIGHT_TRACE[4]
NAND_DATA01				PDM_BIT [3]	UART4_TX		CORESIGHT_TRACE[5]
NAND_DATA02					I2C4_SDA		CORESIGHT_TRACE[6]
NAND_DATA03							CORESIGHT_TRACE[7]
NAND_DATA04							CORESIGHT_TRACE[8]
NAND_DATA05							CORESIGHT_TRACE[9]
NAND_DATA06							CORESIGHT_TRACE[10]
NAND_DATA07							CORESIGHT_TRACE[11]
NAND_DQS				PDM_CLK	I2C3_SCL		CORESIGHT_TRACE[12]
NAND_RE_B				PDM_BIT [1]			CORESIGHT_TRACE[13]
NAND_READY_B				PDM_BIT [3]	I2C3_SCL		CORESIGHT_TRACE[14]
NAND_WE_B					I2C3_SDA		CORESIGHT_TRACE[15]
NAND_WP_B					I2C4_SDA		CORESIGHT_EVENTO
SAI5_RXFS		SAI1_TX_DATA[0]					
SAI5_RXC		SAI1_TX_DATA[1]					
SAI5_RXD0		SAI1_TX_DATA[2]					
SAI5_RXD1		SAI1_TX_DATA[3]	SAI1_TX_SYNC				
SAI5_RXD2		SAI1_TX_DATA[4]	SAI1_TX_SYNC				
SAI5_RXD3		SAI1_TX_DATA[5]	SAI1_TX_SYNC				
SAI5_MCLK		SAI1_TX_BCLK					
SAI1_XXX PINS		REMOVED	REMOVED	REMOVED	REMOVED		REMOVED
SAI2_RXFS							PDM_BIT [2]
SAI2_RXC							PDM_BIT [1]
SAI2_RXD0				SAI2_TX_DATA[1]			PDM_BIT [3]
SAI2_TXFS							PDM_BIT [2]
SAI2_TXC							PDM_BIT [1]
SAI2_MCLK							SAI3_MCLK
SAI3_RXFS					SPDIF_IN		PDM_BIT [0]
SAI3_RXC				SAI2_RX_DATA[1]			PDM_CLK
SAI3_RXD				SAI3_TX_DATA[1]			PDM_BIT [1]
SAI3_TXFS							PDM_BIT [3]
SAI3_TXC				SAI2_TX_DATA[1]			PDM_BIT [2]
SAI3_TXD					SPDIF_EXT_CLK		
SAI3_MCLK					SPDIF_OUT		SPDIF_IN
ECSP11_SCLK			I2C1_SCL	SAI5_RX_SYNC			
ECSP11_MOSI			I2C1_SDA	SAI5_RX_BCLK			
ECSP11_MISO			I2C2_SCL	SAI5_RX_DATA[0]			
ECSP11_SS0			I2C2_SDA	SAI5_RX_DATA[1]	SAI5_TX_SYNC		
ECSP12_SCLK			I2C3_SCL	SAI5_RX_DATA[2]	SAI5_TX_BCLK		
ECSP12_MOSI			I2C3_SDA	SAI5_RX_DATA[3]	SAI5_TX_DATA[0]		

Table 6. Different IOMUX Selections in the 8M Nano

i.MX 8M Pins	0	Alt1	Alt2	Alt3	Alt4	5	Alt6
ECSPI2_MISO			I2C4_SCL	SAI5_MCLK			
ECSPI2_SS0			I2C4_SDA				
I2C1_SCL				ECSPI1_SCLK			
I2C1_SDA				ECSPI1_MOSI			
I2C2_SCL				ECSPI1_MISO			
I2C2_SDA				ECSPI1_SS0			
I2C3_SCL				ECSPI2_SCLK			
I2C3_SDA				ECSPI2_MOSI			
I2C4_SCL			PCIE_CLKREQ_B	ECSPI2_MISO			
I2C4_SDA				ECSPI2_SS0			
UART1_RXD							
UART1_TXD							
UART2_RXD				GPT1_COMPARE3			
UART2_TXD				GPT1_COMPARE2			
UART3_RXD				GPT1_CAPTURE2			
UART3_TXD				GPT1_CLK			
UART4_RXD			PCIE_CLKREQ_B	GPT1_COMPARE1			
UART4_TXD				GPT1_CAPTURE1			

4.5. Power supplies

The i.MX 8M Nano has a few different power supply requirements from the i.MX 8M Mini. These changes are from two factors:

- Removal of modules with dedicated power pins
- Design improvements

Even with the power supply changes, the two devices are both design and functionally compatible.

4.5.1. Power Supply Pin differences

As shown in the Feature Comparison table, some functional modules were removed from the 8M Mini design to create the 8M Nano. Some of these removed modules had dedicated power supply pins.

Table 7 illustrates the power pins changes between the 8M Mini and 8M Nano.

Table 7. Power Pin Differences

Pin Name	8M Mini Use	8M Nano Use
VDD_PCI_1P8	PCIe	No Connect within Package
VDD_PCI_0P8	PCIe	No Connect within Package
VDD_VPU (7 pins)	VPU	No Connect within Package
NVCC_SAI1	SAI1	No Connect within Package
VDD_MIPI_0P9	MIPI PHY	VDD_MIPI_0P8 / MIPI PHY

When your design will utilize an 8M Mini device, it is the device that drives the un-used power pins states in the HW design for an 8M Nano replacement. The 8M Mini datasheet provides a table named “*Recommended connections for unused power supply rails*” which must be followed. Check the current datasheet and follow those guidelines.

- At this time, the PCIe, and VPU power pins can be either powered or a no connection.
- The NVCC_SAI1 pin must be powered.

The 8M Nano package does not connect these pins, so it is entirely based on the 8M Mini usage within the design.

4.5.2. VDD_MIPI PHY supply differences

The MIPI PHY low voltage pins was improved for the 8M Nano device. This 8M Nano feature allows the VDD_MIPI_0P8 to be grouped with the other 0.8V supply domains on the board. This voltage grouping only applies to a 8M Nano only designs.

The 8M Nano MIPI PHY voltage is backwards compatible with the 8M Mini device. The nominal voltage for the 8M Mini VDD_MIPI_0P9 pin is 0.9 V (consult datasheet). When designing for dual usage, the 8M Mini minimum voltage requirement is the defining requirement. The 8M Nano will allow the usage of the higher 0.9V voltage.

- 8M Mini and 8M Nano compatible designs must set the VDD_MIPI_0Px voltage to a nominal 0.9V. VDD_MIPI_0P8 / VDD_MIPI_0P9 is pin J14.

4.5.3. Voltage domain comparisons

The voltage requirements for each main power domain and the corresponding operating modes are highlighted the tables below. The exact voltage values are defined within each device’s datasheet.

Table 8 and Table 9 illustrate the differences in the VDD_SOC voltage domain between the 8M Mini and the 8M Nano.

Your design (or PMIC) must be able to support the unique VDD_SOC voltages between the 8M Mini and the 8M Nano if you use the Over-Drive or Super-Drive operating modes.

Table 8. 8M Mini Operational Power Requirements

Power Domain	Nominal	Over-Drive	Super Over-Drive
SOC	Standard voltage	STANDARD VOLTAGE	STANDARD VOLTAGE
DDR/VPU/GPU	Standard voltage	Over-Drive voltage	Over-Drive voltage
ARM	Standard voltage	Over-Drive voltage	Super Over-Drive voltage

Table 9. 8M Nano Operational Power Requirements

Power Domain	Nominal	Over-Drive	Super Over-Drive
SOC	Standard voltage	OVER-DRIVE VOLTAGE	OVER-DRIVE VOLTAGE
DDR/VPU/GPU	Standard voltage	Over-Drive voltage	Over-Drive voltage
ARM	Standard voltage	Over-Drive voltage	Super Over-Drive voltage

4.5.4. Re-use of power and decoupling capacitors

As discussed above, some of the power supply rails are not supported within the 8M Nano device. Since the 8M Mini and 8M Nano are pin compatible, this implies these un-used power supply rails would have power and decoupling capacitors associated with them on the 8M Mini. It is recommended to leave the capacitors in place for the 8M Nano design. When the supplies are combined as in Option 1 and Option 2, these capacitors will aid the 8M Nano supplies. For example, the capacitors associated with the VDD_VPU pins could be attached to the VDD_SOC power plane.

The 8M Nano should utilize all capacitor areas and move “free” capacitors to heavier current usage domains.

4.6. PMIC part number

The 8M Nano simplifies the power supply structure. For all the integrated analog modules, MIPI PHY and USB PHY, their 1.8 V and 0.8/0.9 V power will be supplied externally through power pads. The power supplies are separated with other power pads on the package to keep them clean, but they can be shared with other power rails on the board to reduce the number of power supplies from the PMIC. The VDD_GPU/VDD_DRAM can also be combined with the VDD_SOC to save one voltage rail. So there is a new PMIC to support this requirement for less power supplies.

The new PMIC BD71850MWV is changed from BD71847AMWV to default turn off some voltage regulators by new OTP. [Table 10](#) illustrates the voltage regulators ON/OFF between these two PMICs.

Table 10. PMIC differences

	8M Mini Use	8M Nano Use
Voltage Regulators	ROHM BD71847AMWV	ROHM BD71850MWV
BUCK1	ON	ON
BUCK2	ON	ON
BUCK5	ON	OFF
BUCK6	ON	ON
BUCK7	ON	ON
BUCK8	ON	ON
LDO1	ON	ON
LDO2	ON	ON
LDO3	ON	ON
LDO4	ON	OFF
LDO5	OFF	OFF
LDO6	ON	ON
MUXSW	ON	ON

If your design must be able to support the unique VDD_SOC, you should use BD71847AMWV. Otherwise the BD71850MWV is the better one to reduce the power supplies.

CAUTION

If the voltage regulators of PMIC are turned off by OTP, their output components can be removed. Other output components from the voltage regulators that are default turned on can't be removed even though they

aren't used. If the components are removed, the VR fault would be detected and PMIC would shut down.

4.7. On-Die GPIO resistors

NOTE

Datasheet and Errata documents define the IC specifications and operation. Always check the most current documents.

Both the 8M Mini and 8M Nano contain on-die resistors at each GPIO pad. These are selectively enabled or disabled by SW. At the time of this document generation, an erratum to the 8M Mini has been announced. This erratum describes a design error such that it is recommended not to use the on-die resistors of the 8M Mini with 3.3V IO lines. It is recommended to use PCB resistors and disable the on-die resistors.

This design issue has been corrected within the 8M Nano silicon. The on-die resistors should function properly on the 8M Nano device.

This design errata only applies to 3.3V IO signals. The 1.8V signals are not affected and can use the on-die resistors on both the 8M MINI and 8M NANO.

For design compatibility use the following recommendations:

- Check the current 8M Mini errata to determine if this design error has been corrected.
- If not corrected, then you will need to implement resistor pull-up or pull-downs on your PCB for 3.3V IO lines.

This ensures proper system operation and compatibility with both 8M Mini and 8M Nano.

As a BOM cost reduction path, you may remove the 3.3 V resistors when an 8M Nano is installed in the design. If the resistors are removed, then the 8M Nano software will need to enable the on-die resistors. You may opt to maintain SW compatibility across both 8M devices and leave the PCB resistors installed.

4.8. Enter Boundary-Scan mode

Boundary-scan is an electronic serial interface that allows access to the special embedded logic on the ICs. It involves the inclusion of a shift-register stage adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles.

Boundary scan description language (BSDL) is used for board-level testing after components have been assembled. The interface for this test uses the JTAG pins. The definition is contained within IEEE Std 1149.x.

When doing boundary-scan operation, the compliance patterns or special entry sequence are used to force the board to enter boundary-scan mode.

The 8M Mini can follow below CPMLIANCE_PATTERNS mentioned in the BSDL file to enter boundary-scan mode.

attribute COMPLIANCE_PATTERNS of IMX8MM: entity is

```
"(BOOT_MODE0, BOOT_MODE1, JTAG_MOD, TEST_MODE) (1101)";
```

- BOOT_MODE0(G26)&BOOT_MODE1(G27)&TEST_MODE(D26) should be high
- JTAG_MOD should low.

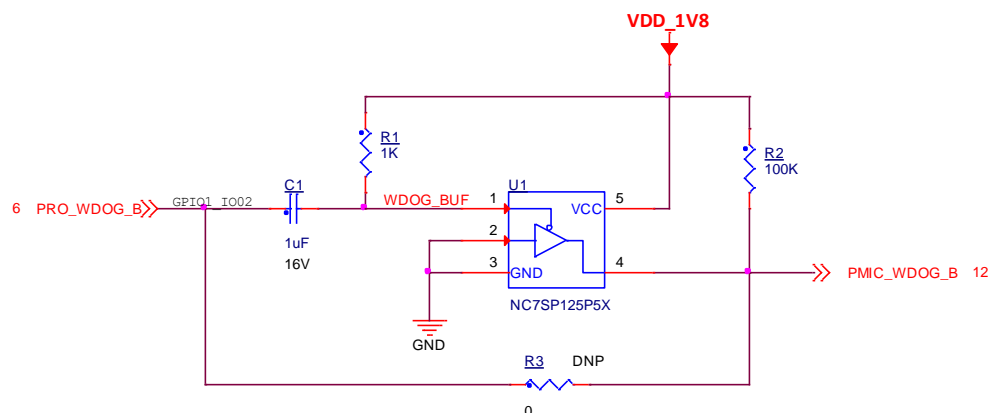
As above mentioned, the 8M Nano device re-purposed the TEST_MODE pin of 8M Mini to BOOT_MODE3, so the requirement of 8M Nano to enter boundary-scan mode is different to 8M Mini. The 8M Nano doesn't have the COMPLIANCE_PATTERNS, it needs a special setup sequence to enter boundary-scan mode as below. This is not completely compliant with IEEE 1149.x.

- BOOT_MODE0(G26)&BOOT_MODE1(G27)& BOOT_MODE2(C27)& BOOT_MODE3(D26) should be high, then power up the board.
- Load the instruction and data codes to the chip TAP controller by JTAG port to enter boundary-scan mode.
 - a) Soft reset the JTAG TAP controller, go to Test-Logic Reset state
 - b) Go to Shift-IR state, load IR Instruction = b10000
 - c) Go to RUN-TEST-IDLE state
 - d) Go to Shift-DR state, load DR data = b00111000
 - e) Go to RUN-TEST-IDLE state
 - f) End task.

For 8M Mini to 8M Nano design conversions, the JTAG_TRST_B/TEST_MODE pin should be connected with pull-up and pull down resistors for entering boundary scan mode with the 8M Mini or Boot Mode selection when prototyping with the 8M Nano device.

CAUTION

GPIO1_IO02 is used as WDOG_B to control the PMIC. When entering boundary-scan mode, this pin is floating on 8M Mini, but always output low on 8M Nano. It will cause the system repeatedly reboot due to WDOG cold reset. The designer can add an external 100K ohm pull up resistor for 8M Mini. But if plan to design for 8M Mini and 8M Nano compatibility, please use below Watch Dog Buffer circuit.



If the boundary-scan test is not required or the PMIC default disable the WDOG_B reset, GPIO1_IO02(WDOG_B, ball AG13) can be connected to external PMIC directly without this circuit.

4.9. JTAG_TMS recommendation

The JTAG_TMS pin must be connected with a 50ohm serial resistor near the component or floating if not used for 8M Nano, please refer to the datasheet for more detail. When designing for dual usage, the 8M Mini also must add a 50 ohm serial resistor or floating for compatible.

5. Package and Ballmap

Table 11. 8M Nano Ballmap – Unused Pins Locations

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
A																			PCIE_RXN_N	PCIE_TXN_N	PCIE_CLK_N		USB2_DN				
B																			PCIE_RXN_P	PCIE_TXN_P	PCIE_CLK_P		USB2_DP				
C																											C27
D																			PCIE_RESREF				USB2_ID				D26
E																							USB2_TXRTUNE				
F																							USB2_VBUS				
G														VDD_PCI_IP8													
H																											
J														J14		VDD_PCI_OP8											
K											VDD_VPU	VDD_VPU															
L											VDD_VPU	VDD_VPU															
M											VDD_VPU	VDD_VPU															
N											VDD_VPU																
P																											
R																											
T																											
U																											
V	DRAM_DQ21	DRAM_DQ20																									
W	DRAM_DQ18	DRAM_DQ19																NVCC_SAI1									
Y	DRAM_DQS2_N																										
AA	DRAM_DQS2_P	DRAM_DQ17																									
AB	DRAM_DM2	DRAM_DQ16																SAI1_MCLK	SAI1_TXFS								
AC	DRAM_DQ22	DRAM_DQ23																SAI1_TXC									
AD	DRAM_DQ27	DRAM_DQ26																									
AE	DRAM_DQ28																										
AF	DRAM_DQ29	DRAM_DQS3_N	DRAM_DQ31	DRAM_DQ25										SAI1_RXD1	SAI1_RXC	SAI1_RXD3	SAI1_RXD5	SAI1_RXD7	SAI1_TXD1	SAI1_TXD3	SAI1_TXD5	SAI1_TXD7					
AG	DRAM_DQS3_P	DRAM_DQ30	DRAM_DM3	DRAM_DQ24										SAI1_RXD0	SAI1_RXFS	SAI1_RXD2	SAI1_RXD4	SAI1_RXD6	SAI1_TXD0	SAI1_TXD2	SAI1_TXD4	SAI1_TXD6					

- The pin names above are 8M Mini functions that were removed on the 8M Nano. These pins exist as “NC_xx” names on the 8M Nano package.
- The pin locations marked in “Orange” are described in [Table 12](#).

Table 12. Pin Functional Change List on the 8M Nano

BGA Pin #	8M Mini Function	8M Nano Function	Comments
C27	JTAG_TRST_B	BOOT_MODE2	Refer to 4.3 Boot Mode controls
D26	TEST_MODE	BOOT_MODE3	Refer to 4.3 Boot Mode controls
J14	VDD_MIPI_OP9	VDD_MIPI_OP8	Voltage Change

5.1. 8M Nano unused pin list

The table below lists 8M Nano pins which are Not Connected (“NC”). These pins on the 8M Nano package are only connected to the solder ball for mechanical stability. The “NC_xx” pins on the 8M Nano can float or be tied to power since they are not used with the 8M Nano package. [Table 13](#) provides a column for common usage for both 8M Mini to 8M Nano.

- **NVCC_SAI1 must be tied to power on the 8M MINI even if the signals are not used. The 8M Nano does not use this power pin.**

Table 13. Full Unused Pin List for 8M Nano

8M Mini Pin Name	BGA Pin #	8M Module Assignment	Mini to Nano PCB Connection
PCIE_RXN_N	A19	PCle	Unconnected
PCIE_TXN_N	A20	PCle	Unconnected
PCIE_CLK_N	A21	PCle	Unconnected
PCIE_RXN_P	B19	PCle	Unconnected
PCIE_TXN_P	B20	PCle	Unconnected
PCIE_CLK_P	B21	PCle	Unconnected
PCIE_RESREF	D19	PCle	Unconnected
VDD_PCI_1P8	G14	PCle	Unconnected
VDD_PCI_0P8	J16	PCle	Unconnected
USB2_DN	A23	USB2	Unconnected
USB2_DP	B23	USB2	Unconnected
USB2_ID	D23	USB2	Unconnected
USB2_TXRTUNE	E22	USB2	Unconnected
USB2_VBUS	F23	USB2	Unconnected
VDD_VPU	K12	VPU	Unconnected
VDD_VPU	K13	VPU	Unconnected
VDD_VPU	L11	VPU	Unconnected
VDD_VPU	L13	VPU	Unconnected
VDD_VPU	M13	VPU	Unconnected
VDD_VPU	M14	VPU	Unconnected
VDD_VPU	N11	VPU	Unconnected
DRAM_DQ21	V1	DRAM	Unconnected
DRAM_DQ20	V2	DRAM	Unconnected
DRAM_DQ18	W1	DRAM	Unconnected
DRAM_DQ19	W2	DRAM	Unconnected
DRAM_DQS2_N	Y1	DRAM	Unconnected
DRAM_DQS2_P	AA1	DRAM	Unconnected
DRAM_DQ17	AA2	DRAM	Unconnected
DRAM_DM2	AB1	DRAM	Unconnected
DRAM_DQ16	AB2	DRAM	Unconnected
DRAM_DQ22	AC1	DRAM	Unconnected
DRAM_DQ23	AC2	DRAM	Unconnected
DRAM_DQ27	AD1	DRAM	Unconnected
DRAM_DQ26	AD2	DRAM	Unconnected
DRAM_DQ28	AE1	DRAM	Unconnected
DRAM_DQ29	AF1	DRAM	Unconnected
DRAM_DQS3_N	AF2	DRAM	Unconnected
DRAM_DQ31	AF4	DRAM	Unconnected
DRAM_DQ25	AF5	DRAM	Unconnected
DRAM_DQS3_P	AG2	DRAM	Unconnected

Table 13. Full Unused Pin List for 8M Nano

8M Mini Pin Name	BGA Pin #	8M Module Assignment	Mini to Nano PCB Connection
DRAM_DQ30	AG3	DRAM	Unconnected
DRAM_DM3	AG4	DRAM	Unconnected
DRAM_DQ24	AG5	DRAM	Unconnected
NVCC_SAI1	W18	SAI1	Connect to PWR
SAI1_MCLK	AB18	SAI1	Unconnected
SAI1_TXFS	AB19	SAI1	Unconnected
SAI1_TXC	AC18	SAI1	Unconnected
SAI1_RXD1	AF15	SAI1	Unconnected
SAI1_RXC	AF16	SAI1	Unconnected
SAI1_RXD3	AF17	SAI1	Unconnected
SAI1_RXD5	AF18	SAI1	Unconnected
SAI1_RXD7	AF19	SAI1	Unconnected
SAI1_TXD1	AF20	SAI1	Unconnected
SAI1_TXD3	AF21	SAI1	Unconnected
SAI1_TXD5	AF22	SAI1	Unconnected
SAI1_TXD7	AF23	SAI1	Unconnected
SAI1_RXD0	AG15	SAI1	Unconnected
SAI1_RXFS	AG16	SAI1	Unconnected
SAI1_RXD2	AG17	SAI1	Unconnected
SAI1_RXD4	AG18	SAI1	Unconnected
SAI1_RXD6	AG19	SAI1	Unconnected
SAI1_TXD0	AG20	SAI1	Unconnected
SAI1_TXD2	AG21	SAI1	Unconnected
SAI1_TXD4	AG22	SAI1	Unconnected
SAI1_TXD6	AG23	SAI1	Unconnected

6. References

Following documents may offer further reference:

- i.MX 8M Mini Applications Processor Datasheet for Consumer Products: IMX8MMCEC
- i.MX 8M Nano Applications Processor Data Sheet for Consumer Products: IMX8MNCEC
- i.MX 8M Mini Applications Processor Reference Manual: IMX8MMRM
- i.MX 8M Nano Applications Processor Reference Manual: IMX8MNRM
- i.MX 8M Mini Hardware Developer's Guide: IMX8MMHDG
- i.MX 8M Nano Hardware Developer's Guide: IMX8MNHDG
- i.MX 8M Mini EVK schematics and layout files
- i.MX 8M Nano EVK schematics and layout files

7. Revision history

The table below provides a revision history for this document.

Table 14. **Revision history**

Rev.	Date	Substantive change(s)
Rev 0	12/2019	Initial Release

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