AN13638

NXP PMIC Solution for TI TDA2x_TDA2Ex Processor

Rev. 1 — 2 August 2022   **Application note**

Document information

Information	Content
Keywords	Power solution, BYLink,TDA2x, TDA2Ex, DRA7x, FS56, PF81/82
Abstract	This application note explains how to use NXP power management integrated circuit (PMIC) FS56 and PF81/82 to power the TI TDA2/TDA2Ex processor systems.

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AN13638

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Application note

Rev. 1 — 2 August 2022

2 / 17

1   Introduction

The BYLink System Power Platform is a safe, scalable, and expandable solution based on NXP automotive power management integrated circuit (PMIC) devices working together as a single-power solution. This is a simple way to enable complex applications. By using the NXP BYLink System Power Platform, NXP provides customers with a scalable power solution for TDA2x/TDA2Ex systems.

This application note shows the power solution using NXP PMIC FS56, PF81/82 to power TI TDA2x/TDA2Ex devices. Users will learn how to use NXP PMICs to accomplish the power solution design, including power rail configuration, system features, and typical schematic. This application note also provides a general description of the interconnection between NXP PMIC and TDA2x/TDA2Ex.

This power solution is also suitable for TI DRA72x, DRA74x, or DRA75x devices.

2   TDA2x/TDA2Ex and NXP PMIC overview

TI's TDA2x/TDA2Ex system-on-chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS). The TDA2x family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power, and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.
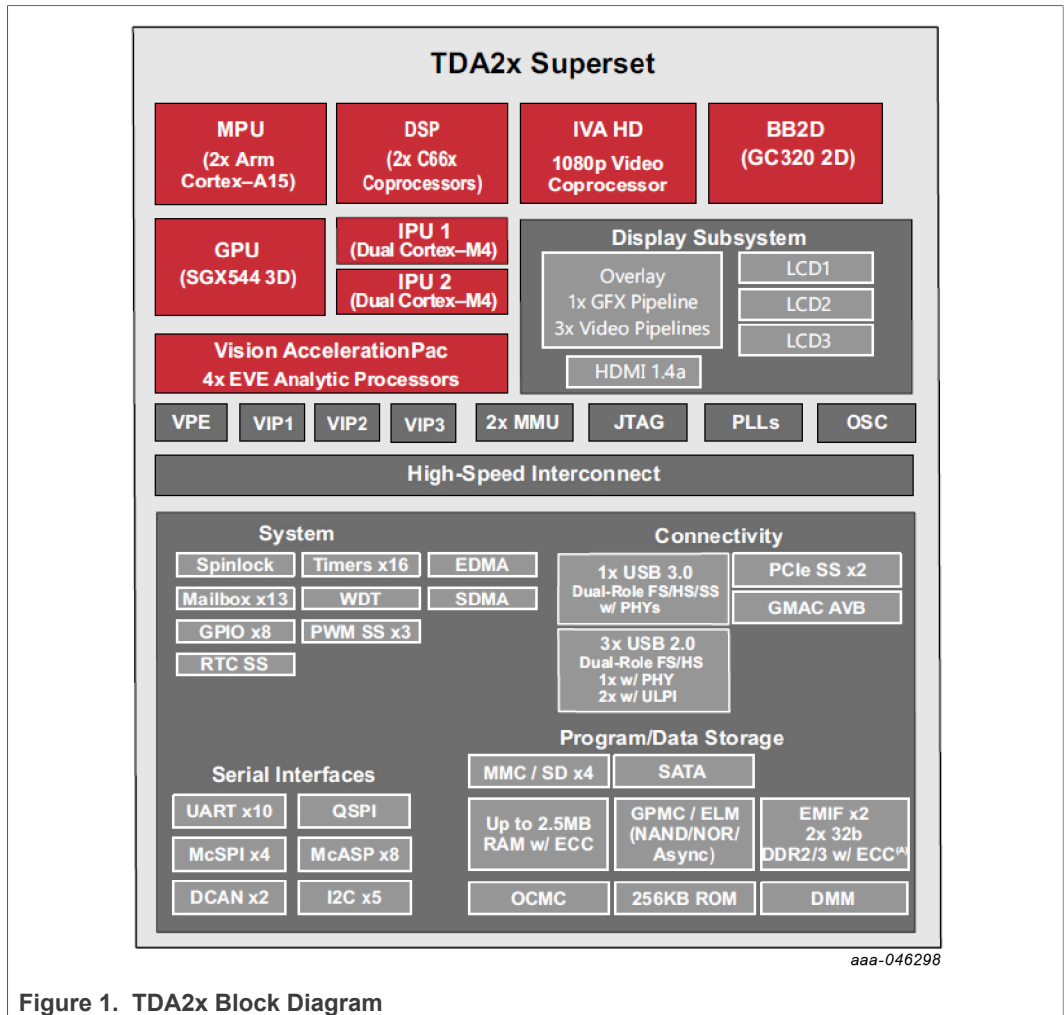
Figure 1. TDA2x Block Diagram

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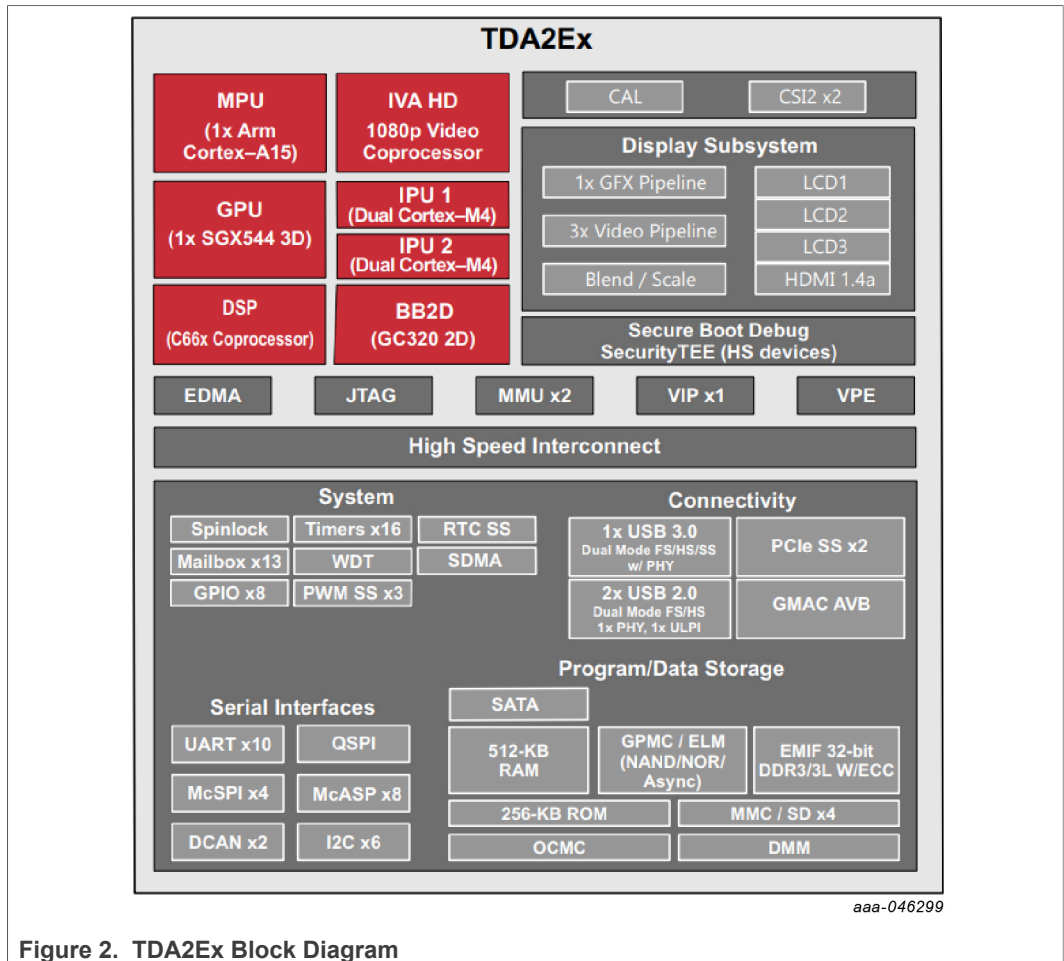**Application note**

Rev. 1 — 2 August 2022

4 / 17

Figure 2. TDA2Ex Block Diagram

NXP provides the BYLink System Power Platform, which includes HVPMICs (high-voltage PMIC) and LVPMICs (low-voltage PMIC).

PF81/82 devices are high-integration PMICs designed for high-performance processor-based system, and they belong to LVPMIC of NXP BYLink Power Concept. LVPMIC have similar design structure and can be used to work together in system by logic connection and power companion. Figure 3 shows the block diagram for PF81/82 family device.

AN13638

Application note

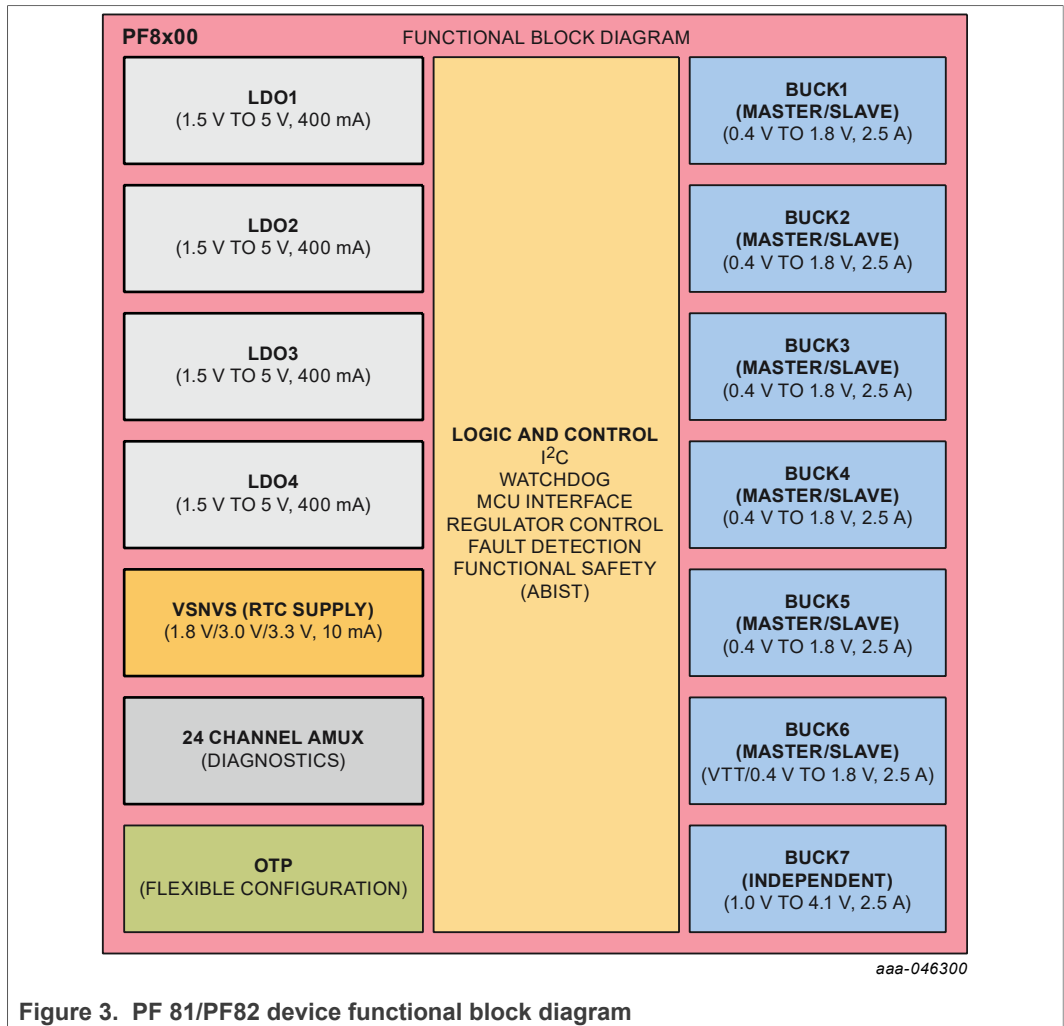**Rev. 1 — 2 August 2022**

5 / 17

Figure 3. PF 81/PF82 device functional block diagram

For automotive application, HV PMICs which can be powered directly by 12 V battery are also necessary in customer system. NXP provides a complete portfolio of PMICs with embedded system features. FS84/85, FS56 series HV PMICs can be chosen as front-power devices. In this application note, FS56 with two HV BUCK was chosen as the pre-buck of TDA2x/TDA2E2x power solution. Figure 4 shows the block diagram for FS56 family device.
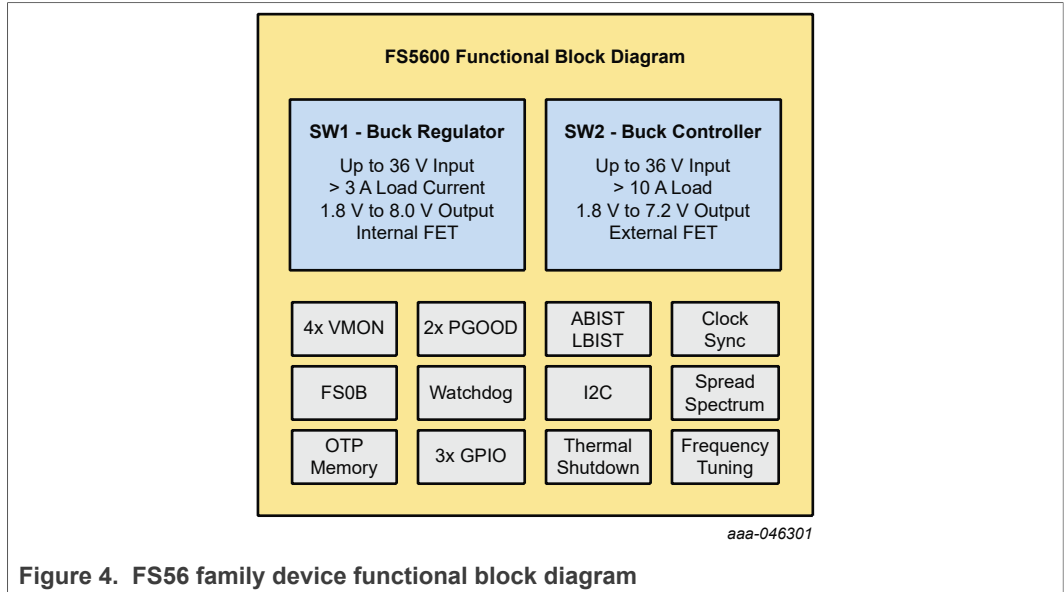
Figure 4. FS56 family device functional block diagram

3 TDA2x/TDA2Ex power solution introduction

To implement the NXP power solution for TDA2x/TDA2Ex, high-voltage PMIC FS56 work with low-voltage PMIC PF81/82 solution is suitable for TDA2x/TDA2Ex total system in automotive application. Figure 5 shows the TI TDA2x/TDA2Ex system power solution block diagram.
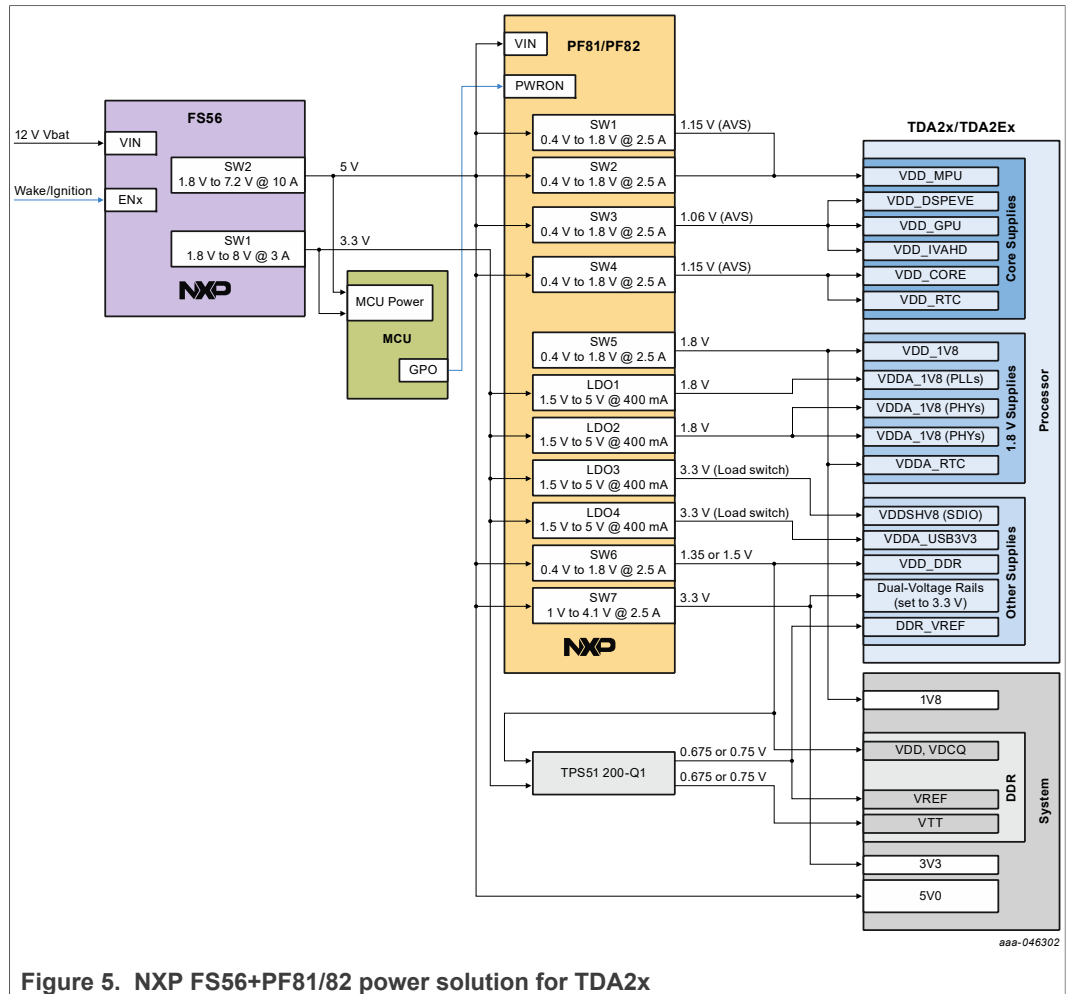
Figure 5. NXP FS56+PF81/82 power solution for TDA2x

The FS5600 integrates a battery connected DC-DC controller with external FETs and a battery connected DC-DC converter with internal FETs. The FS56 has the ability to provide the input of PF-PMICs and other peripherals power. The current capability of FS56 SW2 can achieve 10 A with a voltage range of 1.8 V - 7.2 V. SW1 can provide 1.8 V - 8.0 V/3 A high-efficiency power for processors or peripherals.

PF81/82 includes seven high-efficiency bucks and four low dropouts (LDOs) for powering the processor, memory, and miscellaneous peripherals. Each buck has a 2.5 A stable current capability and can work in multiphase to supply up to a 10 A current. Each LDO can output a 400 mA current with low drop-out voltage. Each LDO can be used as load switch.

In this solution, the 5 V/10 A output from FS56 BUCK2 is used as the input of PF81/82 BUCKx regulators. The 3.3 V/3 A output from the FS56 BUCK1 is used as the input of the PF81/82 LDOx regulators, which can reduce the power consumption and improve the efficiency. LDO3 and LDO4 are used in switch mode to output 3.3 V.

4   Power up and power down sequence

This application note shows a typical NXP PMIC design for a TDA2x/TDA2Ex device system. Table 1 shows the design parameters of the F56+PF81/82 attach TDA2xTDA2Ex

AN13638

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Application note

Rev. 1 — 2 August 2022

8 / 17

solution, including detailed PMIC power tree configurations, power-up sequences, and current capability of each power rail.

Table 1. The design parameters of the PF8200+PF5024 attach J3 solution

Item	Power config	Voltage (V)	Max load (A)	System power rail	Power-up delay
1	PF81/82 SW1-2	1.15	5	VDD_MPU	2.5ms-slot5
2	PF81/82 SW3	1.06V	2.5	VDD_DSPEVE VDD_GPU VDD_IVAHD	2.0ms-slor4
3	PF81/82 SW4	1.15	2.5	VDD_CORE VDD_RTC	3.0ms-slot6
4	PF81/82 SW5	1.8	2.5	VDD_1V8 VDDA_RTC SYS_1V8	0.5ms-slot1
5	PF81/82 SW6	1.35 or 1.5	2.5	VDD_DDR VDDQ_DDR	1.5ms-slor3
6	PF81/82 SW7	3.3	2.5	Dual-Voltage Rails(3.3V) SYS_3V3	4.0ms-slot8
7	PF81/82 LDO1	1.8	0.4	VDDA_1V8(PLLs)	1ms-slot2
8	PF81/82 LDO2	1.8	0.4	VDDA_1V8(PHYs)	3.5ms-slot7
9	PF81/82 LDO3	3.3	0.4	VDDSHV8()SDIO	6.5ms-slo13
10	PF81/82 LDO4	3.3	0.4	VDDA_USB3V3	7ms-slot14
11	nRESET	-	-	RESETBMCU	7.5ms-slot15

NXP PMICs feature a built-in, one time programmable (OTP) memory that stores key startup configurations. Users define the OTP configuration based on their specific application requirements. The default sequence slot for PMICs are programmed via the OTP configuration registers. The sequence slot includes time base and time slot to realize flexible power-up\power-down sequence configuration. There are 255 sequence time slots for each regulator. PGOOD and RESETMCU can be set from 0 to 254. Time base has four options: 30 µs, 120 µs, 250 µs and 500 µs. The LV PMICs feature a dedicated functional block for synchronizing power-up sequences from multiple PMICs. XFAILB is a bidirectional pin with an open drain output used to synchronize the power-up and power-down sequences of multiple LV PMICs.

Figure 6 and Figure 7 show the TDA2x/TDA2Ex power-up and power-down sequence.

AN13638
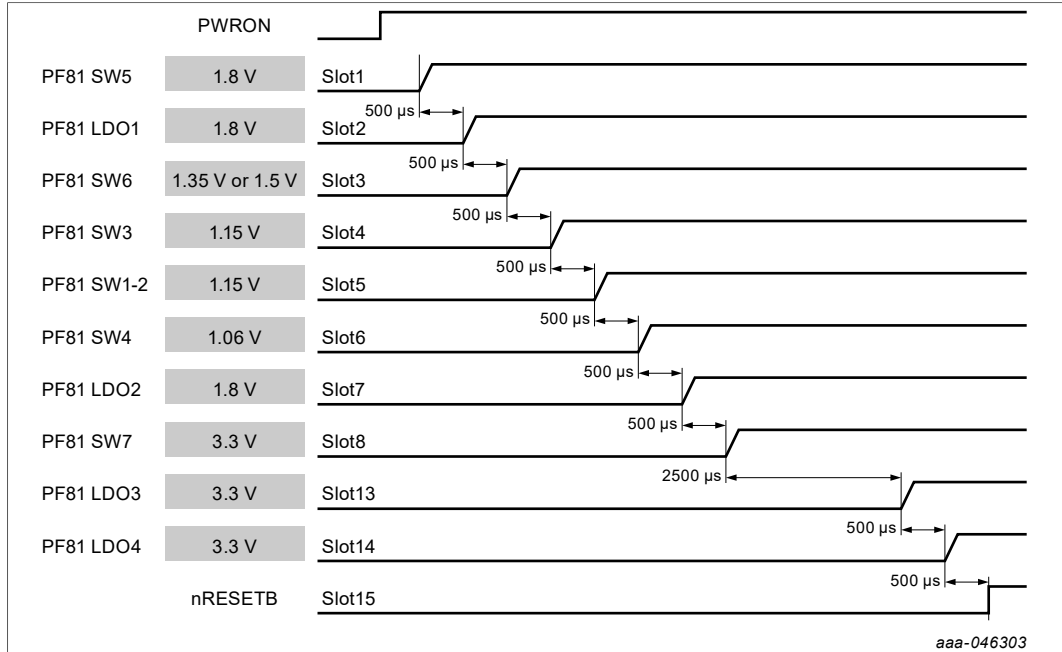
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Rev. 1 — 2 August 2022

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9 / 17

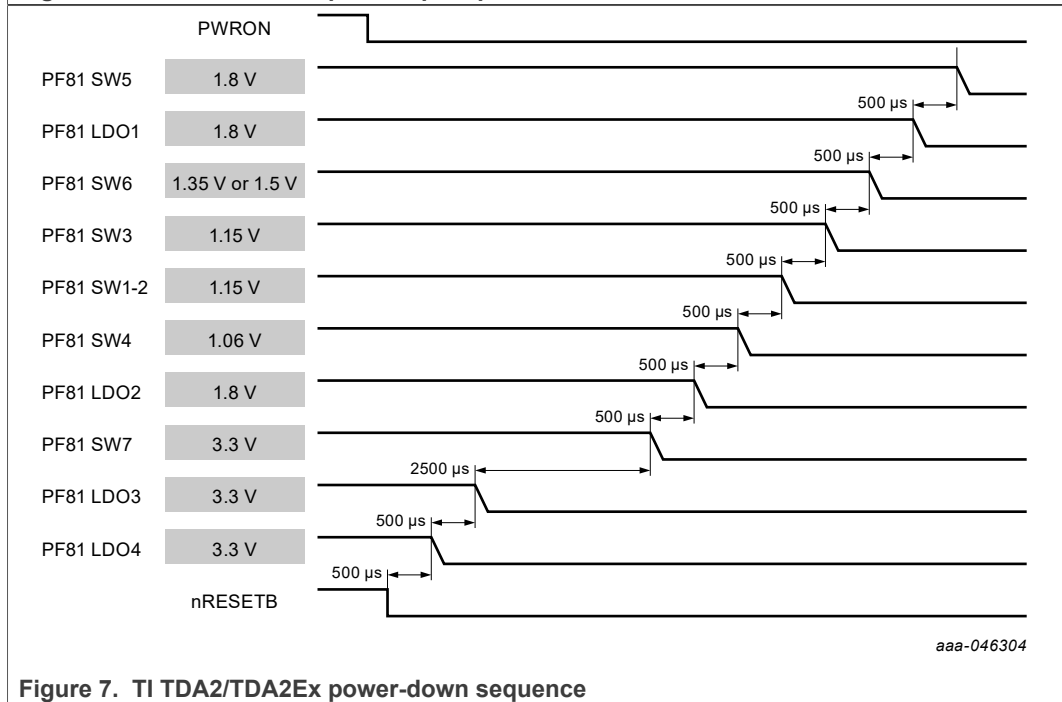**Figure 6. TI TDA2/TDA2Ex power-up sequence**

Figure 7. TI TDA2/TDA2Ex power-down sequence

ENs of FS56 can be connected with an ignition signal or the CAN PHY wake-up signal. FS56 output should be power up first and power down last in this system. PWRON of PF81/82 can be controlled by the MCU of the system. One typical use for the TDA2x/TDA2Ex automotive system is shown in Figure 5. If input voltage for PF81/82 is ready, the device will start up when PWRON is pulled high. The power rails of PF81/82 will follow the power up sequence as defined in OTP. RESETBMCU which is connected with TDA2x/TDA2Ex processor reset pin will be released at the end of the power sequence if all the power rails of PMIC turn on with no fault. Then TDA2x/TDA2Ex system will continue to operate other boot up actions. PF81/82 will start power down in reverse order

as defined in OTP when PWRON pulled low. The customer doesn't need to do additional design on the hardware or software, and the power-up and power-down sequences will be achieved automatically if correct version OTP device is used.

5 Optional safety features

FS56, PF81/82 devices feature embedded safety mechanism. These PMICs meet ISO 26262 standards and up to ASIL B functional safety level. The safety mechanism includes the following functional safety features:

- **Independent voltage monitoring and fault detection:** The PMICs feature independent fault monitoring functions for each regulator. UV, OV, and ILIM are three types of faults monitored by the PMIC fault monitor block. The PMIC can indicate the output state of each regulator through PGOOD signal.

- **Watchdog monitoring and internal watchdog counter:** PF81/82 feature internal watchdog counters for monitoring watchdog events that happen in the processor. If the PMIC internal watchdog expiration counter reaches the maximum value, a reset event is performed by the PMIC. The watchdog can be disabled if it is not needed.

- **I^{2}C CRC and write protection:** The fuses are loaded into the functional I^{2}C registers of the PMIC. The fuse circuits have a CRC error check routine that reports and protects against register loading errors on the PMIC registers. If a register loading error is detected, the corresponding flag is asserted. The I^{2}C secure write protects the secure registers from wrong operations.

- **Functional safety output:** When a fault is detected by the PMIC, such as an incorrect regulator output or WD failure, the PMIC can reset the TDA2x/TDA2Ex processor through the RESETBMCU pin. The PMIC can trigger the FSOB pin to put the system into safe state.

- **Analog built-in self-test (ABIST):** When the power system is turned on, the PMIC routinely implements an ABIST process of all output voltage monitors before starting power-up sequence. ABIST checks whether the state of each regulators' voltage monitoring block (OV/UV) is normal. If a failure on the OV/UV monitor is detected during the ABIST on-demand request, the PMIC will assert the corresponding ABIST flags.
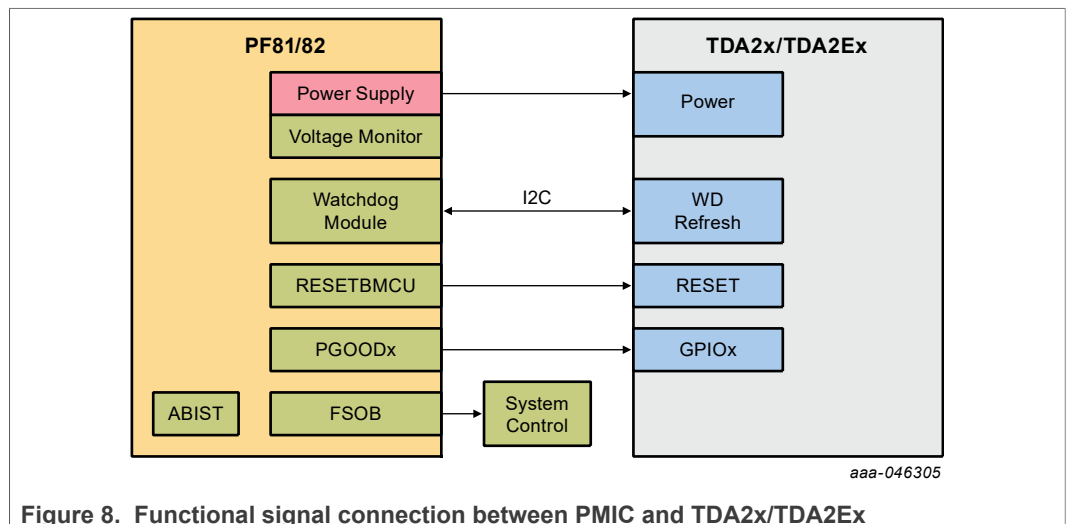

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Figure 8. Functional signal connection between PMIC and TDA2x/TDA2Ex

Figure 8 shows the recommended functional signal connections between the PMIC and TDA2x/TDA2Ex processor.

AN13638

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Application note

Rev. 1 — 2 August 2022

11 / 17

If the application does not need these PMIC safety features, NXP provides QM PMIC parts, which are pin-to-pin compatible with the ASIL B parts. The QM versions of the PMICs are low-cost devices with basic regulator OV/UV/OC fault monitoring features. Refer to the F56 and PF81/82 data sheets for details about the functional differences between QM and ASIL B devices.

6   Schematic

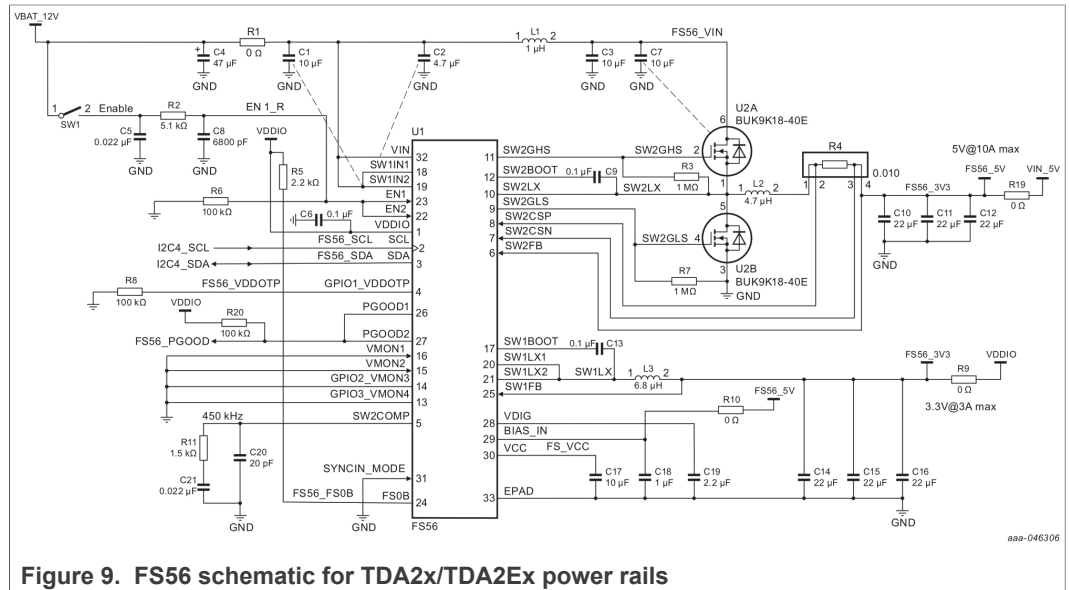Figure 9 and Figure 10 show the TDA2x/TDA2Ex power solution schematic based on NXP PMICs FS56 and PF81.

Figure 9. FS56 schematic for TDA2x/TDA2Ex power rails
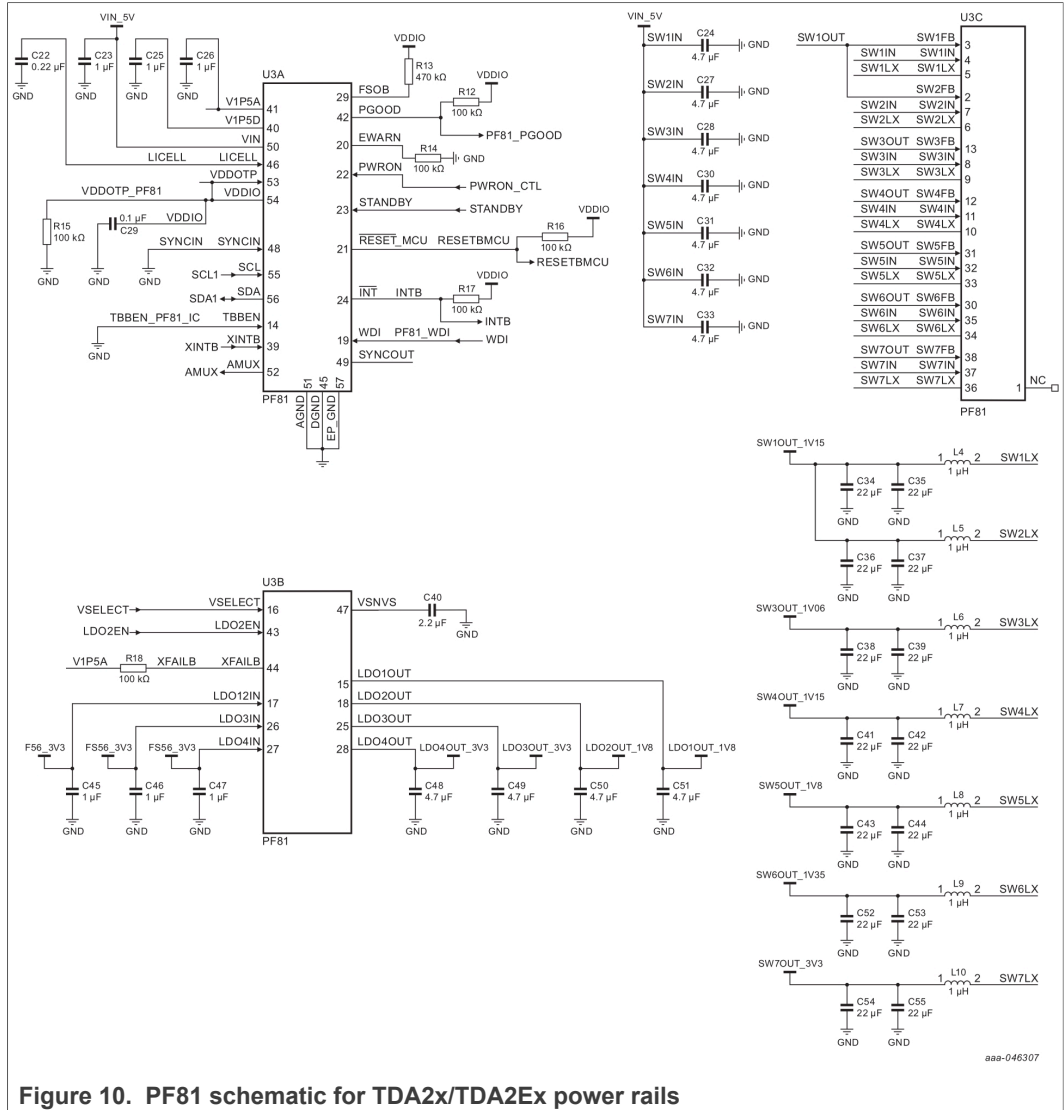
Figure 10. PF81 schematic for TDA2x/TDA2Ex power rails

7   References

[1]   PF81/82 — information and tools can be found in link: https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/12-channel-power-management-integrated-circuit-pmic-for-high-performance-processing-applications:PF8100-PF8200

[2]   FS56 — information can be found in the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/automotive-dual-buck-regulator-and-controller-with-voltage-monitors-and-watchdog-timer:FS5600

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Figures

Contents