AN14002

RW61x Design Guide

Rev. 2.0 — 1 November 2024 Application note

Document information

Information	Content
Keywords	Power supply, clock source, reset, host interface, RF interface, PCB layout, PCB stack-up, reference design, evaluation board (EVB)
Abstract	Provides design guidelines for RW61x.

1 Overview

This document provides design guidelines for the RW61x device. The RW61x is a highly integrated, low-power tri-radio Wireless MCU with an integrated MCU and Wi-Fi 6 + Bluetooth Low Energy (LE)/802.15.4 radios. RW61x is designed for a broad array of applications, such as smart home devices, enterprise, and accessories. The RW61x is available in three package options – TFBGA, HVQFN, and WLCSP.

NXP reference designs provide examples to design a PCB using the RW61x device. Follow these design guidelines closely.

To discuss design options and schedule a design review, contact your NXP representative.

Note: *In the following sections, the RW61x is also referred to as "Wireless SoC".*

Figure 1 shows RW610 block diagram for the dual antenna configuration.

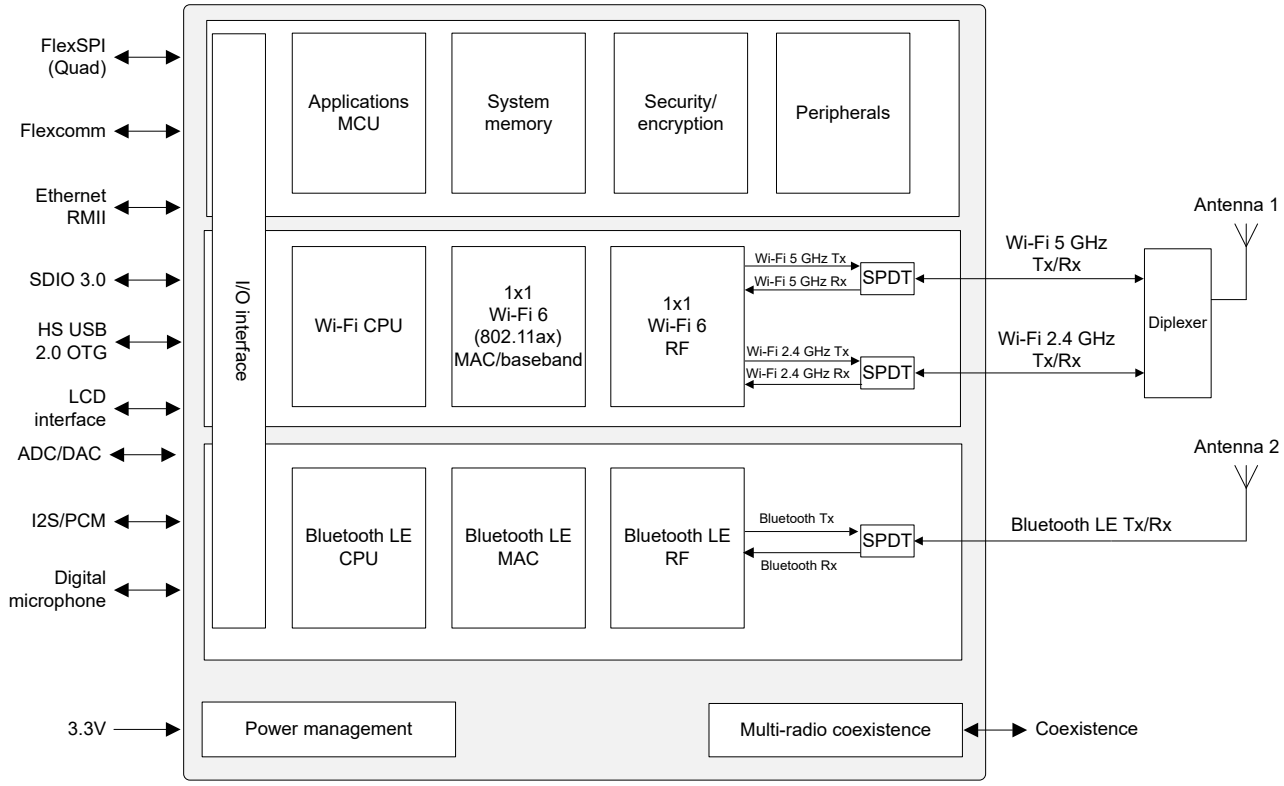

Figure 1. RW610 block diagram - Dual antenna configuration

Figure 2 shows RW612 block diagram for the dual antenna configuration.

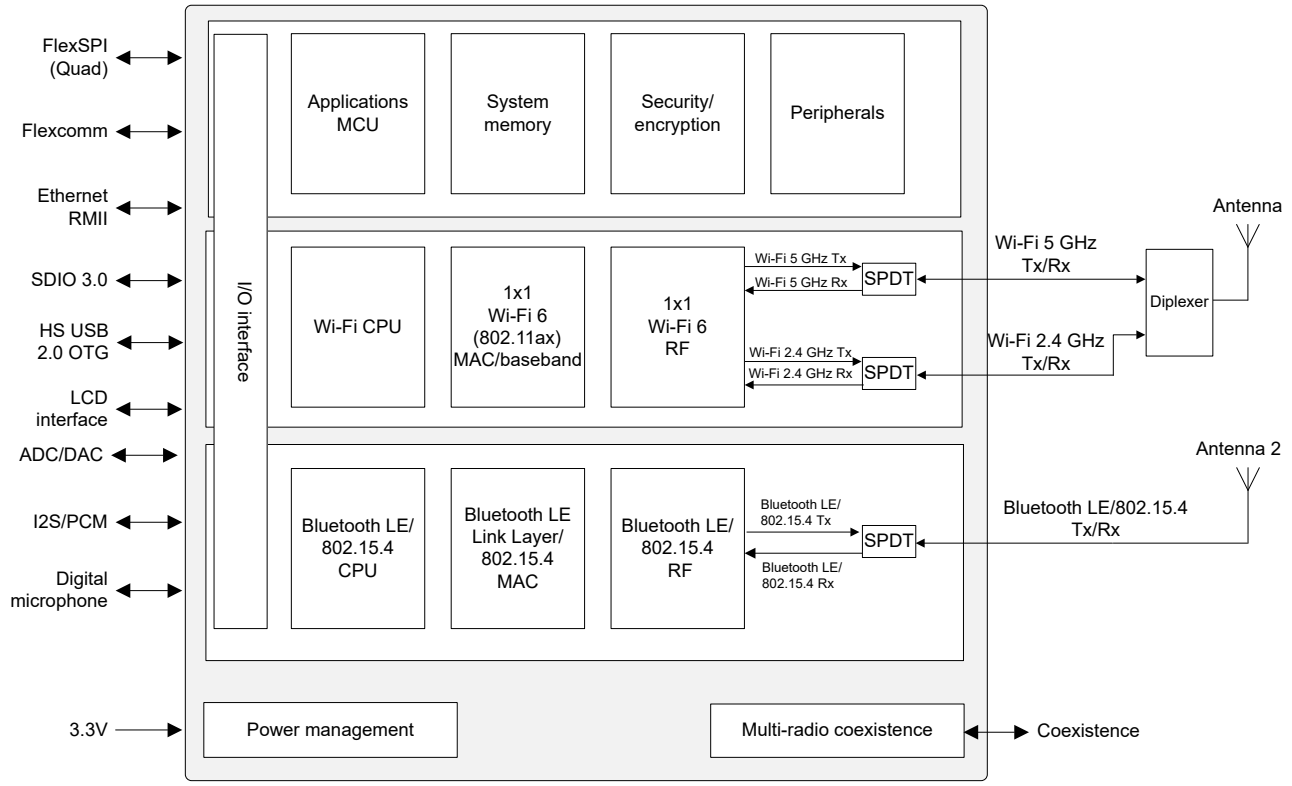

Figure 2. RW612 block diagram - Dual antenna configuration

2 Power supply

2.1 Overview

Table 1 lists RW61x power supply pins and respective voltage values.

Table 1. Power supply pins

Supply	Description	Typical value (V)
VCORE	Core power supply	1.05
VIO, VIO_SD	Digital I/O power supply	1.8 or 3.3
VIO_RF	Digital I/O RF power supply	1.8 or 3.3
AVDD18	Analog power supply	1.8
AVDD33_USB	Analog power supply for USB	3.3
VPA	Analog power supply	3.3
VBAT	Input power supply to internal buck regulators	3.3

2.2 Topology

RW61x requires an external 3.3 V DC power supply. The 3.3 V DC powers VBAT and VPA. Two internal buck regulators are used to power VCORE and AVDD18. For details, refer to RW61x data sheets [1] and [2], and to the reference design.

Figure 3 shows a simplified diagram of the RW61x power supply.

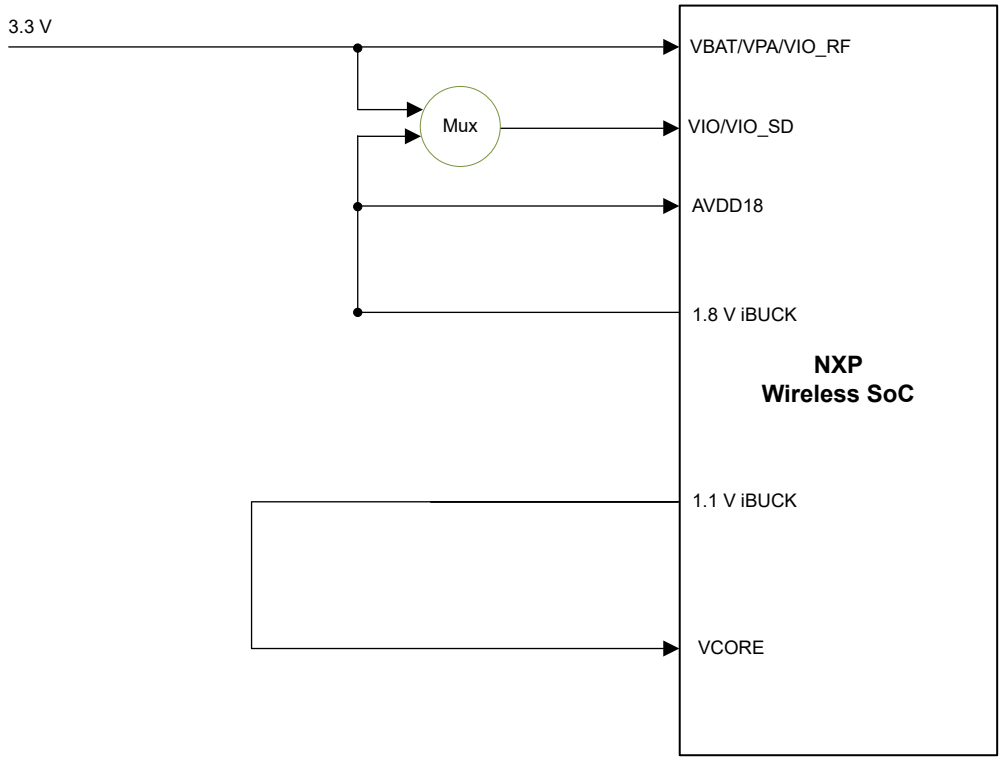

Figure 3. RW61x power supply

2.3 VBAT

VBAT is the power supply to the internal buck regulators. Decoupling capacitors are required for the VBAT supply pin. The capacitor values are 0.1 µF and 22 µF. The 0.1 µF capacitors must be placed as close to VBAT pins as possible. To connect to VBAT, use capacitors with low equivalent series resistance (ESR).

Figure 4 shows a typical VBAT power supply circuit for BGA.

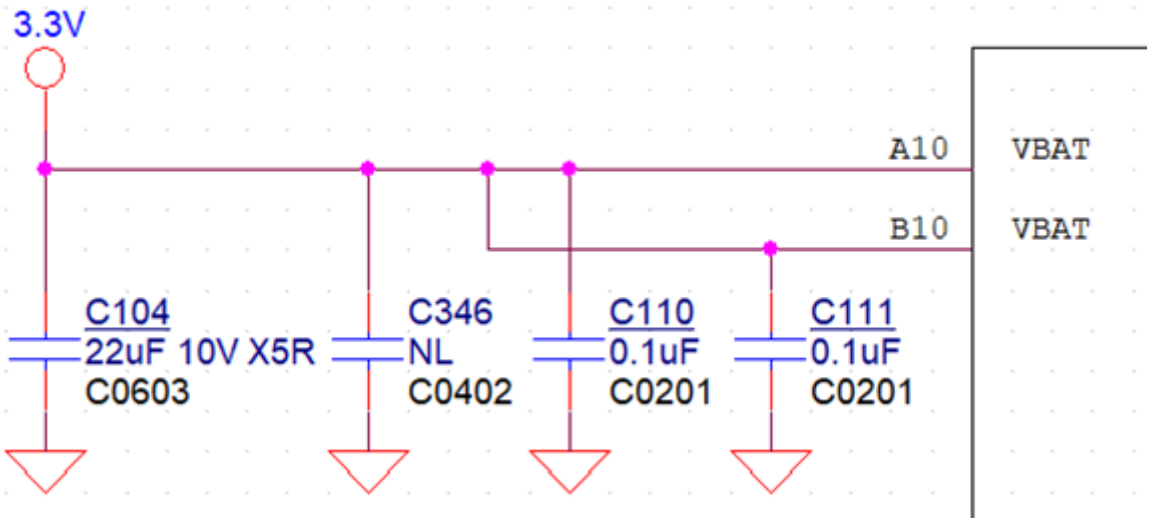

Figure 4. VBAT power supply circuit for TFBGA package

Table 2 shows the VBAT components.

Table 2. VBAT components

Component	Manufacturer	Part number
Decoupling capacitor, C104 = 22 µF (0603)	Murata	GRM188R61A226ME15
Decoupling capacitor C110 = C111 = 0.1 µF (0201)	Murata	GRM033R61A104KE84D

2.4 Internal buck regulator guidelines

The internal buck regulators supply AVDD18 and VCORE pins.

Figure 5 shows a simplified BGA application circuit for AVDD18 and VCORE supply using internal buck regulators.

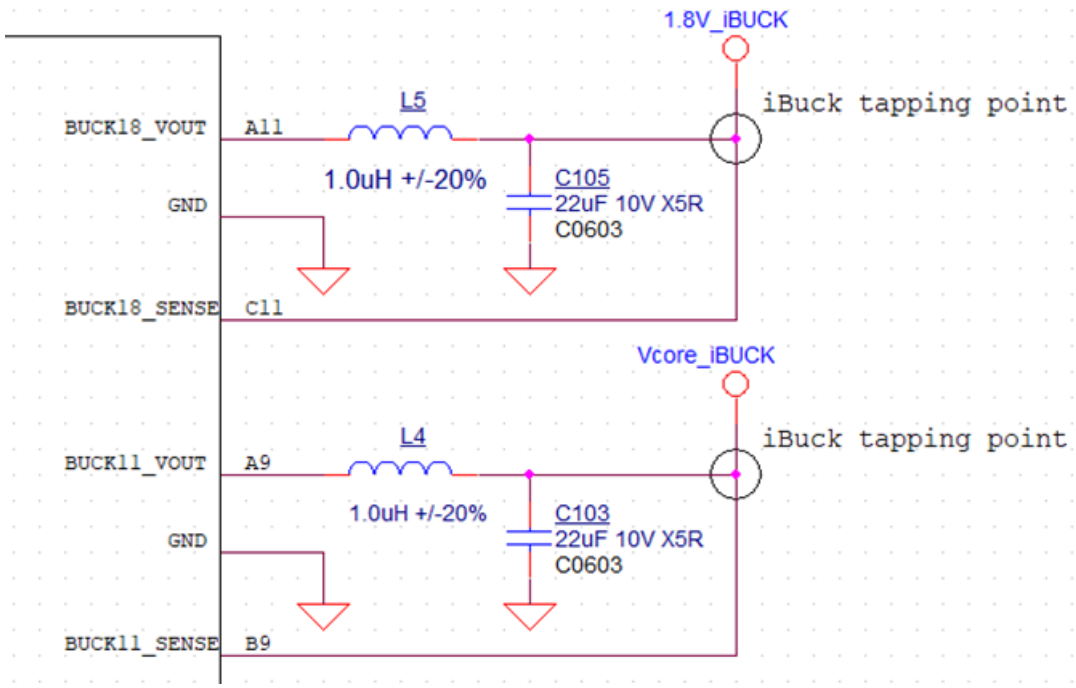

Figure 5. Application circuit for AVDD18 and VCORE - TFBGA package

Table 3 shows the 11V_iBUCK and 18_iBUCK components.

Table 3. Internal regulator components

Component	Manufacturer	Part number
Decoupling capacitor C103 = C105 = 22 µF (0603)	Murata	GRM188R61A226ME15
Inductor L4 = L5 = 1 nH (SMD 2.0x1.6x1.0mm)	Chilisin	BDUEDZ2016101R0MQ1

Note: *The tapping point of BUCK18_SENSE must not be in the path between the inductor and capacitor. The tapping point must be after the capacitor.*

- To reduce the efficiency loss, use the power inductors with low ESR.
- Use an inductor with the lowest DC resistance as possible. For example, the reference design uses a DC resistance of the selected inductor is less than 60 mΩ and Irms=2.7 A.

2.5 VCORE

To avoid false glitch detect, and to reduce noise coupling and ripples, the capacitors are placed on each VCORE pin.

Figure 6 shows 470 pF capacitors (C117, C287, C124, and C292) placed on VCORE pins on BGA package.

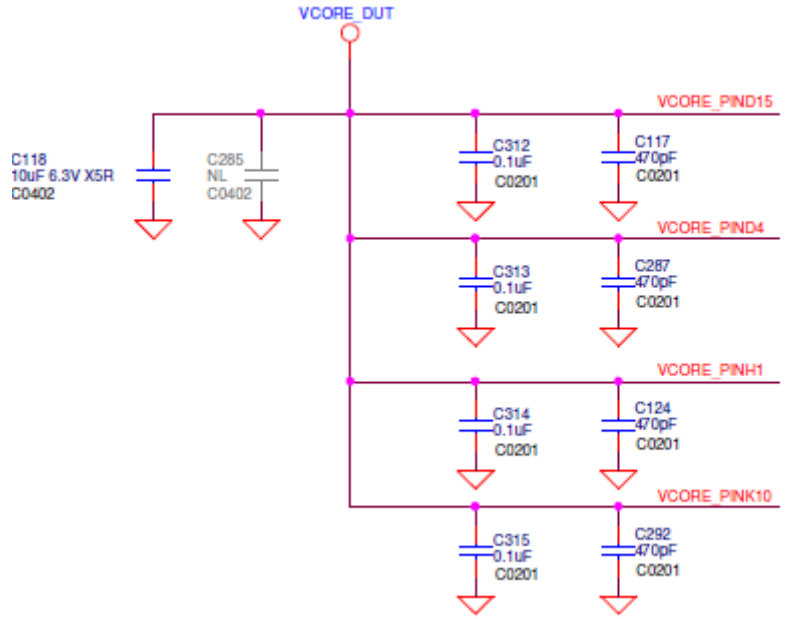

Figure 6. Capacitors on VCORE (BGA package)

Note: *For QFN package, the capacitors C117, C287, C124, and C292 are 180 pF.*

Table 4 shows VCORE components.

Table 4. VCORE components

Component	Manufacturer	Part number
Decoupling capacitor, C118 = 10 µF (0402)	Murata	GRM155R60J106ME44D
Decoupling capacitor C312 = C313 = C314 = C315 = 0.1 µF (0201)	Murata	GRM033R61A104KE84D
Decoupling capacitor C117 = C287 = C124 = C292 = 470 pF (0201)	Murata	GRM033R71E471K

2.6 VPA

VPA is the power supply to the internal Wi-Fi PA. Decoupling capacitors are required for the VPA supply pin. The capacitor values are 10 µF and 100 pF. The 100 pF capacitors must be placed as close to VPA pins as possible.

Figure 7 shows a VPA power supply circuit.

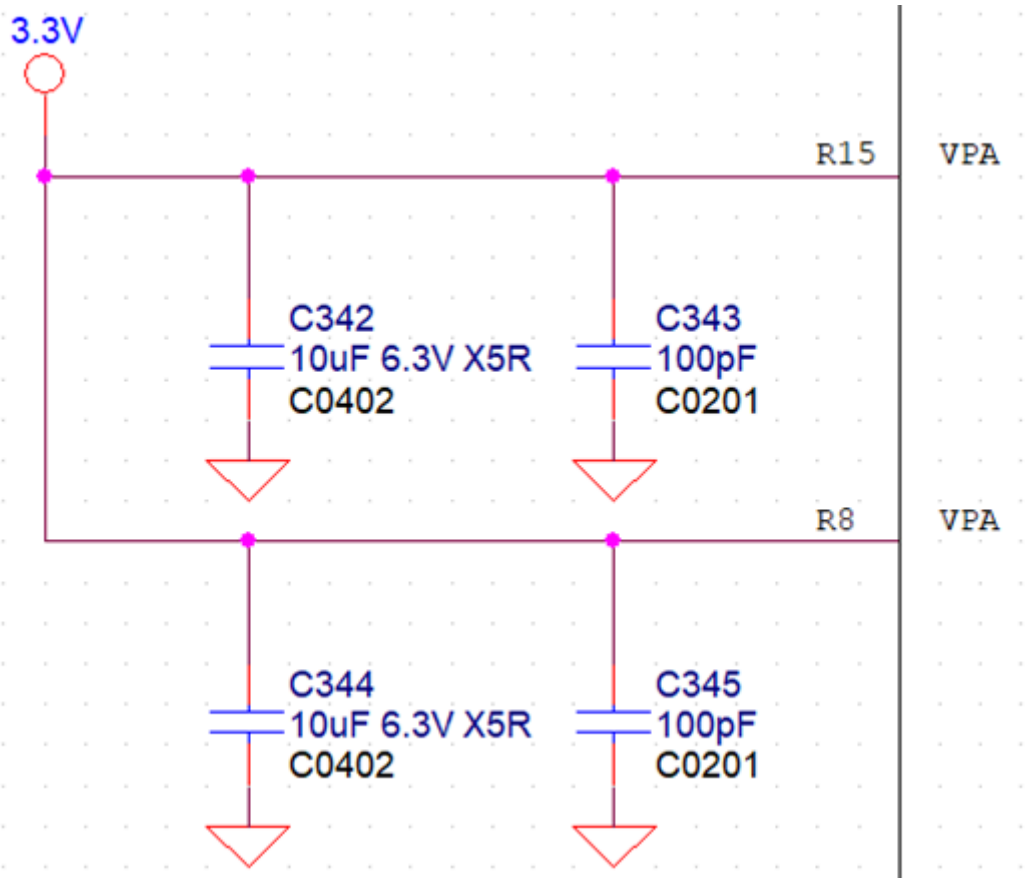

Figure 7. VPA power supply circuit

Table 5 shows VPA components.

Table 5. VPA components

Component	Manufacturer	Part number
Decoupling capacitor C342 = C344 = 10 µF (0402)	Murata	GRM155R60J106ME44D
Decoupling capacitor C343 = C345 = 100 pF (0201)	Murata	GCM033R71E101KA03

2.7 AVDD18

Each AVDD18 supply pin requires one capacitor unless stated otherwise. Refer to the NXP reference design for details. Figure 8 shows the typical circuit of AVDD18 supply pins.

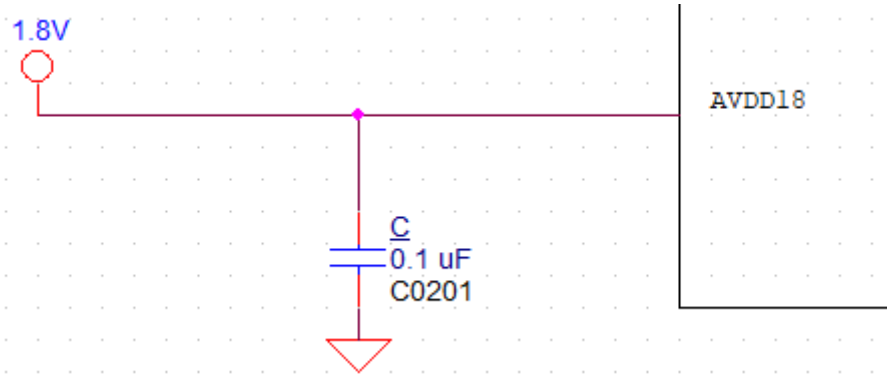

Figure 8. Circuit for AVDD18 supply pins

Table 6 shows AVDD18 components.

Table 6. AVDD18 components

Component	Manufacturer	Part number
Decoupling capacitor C = 0.1 µF (0201)	Murata	GRM033R61A104KE84D

One AVDD18 pin requires an RC filter. Table 7 shows the pin number in RW61x packages.

Table 7. AVDD18 pin with RC filter

Package	Pin number
TFBGA	J15
HVQFN	68
WLCSP	Y6

Figure 9 shows the typical circuit of AVDD18 supply pin with RC filter.

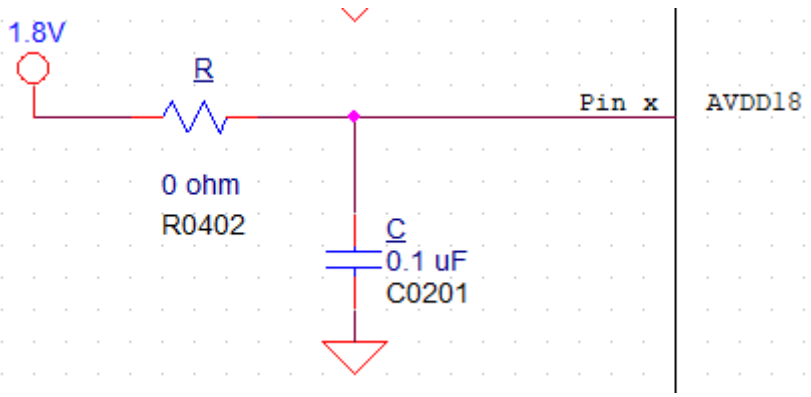

Figure 9. Circuit for AVDD18 supply pin with RC filter

Table 8 shows the components of AVDD18 supply pin with RC filter.

Table 8. Components of AVDD18 supply pin with RC filter

Component	Manufacturer	Part number
Series resistor R = 0 ohm (0402)	CYNTEC	PFR05S-000-XNH
Decoupling capacitor C = 0.1 µF (0201)	Murata	GRM033R61A104KE84D

2.8 VIO

RW61x VIO pins are supplied by either 3.3 V or 1.8 V (with exceptions).

- VIO_RF can be 3.3 V or 1.8 V based on RF front-end requirements and on the selected switch. VIO_RF performs best at 3.3 V For the SPDT switch used in NXP reference design.
- VIO_3 is an always on (AON) supply that requires an external supply.

Each supply pin requires one decoupling capacitor unless stated otherwise. Refer to the NXP reference design for details. Figure 10 shows the typical circuit of VIO supply pins.

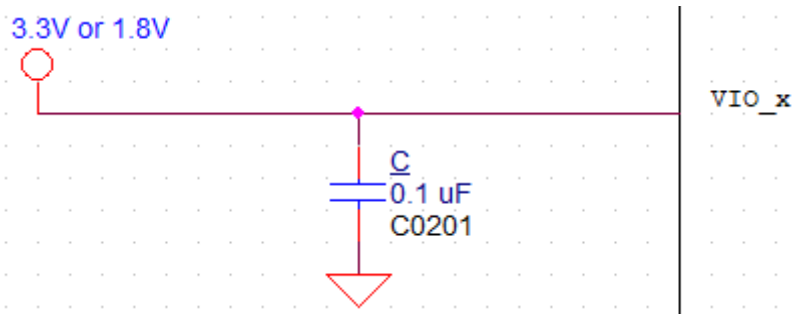

Figure 10. Circuit for VIO supply pins

Table 9 shows VIO components.

Table 9. VIO components

Component	Manufacturer	Part number
Decoupling capacitor C = 0.1 µF (0201)	Murata	GRM033R61A104KE84D

2.9 Power-up sequence

Refer to the section *Power-up sequence* in RW61x data sheets [1] and [2].

Make sure the PDn (power down) is deasserted after all external power supplies are up.

2.10 PCB layout guidelines

Refer to the following PCB layout guidelines for power supply:

- Place the power inductor as close to BUCK_OUT as possible.
- Separate BUCK_VOUT and BUCK_SENSE as much as possible to reduce coupling in between. BUCK_VOUT is a switching node.
- Use a minimum trace width for BUCK_SENSE to reduce noise pickup. The trace can be routed to a different layer to reduce coupling.
- Place the decoupling capacitor as close as possible to the power inductor.
- Use the lowest possible impedance to connect BUCK18 and BUCK11 decoupling capacitor (22 µF) ground to EPAD in the QFN case. The same layer is recommended.
- The supply rails and respective decoupling caps must share the ground and supply plane.
- If there is no direct connection between the critical decoupling caps connection to the ground and power plane, use multiple vias to reduce parasitic inductance.
- Calculate the optimal trace width for connecting BUCK_VOUT and inductor based on the maximum inductor current rating.
- Use power planes or wide traces as much as possible for power supply rails.
- Place the power vias and ground vias as close as possible to the decoupling capacitors, as shown in Figure 11.

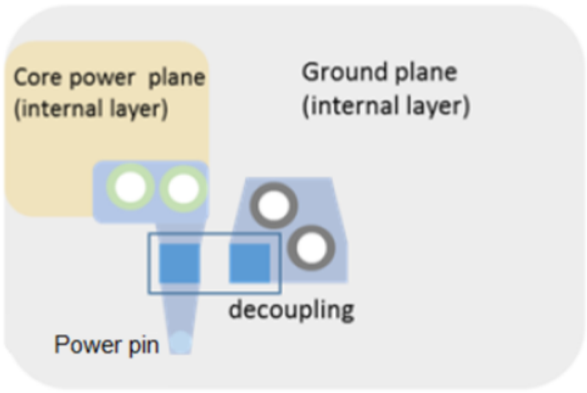

Figure 11. Power vias and ground vias

- The power from source to power pin must go through the decoupling network before connecting to the power pin as shown in Figure 12.

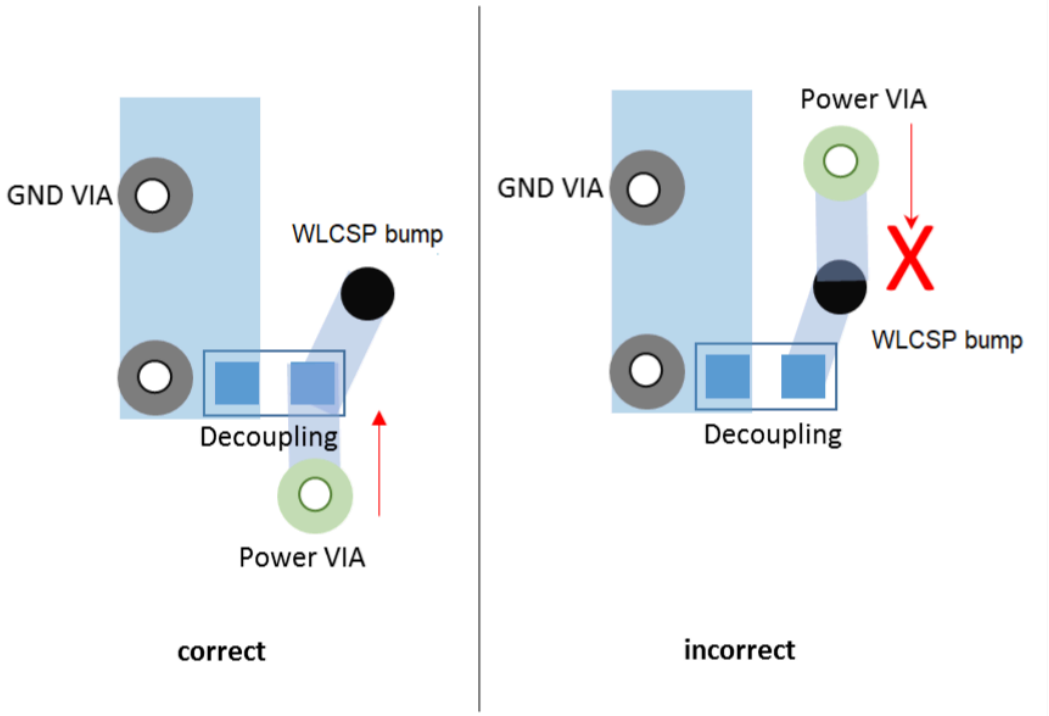

Figure 12. Example of power trace routing to power pin

- Ensure that each power pin has its own decoupling capacitors. Place the decoupling capacitors, especially the high frequency ones (C9), as close as possible to the power pin. Figure 13 shows an example where C9 is the decoupling capacitor for K5 pin. In this example, place C9 as close as possible to K5 pin, and place C58 close to C9.

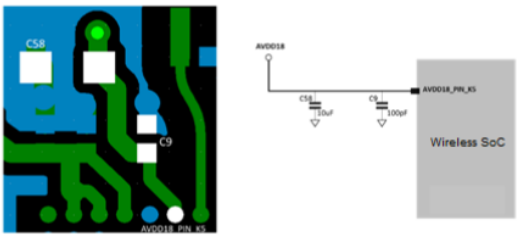

Figure 13. Decoupling capacitor and bulk capacitor placements

- Ensure the current return path/loop is as small as possible. The current loop consists of BUCK18_VOUT, inductor, capacitor, and ground pins. Figure 14 shows the buck input ground loop

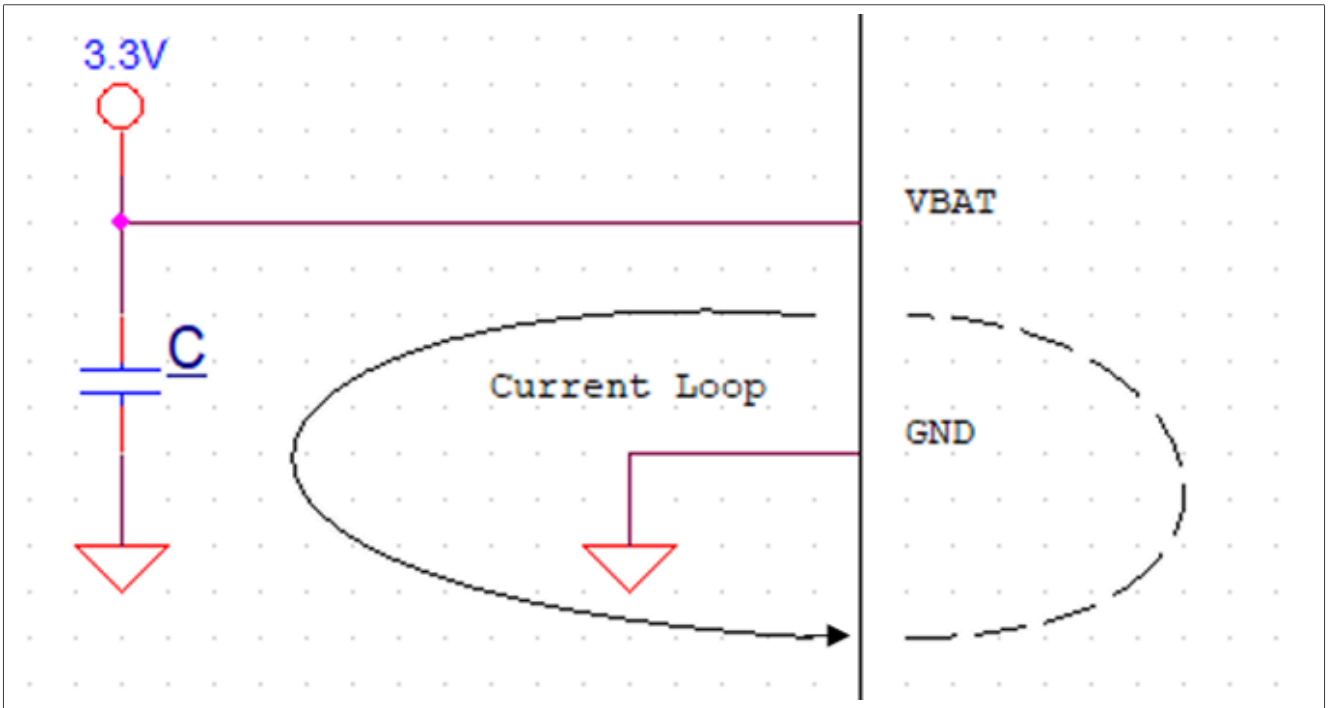

Figure 14. Buck input ground loop

Figure 15 shows the buck output ground loop.

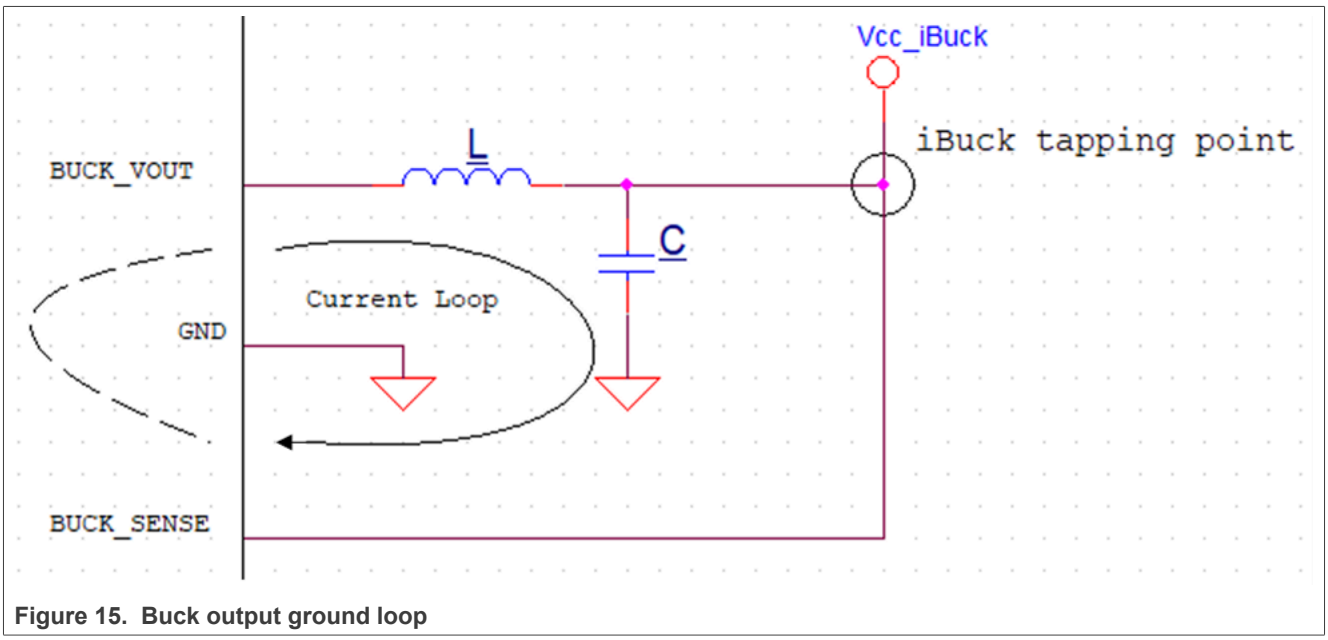

Figure 15. Buck output ground loop

3 RF interface

NXP reference designs for the Wireless SoC show the front-end configurations currently supported by NXP. Discuss your desired front-end configuration with your NXP representative and have your design reviewed by NXP.

3.1 RF front-end for TFBGA and HVQFN packages

The RF front-end can be configured for a single or dual antenna design with or without antenna diversity.

In a dual-antenna design with or without antenna diversity, one antenna is for Wi-Fi and the other antenna is for Bluetooth LE/802.15.4.

In a single antenna application, the antenna is shared between Wi-Fi and Bluetooth LE/802.15.4.

3.1.1 Dual antenna RF front-end without antenna diversity

Figure 16 shows the typical RF front-end topology for a dual-antenna design without antenna diversity. Use discrete low-pass filters (LPF) to ensure the rejection of out-of-band emissions. LPF components also act as impedance matching circuits between the wireless SoC pin and the diplexer part on the PCB. For maximum power transfer in RF, the input/output impedance must match 50 Ω.

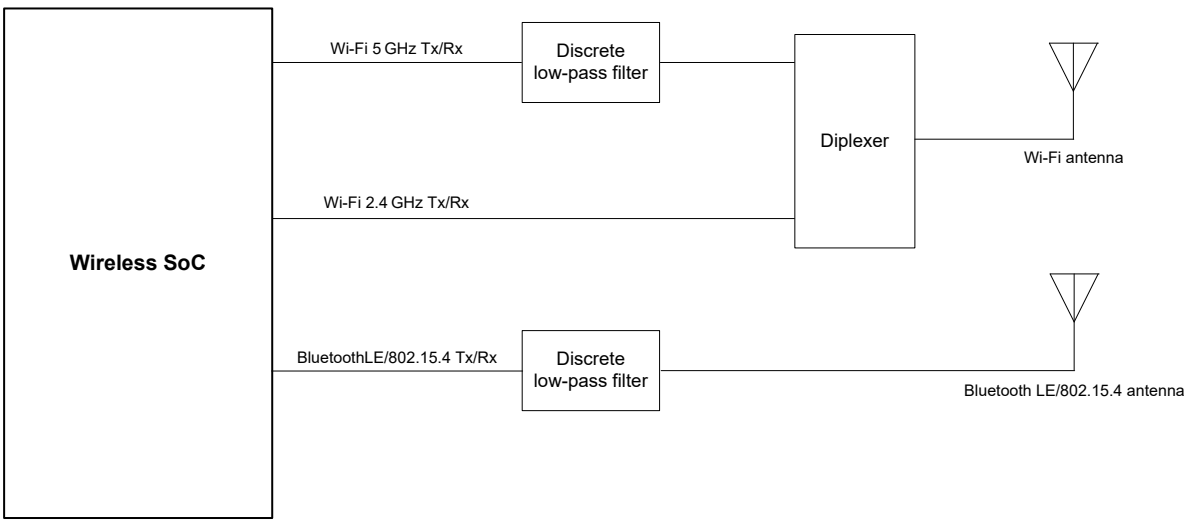

Figure 16. RF front-end diagram for dual-antenna configuration without antenna diversity

Figure 17 shows the typical circuit diagram for a two-antenna design without antenna diversity.

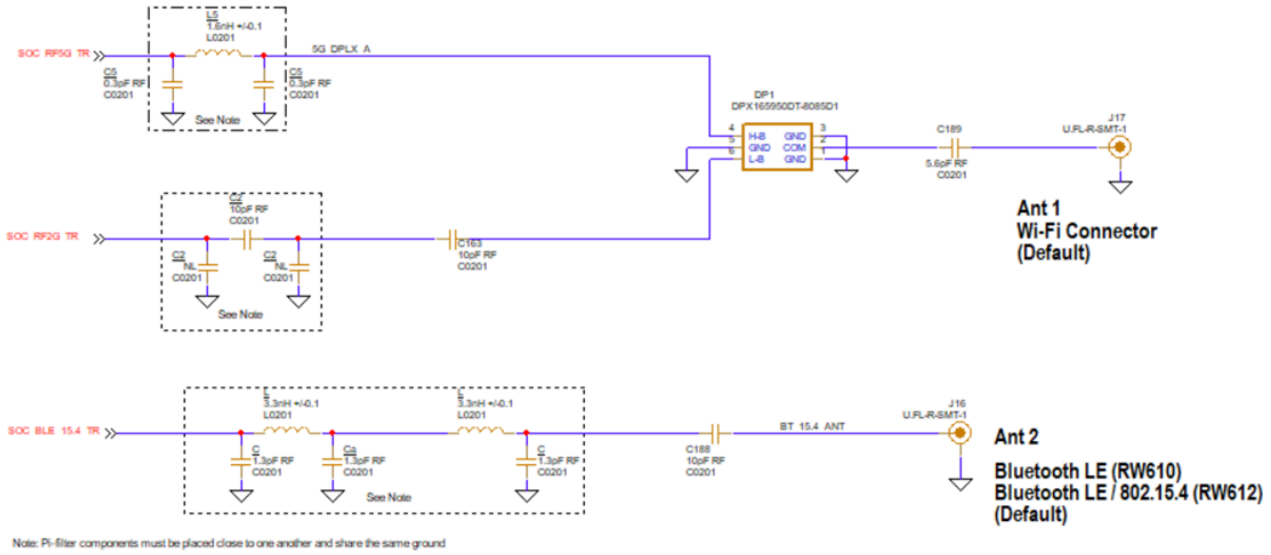

Figure 17. Circuit diagram for dual-antenna configuration without antenna diversity

Table 10 lists the recommended RF front-end components for two-antenna without diversity.

Table 10. RF front-end components for two antennas and no diversity

RF component	Manufacturer	Part number
Diplexer	TDK	DPX165950DT-8085D1
Discrete LPF on Wi-Fi 5 GHz path	—	L5 = 1.6 nH ± 0.1 nH (0201), C5 = 0.3 pF (0201)
Discrete LPF on Wi-Fi 2.4 GHz path[1]	—	C2 = 10 pF (0201), C3 = NL
Discrete LPF on Bluetooth LE/802.15.4 path	—	C = 1.3 pF (0201), L = 3.3 nH ± 0.1 nH (0201), Ca = 2.0 pF (0201)

[1] Placeholder for filter

3.1.2 Single antenna RF front-end

Figure 18 shows the typical front-end topology for a single-antenna application. An external SPDT switch is required to select either 2.4 GHz Wi-Fi or Bluetooth LE/802.15.4 transmit/receive paths. Use discrete low-pass filters (LPF) to ensure the rejection of out of band emissions. LPF components also act as impedance matching circuits between the wireless SoC pin and the diplexer part on the PCB. For maximum power transfer in RF, the input/output impedance must match 50 Ω.

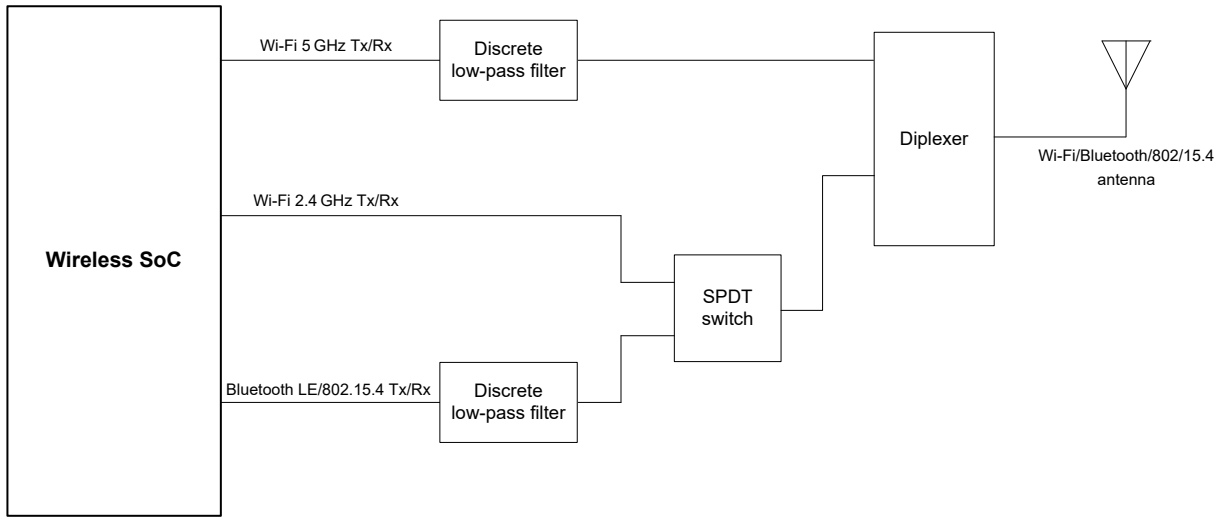

Figure 18. Front-end diagram for single-antenna application

Figure 19 shows the typical circuit diagram for a single antenna design.

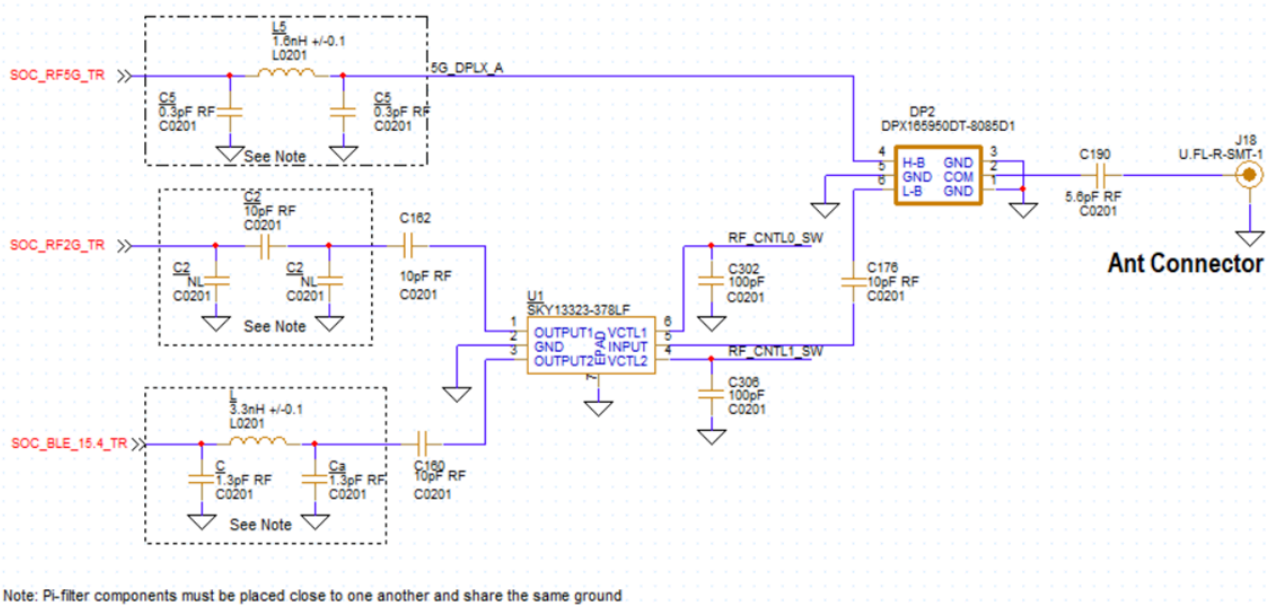

Figure 19. Circuit diagram for single-antenna design

Note: *In single antenna designs, a three-element low-pass filter is needed on the Bluetooth LE/802.15.4 RF path.*

Table 11 lists the recommended RF front-end components for a single antenna design.

Table 11. RF front-end components for single antenna designs

RF component	Manufacturer	Part number
Diplexer	TDK	DPX165950DT-8085D1
Discrete LPF on Wi-Fi 5 GHz path	—	L5 = 1.6 nH ± 0.1 nH (0201), C5 = 0.3 pF (0201)
Discrete LPF on Wi-Fi 2.4 GHz path[1]	—	C2 = 10 pF (0201), C3 = NF
Discrete LPF on Bluetooth LE/802.15.4 path	—	C = 1.3 pF (0201), L = 3.3 nH ± 0.1 nH (0201), Ca = 1.3 pF (0201)
SPDT RF switch 0.1GHz-3GHz	Skyworks	SKY13323-378LF

[1] Placeholder for filter

3.1.3 Single antenna RF front-end with antenna diversity

Figure 20 shows the typical RF front-end topology for a single antenna design with antenna diversity. Two external SPDT switches are required to switch Wi-Fi and Bluetooth LE/802.15.4 paths. Use discrete low-pass filters (LPF) to ensure the rejection of out-of-band emissions. LPF components also act as impedance matching circuits between the wireless SoC pin and the diplexer part on the PCB. For maximum power transfer in RF, the input/output impedance must match 50 Ω.

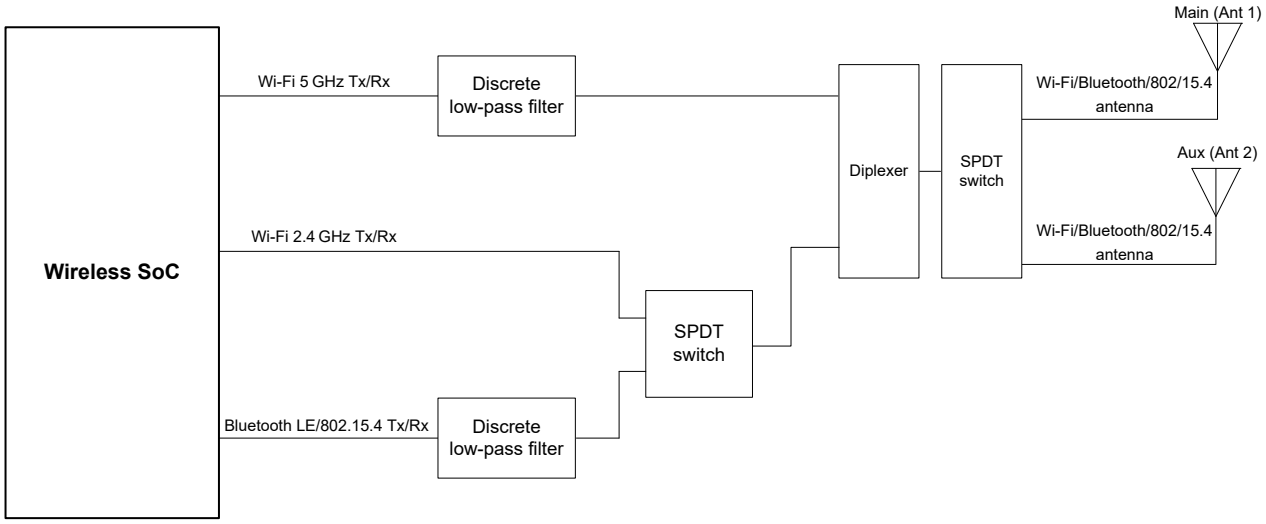

Figure 20. RF front-end diagram- Single antenna with diversity

Figure xx shows the typical circuit diagram for a single antenna design.

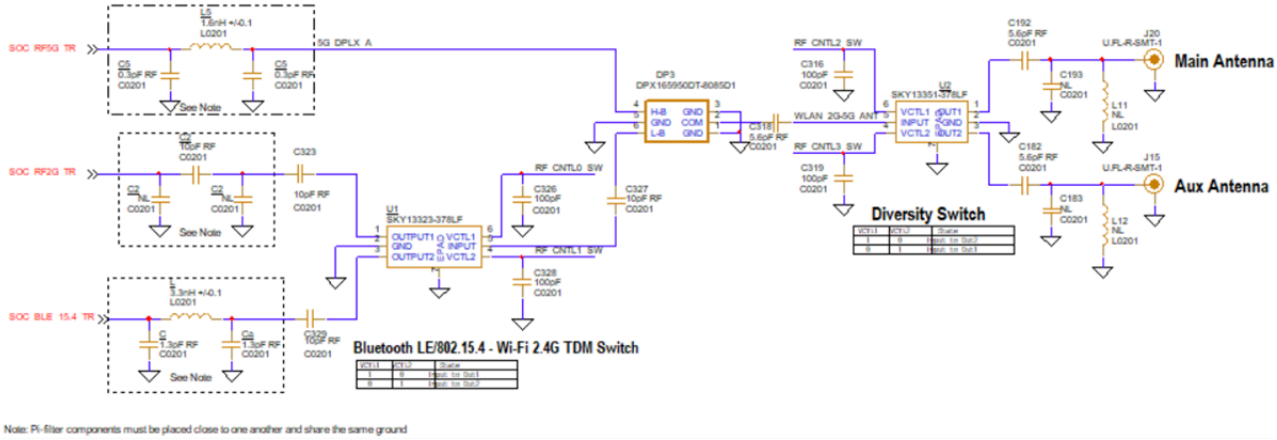

Figure 21. Circuit diagram for single antenna with diversity

Table 12 lists the recommended RF front-end components for a single antenna design with antenna diversity.

Table 12. RF front-end components for single-antenna design with antenna diversity

RF component	Manufacturer	Part number
Diplexer	TDK	DPX165950DT-8085D1
Discrete LPF on Wi-Fi 5 GHz path	—	L5 = 1.6 nH ± 0.1 nH (0201), C5 = 0.3 pF (0201)
Discrete LPF on Wi-Fi 2.4 GHz path[1]	—	C2 = 10 pF (0201), C3 = NF
Discrete LPF on Bluetooth LE/802.15.4 path	—	C = 1.3 pF (0201), L = 3.3 nH ± 0.1 nH (0201), Ca = 1.3 pF (0201)
SPDT RF switch 0.1GHz-3GHz	Skyworks	SKY13323-378LF
SPDT RF switch 20MHz-6GHz	Skyworks	SKY13351-378LF

[1] Placeholder for filter

3.2 RF front-end for WLCSP package

RF front-end for the WLCSP package is the same as for the TFBGA package.

Note: *For optimized PCB design, NXP RW61x EVB for WLCSP package uses a different diplexer pinout than TFBGA design.*

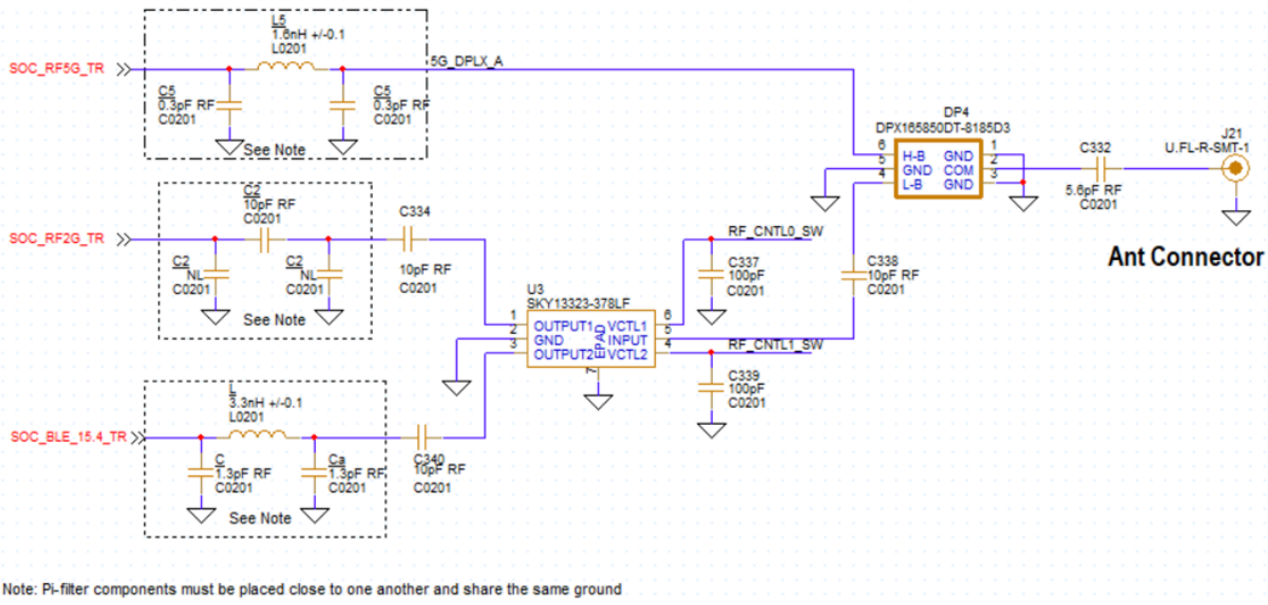

Figure 22. RF front-end diagram for WLCSP package

Table 13. Recommended RF front-end components for single-antenna design and WLCSP package

RF component	Manufacturer	Part number
Diplexer	TDK	DPX165850DT-8185D3
Discrete LPF on Wi-Fi 5 GHz path	—	L5 = 1.6 nH ± 0.1 nH (0201), C5 = 0.3 pF (0201)
Discrete LPF on Wi-Fi 2.4 GHz path[1]	—	C2 = 10 pF (0201), C3 = NF
Discrete LPF on Bluetooth LE/802.15.4 path	—	C = 1.3 pF (0201), L = 3.3 nH ± 0.1 nH (0201)
SPDT RF switch 0.1GHz-3GHz	Skyworks	SKY13323-378LF

[1] Placeholder for filter

3.3 PCB layout guidelines

Refer to the following PCB layout guidelines for RF interface:

- Route the RF signals on the top layer (micro strip) with 50 ohm impedance.
- Reference the RF signals to a solid ground plane.
- To minimize the impact on the micro strip impedance, use at least a 3X H clearance between the ground pour and RF micro strip. Maintain this gap around any RF signal via, as shown in Figure 23.

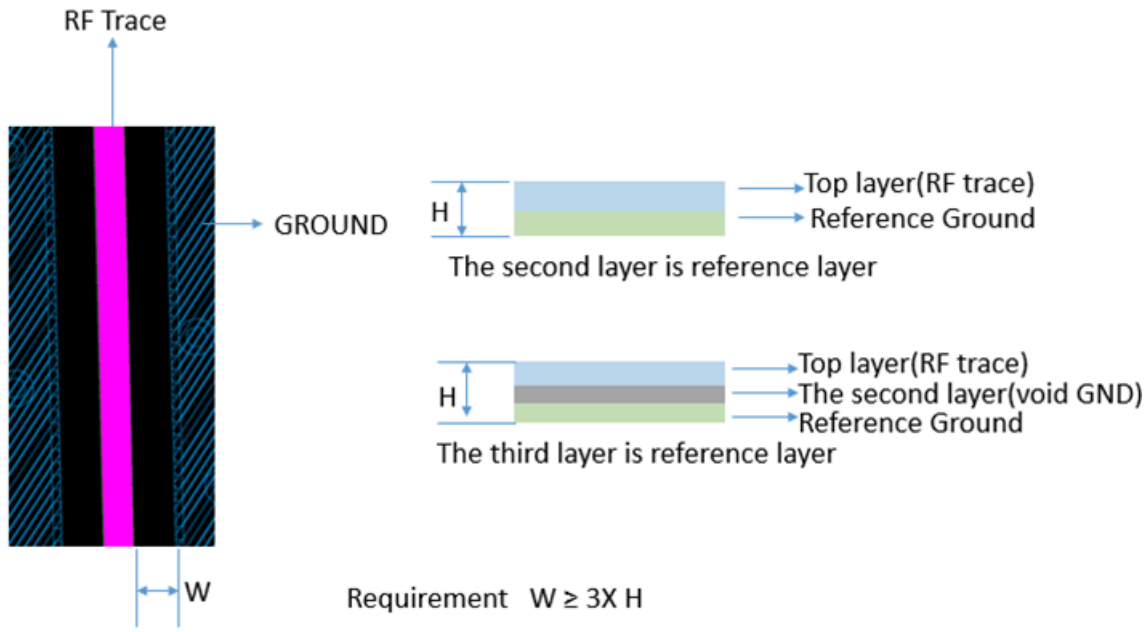

Figure 23. Guidelines for RF micro strip

- Keep the RF trace lengths as short as possible.
- The bend trace routing must be smooth with a large radius rather than of 90 degrees with a sharp edge.
- Place stitching ground vias between the top and reference ground layers to increase isolation as shown in Figure 24.

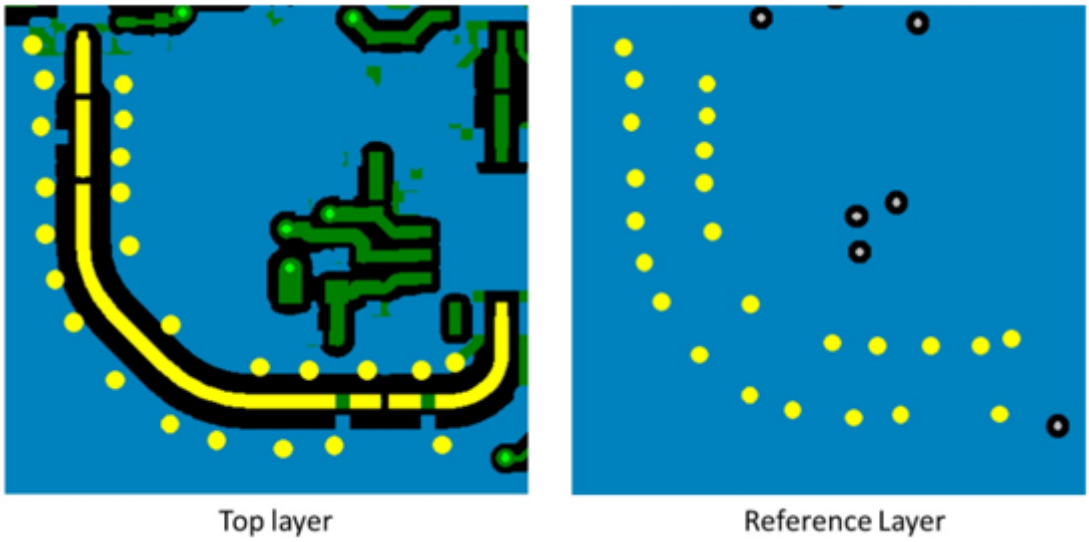

Figure 24. Guidelines for stitching ground vias

- Extend the ground plane between paths as much as possible. Extend the ground to the point where a ground via can be placed at the end, as shown in Figure 25.

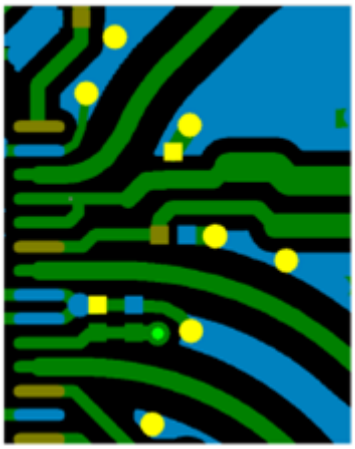

Figure 25. Guidelines for the ground plane

- Keep the RF control signal traces as far away as possible from the RF traces.
- Follow the recommendations of the manufacturer for RF front-end parts. For example, add ground vias close to the ground pin of the front-end part.
- RF ground via along the RF shield must be less than a 100 mil interval.
- Ground via must be close to the matching capacitor ground pin.
- RF trace to RF connector pad transition must be tapered to avoid discontinuity and high insertion loss, especially at 5 GHz band. An example is shown in Figure 26.
- Cut out all layers under RF connector signal pad.

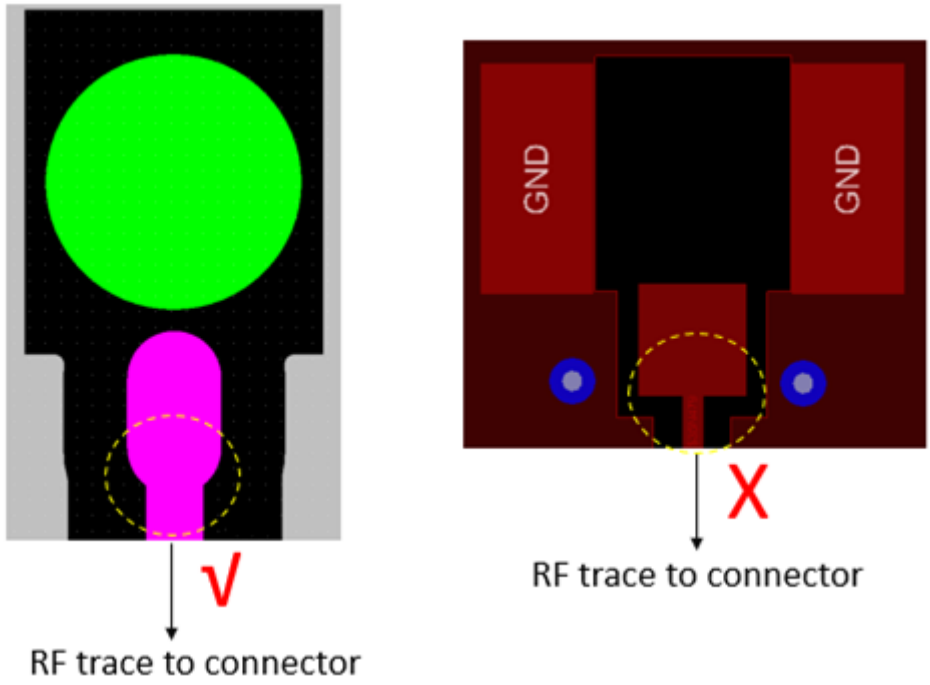

Figure 26. Guidelines for RF trace to connector

- Place (recommendation) a nonplated through hole under the RF connector to minimize the insertion loss as shown in Figure 27.

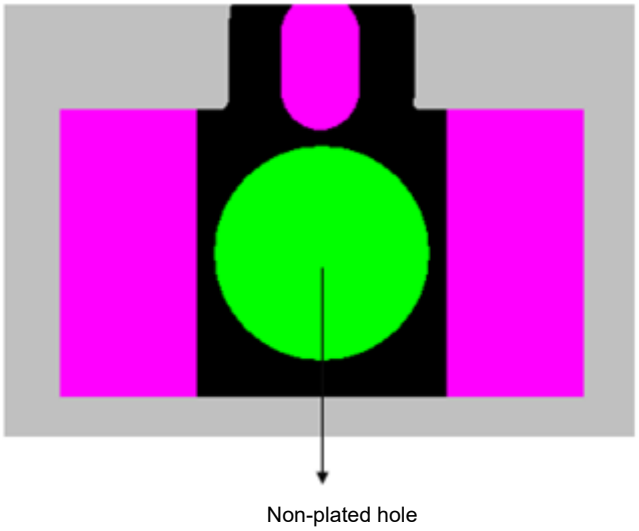

Figure 27. Recommendation - Nonplated through hole under the RF connector

- Add a ground via on each side of RF via near the RF trace layer transition. The distance between the via and RF trace edge-to-edge is about 20 mil.
- Add ground vias close to the diplexer ground pins for a good return path.
- If an ESD protection inductor is required, place the inductor close to the RF connector or close to the ESD sensitive front-end component.
- An RF shield is recommended to minimize radiated emissions and any RF interference.
- Avoid clock signal routes (system clock, SDIO_CLK, SLP_CLK) crossing the power supply traces or vice versa.
- Avoid via in pad for discrete (R,C) components. Via in pad can lead to:
  - Component assembly issues during PCB manufacturing
  - Cold solder joints during rework
  - Via damages during component rework on the PCB
  - Check with the PCB manufacturer that the assembly can handle multiple vias on the component pads.
    Note: *If multiple vias are on a component pad, move the vias out of the component pad (recommendation).*

- For HVQFN package only, add an EPAD ground under the package for thermal relief as shown in Figure 28.
- Make sure that the GND EPAD has multiple thermal vias for the thermal relief path to be effective.

Figure 28 shows QFN EPAD ground layout.

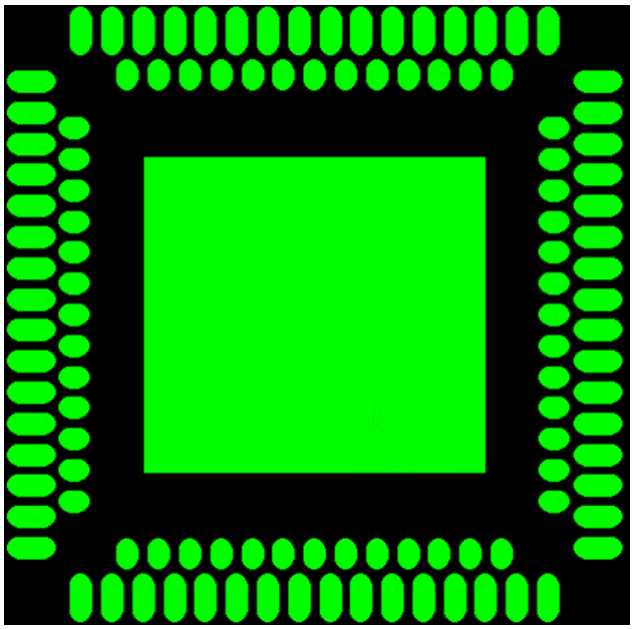

Figure 28. EPAD ground layout for QFN package

- For the WLCSP package only, do not route any signal traces, power planes, ground planes over the on-chip inductor keep-out areas. The keep-out areas of the on-chip inductor are highlighted in Figure 29.

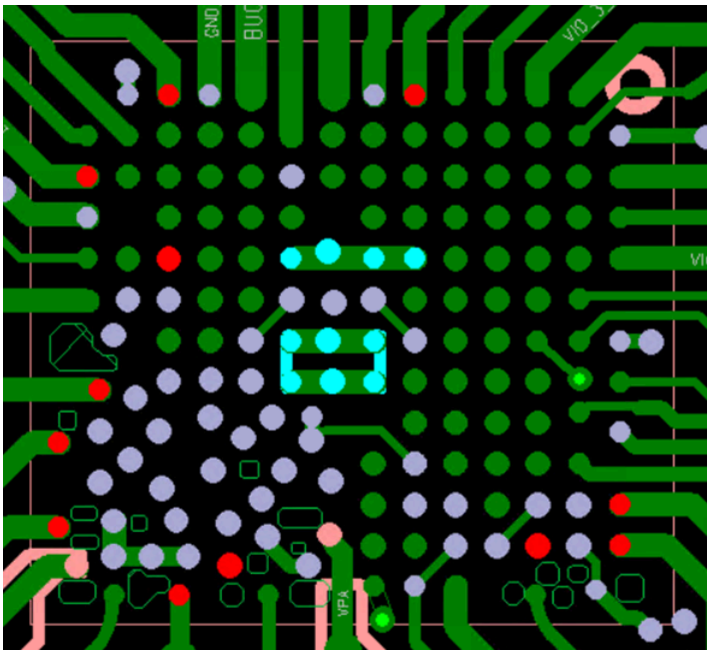

Figure 29. WLCSP keep-out areas

4 Clock source

RW61x requires a reference clock input for its operation. The reference clock can be sourced from either an external crystal or external oscillator.

4.1 Crystal

In a typical application, a 40 MHz crystal is used as a reference clock. Select a crystal with the following characteristics:

- Frequency stability of ±16 ppm over the operating temperature range.
- Typical load capacitance of 8 pF.
- Minimum drive level of 120 µW. Otherwise, the crystal degrades prematurely.

For the detailed crystal specifications, refer to RW61x data sheets [1] and [2].

Figure 30 shows the crystal connections with the Wireless SoC. The internal capacitor in the Wireless SoC is used to tune the crystal frequency. External loading capacitors are typically not needed.

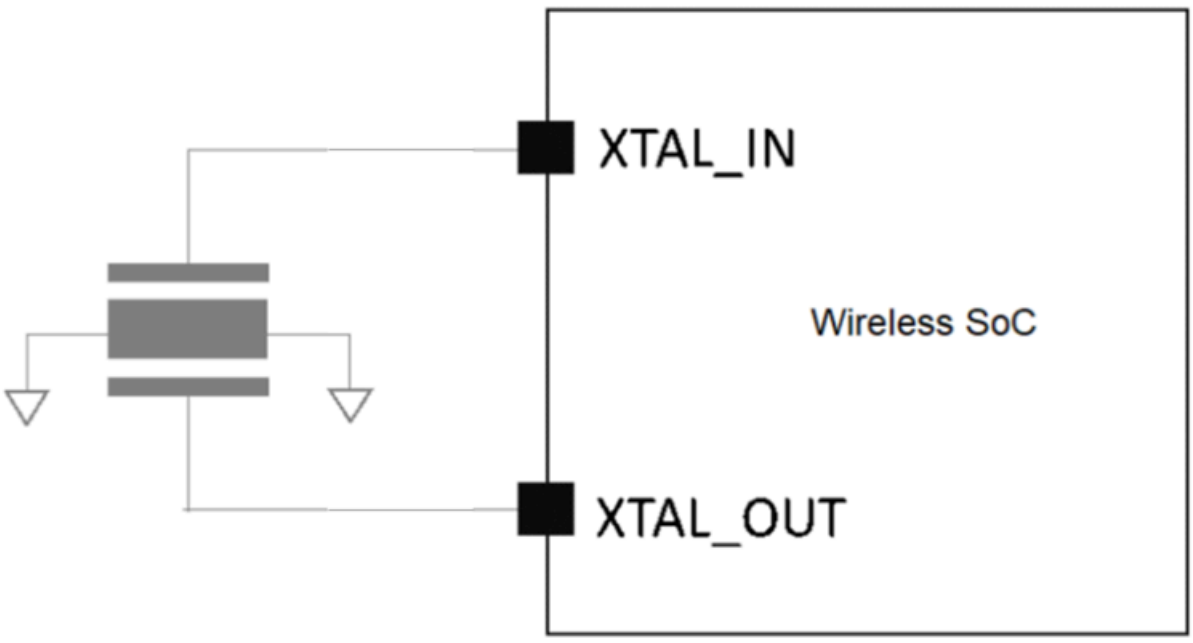

Figure 30. External crystal connections

4.1.1 PCB layout guidelines for the crystal

- Place the crystal close to the Wireless SoC.
- Keep the crystal away from the RF traces and high frequency signal traces such as SDIO, UART, and SPI interface signals, using the ground as a shield. Refer to NXP reference design.
- Keep XTAL_IN and XTAL_OUT traces far from any noisy or switching signal, at a distance of at least ten times the substrate height.
- Keep XTAL_IN and XTAL_OUT traces as short as possible, as shown in Figure 31.

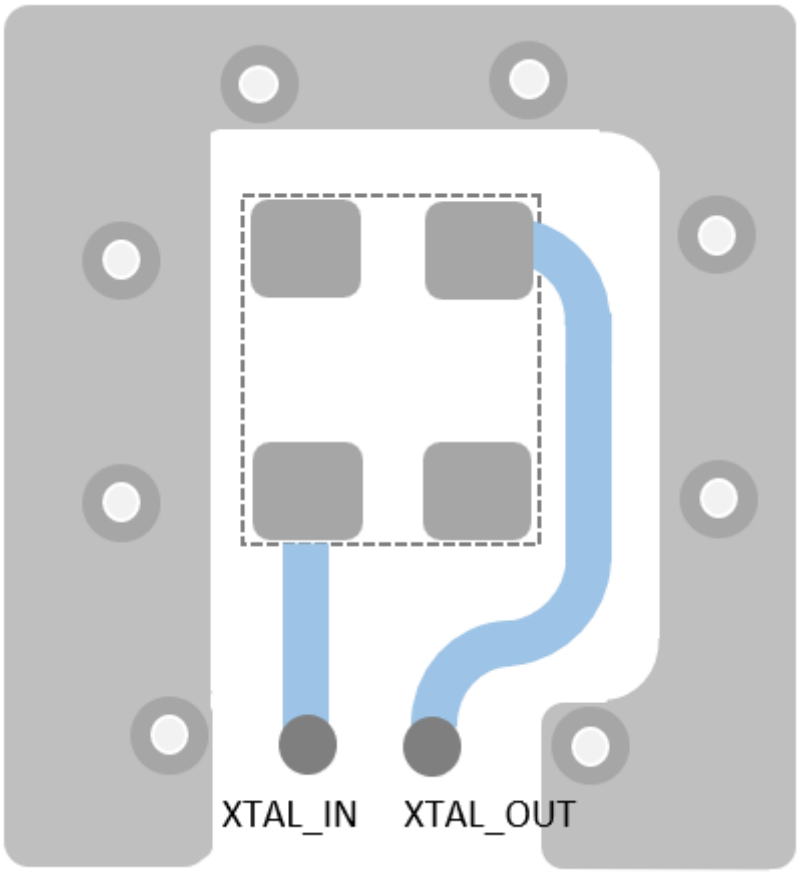

Figure 31. Crystal PCB layout

- Make sure the keep-out is on layer two, and both XTAL_IN and XTAL_OUT traces are referenced to the solid ground plane in layer three.
- Place the ground guard with ground stitching vias around the XTAL_IN and XTAL_OUT traces.
- To minimize the loss in reference clock signals, cut out all internal metal planes under the crystal, and keep the last ground plane as the reference plane.

4.2 External oscillator

Figure 32 shows the typical application circuit for an external oscillator.

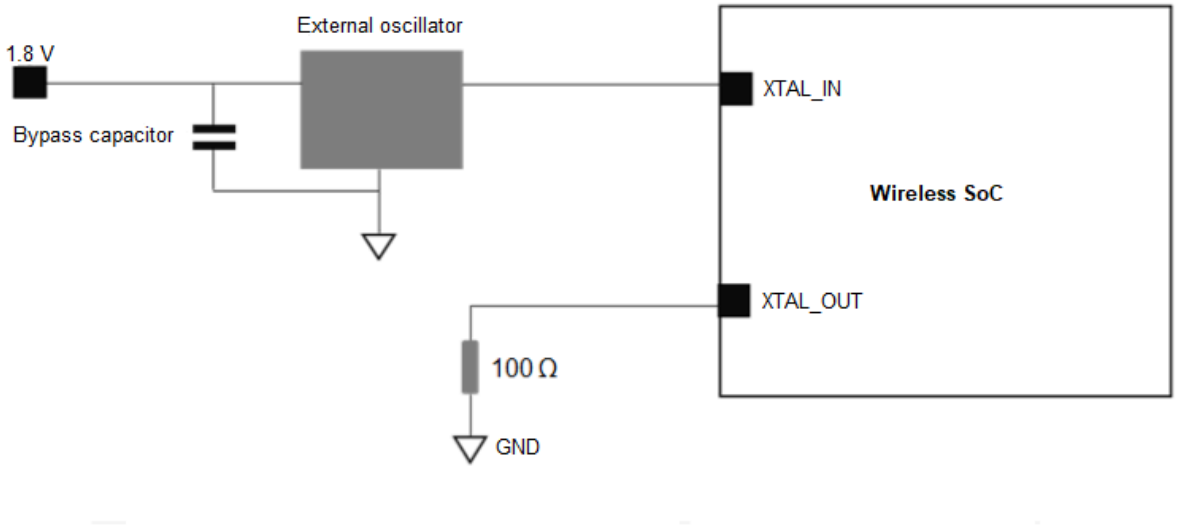

Figure 32. Application circuit for external oscillator

An external 40 MHz external oscillator can be used as a reference clock source. The clock input can be clipped sinusoidal or square wave. Make sure that its frequency accuracy meets the IEEE specification of ±20 ppm over the operating temperature range of the product. For the oscillator requirement specification, refer to RW61x data sheets [1] and [2].

Connect a 100 Ω pulldown resistor from the XTAL_OUT pin to the ground.

4.2.1 PCB layout guidelines for the external oscillator

- Follow the external oscillator recommendations of the vendor for the layout.
- Keep the oscillator away from RF traces and high frequency signal traces such as SDIO, UART, and SPI interface signals, using the ground as a shield.
- Keep the clock trace as short as possible.
- Place the ground guard with ground stitching vias around the clock trace.

5 Reset

5.1 Reset overview

The PDn signal is used to reset RW61x device. One GPIO on the host device can be used to control the PDn pin. On the NXP reference design, the PDn signal is pulled up to an external voltage level between 1.75 V and 3.63 V. Read more about PDn in RW61x data sheets [1] and [2].

5.2 Configuration pins

At RW61x power up, the configuration pins must be set before the PDn signal is deasserted.

The typical connections of the configuration pins are shown in Table 14. The pin connections are for the following configuration of RW61x:

Table 14. Pin configurations

CON	Function
[11]	RF_CNTL2/CONFIG_DAP_USE_JTAG 0 = DAP uses SWD 1 = DAP uses JTAG (default)
[5]	RF_CNTL0: Reference clock 1 = 40 MHz (default) 0 = 38.4 MHz
[3:0]	CONFIG_HOST_BOOT[3:0]/EXT_FREQ, EXT_PRI, EXT_GNT, EXT_REQ: Host configuration options. 1111 = Boot from FlexSPI Flash (default) 1110 = ISP boot (UART/I2C/SPI/USB) 1101 = Serial boot (UART/I2C/SPI/USB) 1100 = ISP boot (SDIO) 1011 = Serial boot (SDIO) 1010 = Reserved

For details on the configuration pins, refer to RW61x data sheets [1] and [2].

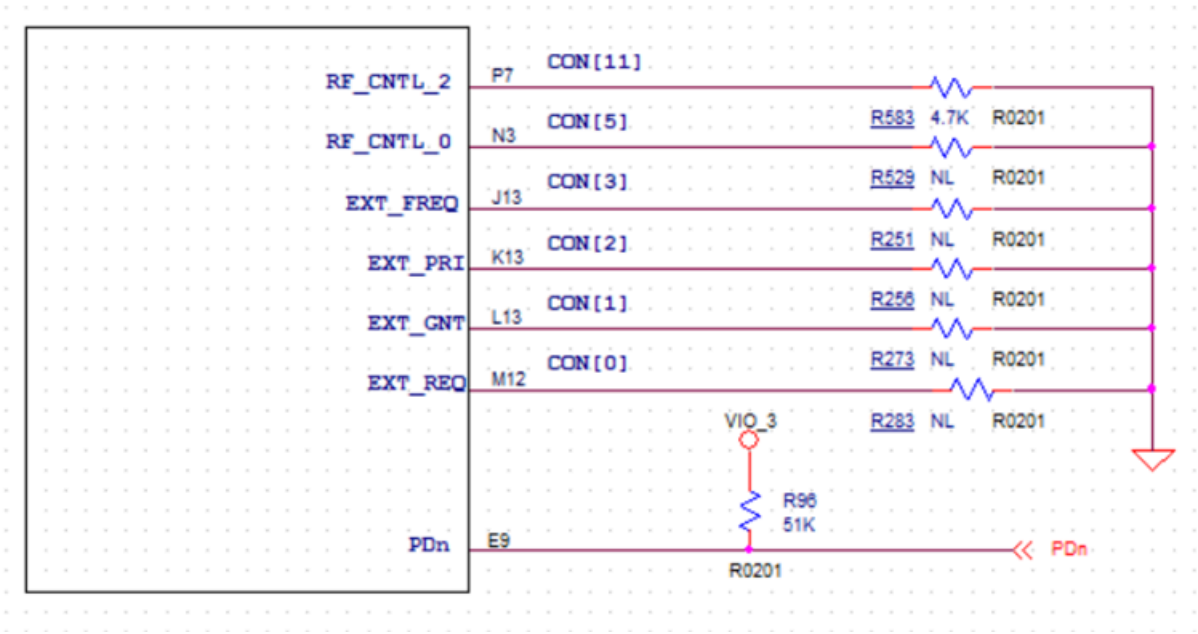

Figure 33. Configuration pins

Note: *VIO_3 is always ON (AON) and supplied with external 1.8 V or 3.3 V.*

5.3 PCB layout guidelines

- To avoid EMI affecting the reset signal, do not route the PDn signal next to a large switching signal or on the edge of the PCB. Refer to Figure 34.
- The pullup resistor on the external reset signal is placed close to the PDn pin.

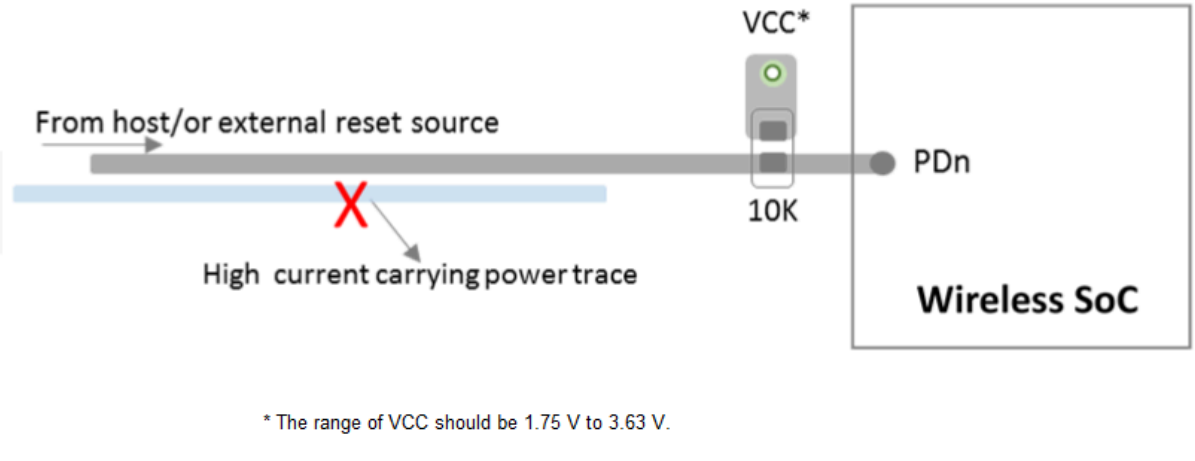

Figure 34. PCB layout guidelines

6 Memory

The FlexSPI module supports all flash memories that are JESD216 standard compliant. Refer to the data sheet of the memory part to ensure it is compatible.

6.1 FlexSPI flash

FlexSPI is a flexible serial peripheral interface between the external flash and MCU. RW61x supports a FlexSPI flash memory size up to 1 Gbit. The cache is limited to a 32 kB cache. Table 15 lists the recommended memories.

Note: *Larger densities are available from the suppliers.*

Table 15. Recommended memories

Part number	Size (Mbit)	Manufacturer
W25Q32JV (3 V)	32	Winbond
W25Q32JW (1.8 V)	32	Winbond
W25Q64JV (3 V)	64	Winbond
W25Q64JW (1.8 V)	64	Winbond
MX25U3232F (1.8 V)	32	Macronix
MX25U6432F (1.8 V)	64	Macronix

6.2 FlexSPI pSRAM

FlexSPI is used to read and write random access memory (RAM), such as working data. FlexSPI RAM memory size is limited to 1 Gbit. The cache is limited to a 32 kB cache. Table 16 lists the recommended memories.

Table 16. Recommended memories

Part number	Size (Mbit)	Manufacturer
APS1604M-SQR-(SN/ZR/RB)	16	AP Memory
APS6404L-SQH-(SN/ZR/WA)	32	AP Memory
IS66WVQ8M4DALL-200BLI	32	ISSI

6.3 Layout tips

- The D0-D3, SCK, and DQS signals must have the same length for proper sampling.
- For details on each memory layout, read the manufacturer recommendations.

7 USB OTG

For full OTG support, USB_VBUS and USB_ID pins are required. USB_VBUS is a detection pin powered by a 5 V input (to bypass external VBAT power draw).

For standard USB host/device mode, USB_VBUS is configured to bypass detection. USB_VBUS is left unconnected.

USB layout guidelines:

- Route the high-speed clocks and the DP and DM differential pair.
- Route the DP and DM signals on the top (or bottom) layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
- Route the traces over the continuous planes (power and ground):
  - They must not pass over any power/GND plane slots or anti-etch.
  - When placing the connectors, make sure that the ground plane clear-outs around each pin have ground continuity between all pins.
- Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to fewer than 5 mils.
- Maintain the symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum number of corners. Use 45 degree turns instead of 90 degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.

8 Minimum bill of materials

NXP EVB is designed for RW61x performance evaluation and software development.

The minimum bill of materials provides an optimized component count while maintaining the optimal RF performance and being a cost-effective design.

For the feature summary of TFBGA, WLCSP, and HVQFN packages, refer to the section *Package information* in RW61x data sheets [1] and [2].

RD-RW61x-BGA-IPA-2A v2.0
Bill of Material

RF critical	Item number	Quantity	Part reference	Description	Manufacturer part number
—	1	1	U37	Wireless MCU with Integrated Wi-Fi 6 + Bluetooth Low Energy 5.2 (RW610) Wireless MCU with Integrated Tri-radio Wi-Fi 6 + Bluetooth Low Energy 5.2/802.15.4 (RW612) VFBGA-145 0.5mm 8 x 8 x 0.87 mm	NXP RW61xET/A1Ixx (xx = packing option)
—	17	1	U27	IC DC-DC BUCK 2.2MHz 2.3-5.5V 2A SOT563-6 1.5X1.5x0.55mm	MPS MP1605GTF
RF critical	24	1	U41	IC RF SW SPDT 0.1GHz-3GHz VCTL 1.8V-5V MLPD-6 0.35mm 1x1x0.5mm	SkyworksSKY13323-378LF
—	38	1	U68	IC SPI/QPI SRL FLASH SIG/DUAL/QUAD I/O 512Mb 1.65V-2V DTR 166MHz WSON-8 8x6x0.8mm EP	Macronix MX25U51245GZ4I00
—	46	7	C119	CAP CER 0.1UF 10V 10% X6S AEC-Q200 0201 (0.3mm)	Murata GRT033C81A104KE01D
—	50	26	C106 C107 C108 C109 C110 C111 C112 C113 C115 C116 C117 C120 C123 C124 C125 C126 C131 C132 C135 C136 C138 C141 C143 C146 C147 C148	CAP CER 0.1uF 10% 10V X5R 0201 (0.3mm)	Murata GRM033R61A104KE84D
—	52	1	C279	CAP CER 0.1uF 10% 6.3V X5R 0201 (0.3mm)	Murata GRM033R60J104K
—	53	2	C103 C105	CAP CER 22uF 20% 4V X5R 0603 (0.8mm)	Murata GRM188R60G226MEA0D
—	54	3	C104 C253 C254	CAP CER 22uF 20% 10V X5R 0603 (0.8mm)	Murata GRM188R61A226ME15
—	56	3	C149 C152 C164	CAP CER 10uF 20% 6.3V X5R 0402 (0.5mm)	Murata GRM155R60J106ME44D
—	58	3	C144 C302 C306	CAP CER 100pF 10% 25V X7R 0201 (0.3mm)	Murata GCM033R71E101KA03
RF critical	60	2	C145 C153	CAP CER 2.4pF ±0.1pF 25V C0G 0201 (0.3mm)	Murata GJM0335C1E2R4B
RF critical	63	3	C163 C177 C188	CAP CER 10pF 5% 25V C0H 0201 (0.3mm)	Murata GJM0336C1E100JB01
RF critical	66	1	C189	CAP CER 5.6pF ±0.25pF 25V C0G 0201 (0.3mm)	Murata GJM0335C1E5R6C
—	78	1	C291	CAP CER 10UF 6.3V 20% X6S HIGH TEMP 0402 (0.5mm)	Murata GRM155C80J106ME11D
RF critical	89	1	DP1	DPLX DB f1(LPF) 2400-2500MHz, f2(HPF) 4900-5950MHz, IL(f1)=0.60dB MAX, IL(f2)=0.7dB MAX, LGA-6 1.6x0.8x0.6mm	TDK DPX165950DT-8085D1
—	115	2	J15 J16	CONN RF U.FL COAX MALE 3X3.1mm PCMNT SMD	Hirose U.FL-R-SMT-1
—	121	2	L4 L5	IND PWR 1.0uH ±20% Irms=2.7A SMD 2.0x1.6x1.0mm	Chilisin BDUEDZ2016101R0MQ1
—	133	2	R500 R538	RES THICK FILM 0Ω 1/16W 5% 0402 SMD	Cyntec PFR05S-000-XNH
—	139	6	R412 R482 R494 R516 R551 R560	RES THICK FILM 0Ω 1/20W 1% 0201 SMD	Cyntec PFR03S-000-XNH_x
—	150	1	R155	RES THICK FILM 44.2kΩ 1/20W 1% 0201 SMD	Cyntec PFR03S-4422-FNH
—	160	3	R565 R583 R585	RES THICK FILM 4.7kΩ 1/16W 5% 0402 SMD	Cyntec PFR05S-472-JNH
—	179	2	R411	RES THICK FILM 100kΩ 1/20W 1% 0201 SMD	Panasonic ERJ-1GNF1003C
—	185	3	R472 R476 R504	RES THICK FILM 51kΩ 1/20W 5% 0201 SMD	Cyntec PFR03S-513-JNH
—	195	1	Y2	XTAL 40MHz ±8ppm FUND 8pF 40Ω -40°C to +85°C, SMD 1.6X1.2X0.3mm	TXC 8Q40070007

Figure 35. Minimum bill of materials for dual antenna without diversity

9 Miscellaneous

9.1 Unused interfaces and pins

Table 17. Unused interfaces and pins

Pin name	PCB connection when not used
XTAL_OUT	Connect a 100 Ω resistor to ground
RF_TR_2	Connect a 50 Ω resistor to ground
RF_TR_5	Connect a 50 Ω resistor to ground
BRF_ANT	Connect a 50 Ω resistor to ground
AVDD33 (USB)	Connect to 3.3 V supply rail
USB_DP	Keep floating/No connection
USB_DM	Keep floating/No connection

9.2 GPIOs

For the typical alternate functions assigned to the GPIO pins, refer to the RW61x data sheets [1] and [2]. If the GPIO pins are not used, keep them unconnected.

Table 18 shows GPIO assignments for Flexcomm functions.

Table 18. GPIO assignments for Flexcomm functions

Pin name	Flexcomm function						Ethernet
GPIO #	**Flexcomm #**	**USART**	**I2C**	**I2S**	**SPI**	**SDIO**	**RMII I/F**
0	0	USART_CTS	—	—	SPI_CS	—	—
2		USART_RXD	I2C_SDA	I2S_DAT	SPI_MOSI	—	—
3		USART_TXD	I2C_SCL	I2S_WS	SPI_MISO	—	—
4		USART_CLK	—	I2S_CLK	SPI_CLK	—	—
5		USART_RTS	—	I2S_MCLK	—	—	—
6	1	USART_CTS	—		SPI_CS	—	—
7		USART_CLK	—	I2S_CLK	SPI_CLK	—	—
8		USART_TXD	I2C_SCL	I2S_WS	SPI_MISO	—	—
9		USART_RXD	I2C_SDA	I2S_DAT	SPI_MOSI	—	—
10		USART_RTS	—	—	—	—	—
13	2	USART_RXD	I2C_SDA	I2S_DAT	SPI_MOSI	—	—
14		USART_TXD	I2C_SCL	I2S_WS	SPI_MISO	—	—
15		USART_CLK	—	I2S_CLK	SPI_CLK	SDIO_CLK	—
16		USART_CTS	I2C_SDA(backup)		SPI_CS	SDIO_DAT3	—
17		USART_RTS	I2C_SCL(backup)			SDIO_CMD	—
19	3	USART_RTS	I2C_SCL(backup)			SDIO_DAT2	—
20		USART_CTS	I2C_SDA(backup)		SPI_CS	SDIO_DAT0	—
22	—	—	—	—	—	SDIO_DAT1	ENET_RX_DATA0
23	—	—	—	—	—	—	ENET_RX_DATA1

Table 18. GPIO assignments for Flexcomm functions*...continued*

Pin name	Flexcomm function						Ethernet
24	3	USART_RXD	I2C_SDA	I2S_DAT	SPI_MOSI	—	ENET_TIMER2
25		USART_CLK		I2S_CLK	SPI_CLK	—	ENET_CLK
26		USART_TXD	I2C_SCL	I2S_WS	SPI_MISO	—	ENET_TIMER3
27	—	—	—	—	—	—	ENET_TIMER0
53	14	USART_CTS	—	—	SPI_CS	—	—
54		USART_CLK	—	I2S_CLK	SPI_CLK	—	—
55		USART_RTS	—	—	—	—	—
56		USART_TXD	I2C_SCL	I2S_WS	SPI_MISO	—	ENET_MDC
57		USART_RXD	I2C_SDA	I2S_DAT	SPI_MOSI	—	ENET_MDIO
58	—	—	—	—	—	—	ENET_TX_DATA0
59		—	—	—	—	—	ENET_TX_DATA1
60		—	—	—	—	—	ENET_TX_EN
61		—	—	—	—	—	ENET_TIMER1
62		—	—	—	—	—	ENET_RX_EN
63		—	—	—	—	—	ENET_RX_ER

9.3 PCB stack-up

- Ensure the stack-up is symmetrical.
- Ensure that all layers meet specified thickness.
- For TFBAG and WLCSP packages, the NXP reference design PCB typically consists of six layers with FR4 material and blind buried vias.

Figure 36 shows the typical six-layer PCB stack-up for TFBGA and WLCSP packages.

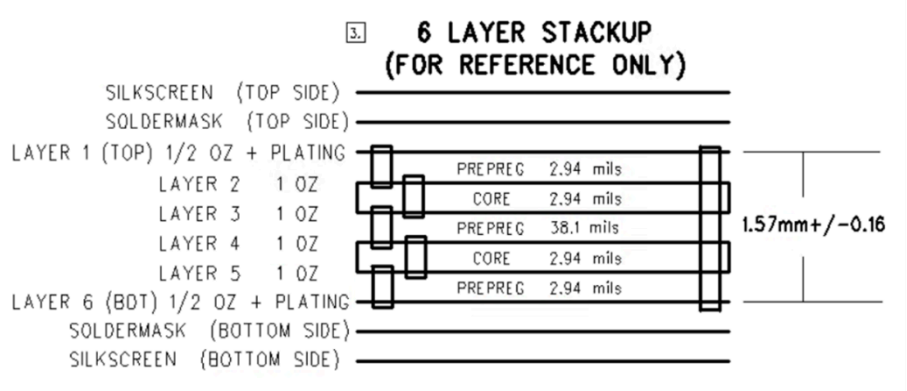

Figure 36. PCB stack-up - WLCSP package

- For HVQFN package, NXP reference design PCB can be of four to six layers with FR4 material and plated through hole vias.

Figure 37 shows the typical six-layer PCB stack-up for HVQFN package.

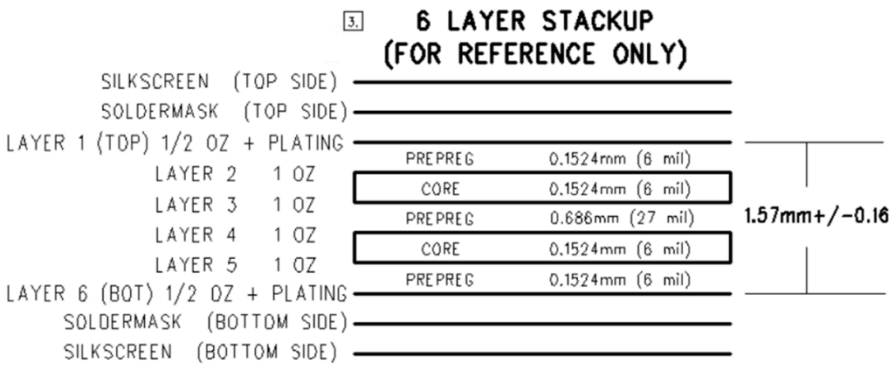

Figure 37. PCB stackup - QFN package

- In general, RF routing is on the top layer with RF trace, and the reference ground is on layer 2.

9.4 Design review rules

To discuss design options and schedule a design review, contact your NXP representative. For a design review, follow these rules:

- File format for the schematic: PDF
- File format for the layout: PADs or Allegro
- Gerber files: not supported or reviewed
- PCB layer stack and thickness: provide the information

10 Debug interface

Serial wire debug (SWD) is the debug interface designed specifically for the micro debugging of processors.

Joint test action group (JTAG) is designed for device and board testing.

The JTAG/SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

10.1 SWD

Table 19. Recommendations for SWD signals

Signal	Recommendation
SWCLK	External 10 kΩ pull-up resistor.
SWDIO	External 10 kΩ pull-up resistor.
SWO	This is an optional pin only used for console and tracing purposes. Routing is optional.

10.2 JTAG

Connect the JTAG signals to test points in the PCB design.

Table 20. Recommendations for JTAG signals

Signal	Recommendation
JTAG_TCK	External 100 kΩ pull-up resistor.
JTAG_TDI	External 100 kΩ pull-up resistor.
JTAG_TDO	Do not use external pullup or pulldown resistors
JTAG_TMS	External 100 kΩ pull-up resistor.
JTAG_nTRST	External 100 kΩ pull-down resistor.

11 References

[1] Data sheet – RW610: Wireless MCU with Integrated Wi-Fi 6 and Bluetooth Low Energy (link)

[2] Data sheet – RW612: Wireless MCU with Integrated Tri-radio Wi-Fi 6 + Bluetooth Low Energy / 802.15.4 – Data sheet (link)

12 Revision history

Revision history

Rev	Date	Description
AN14002 v.2.0	1 November 2024	• Changed the access to public. No changes in the content.
AN14002 v.1.0	18 July 2023	• Initial version

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