AN14057

4:1 switched capacitor charger

Rev. 1.2 — 12 November 2024 Application note

Document information

Information	Content
Keywords	4:1 switched capacitor charger
Abstract	PCA9485 is a highly-integrated switched-capacitor converter with an embedded OVPFET and dual external FET controls, targeted to provide the quadruple output current for the fast charging applications with a 1-cell battery.

1 Introduction

Switched-capacitor (SC) direct charging has been recognized as a good replacement for inductor-based charging, because of its higher efficiency and lower heat dissipation. Fast direct chargers have become mandatory in many mobile devices.

PCA9485UK is a highly integrated switched-capacitor charger with an embedded OVPFET and dual external FET controls, targeted to provide the quadruple output current for the fast charging applications with a 1-cell battery. The device works in 4:1 switching operation with a very high efficiency (around 97 %, at V_{VOUT} = 4.5 V, I_{VOUT} = 8 A), in 1:4, 2:1 and 1:2 switching operation or in 1:1 mode with forward and reverse direction.

As absolute maximum voltage for each VUSB, VWPC, VIN, and VOUT, VUSB/VWPC inputs are designed to support up to 35 V, VIN input supports up to 27 V with the prebias enabled for USB VBUS/wireless receiver output, and VOUT input is designed to support up to 7 V with the prebias enabled for a 1-cell battery application.

The device provides multiple safety schemes such as overcurrent (OC), reverse current (RC), overvoltage (OV), undervoltage (UV), switching pin short, thermal shutdown and others.

PCA9485UK also has a leader-follower function built in that allows two PCA9485s to be used seamlessly in handheld applications.

The device features complete I^2C interface functionality, with up to 1 MHz speed.

2 PCA9485UK charging application

2.1 65 W charging application

For 65 W charging, input voltage of 4:1 switched capacitor charger should be 4 times higher than output voltage to achieve the max 13 A output current.

PCA9485UK is placed in parallel with an inductor-based switching charger that is operated when the USB PD controller cannot adjust input voltage and current in a dead battery case such as a fully discharged battery case. In this case, a mobile device's AP or a microcontroller could not start up to control the USB PD.

External FETs between VBUS/VWPC and VIN could be the replacement of OVP IC, depending on the application requirement. Silicon based NMOS or GaN NMOS for single or back-to-back can be selected.

An example of the charging block is shown in Figure 1.

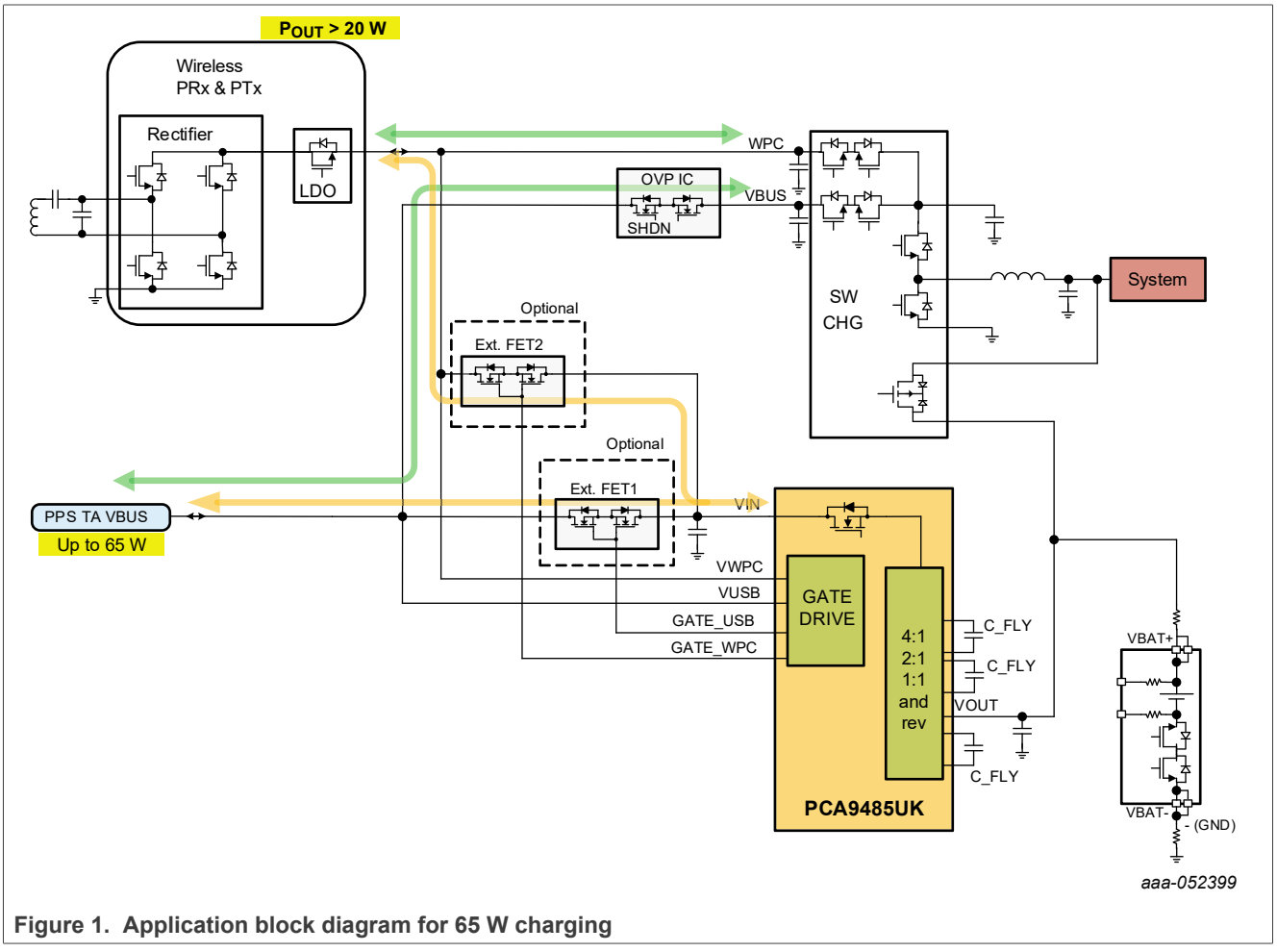

Figure 1. Application block diagram for 65 W charging

2.2 Guidance for mode transition from reverse mode (1:4, 1:2, and R1:1 SW mode) to shutdown/standby state

When changing status from reverse mode (1:4, 1:2, and R1:1) to shutdown state by setting SC OPERATION_MODE_DISABLE bit as 1'b, PCA9485 requires typical 600 µs to discharge flying cap to VOUT through SW4. During this time period, there is current path seen from VOUT to VIN through body diodes of SW4, SW3, SW2, and SW1 even if switching stops.

If there is a load resistor still connected to VIN during this transition time from reverse to shutdown state, it is recommended to use an external FET and control the external FET turned off before setting SC OPERATION_MODE_DISBALE bit as 1’b in order to block reverse current from VOUT to VIN.

2.3 Guidance for enabling/disabling SC OPERATION

When enabling/disabling SC OPERATION for 4:1, 2:1, 1:2, and 1:4 SW mode, FSW_CFG[3:0] setting should be static.

For example, if SC OPERATION for 4:1, 2:1, 1:2 or 1:4 SW mode starts with 1 MHz frequency by setting SC_CNTL_0 (Address: 0x22h) as 0x08h (SC_OPERATION_MODE_DISABLE: 0b and FSW_CFG[3:0]: 1000b), when disabling SC operation for 4:1, 2:1, 1:2 or 1:4 SW mode, SC_CNTL_0 (Address: 0x22h) should be set as 0x88h (SC_OPERATION_MODE_DISABLE: 1b and FSW_CFG[3:0]: 1000b).

Frequency should be kept as an initial value when disabling SC_OPERATION by setting SC_OPERATION_MODE_DISABLE bit as 1b.

3 PCA9485UK reference schematic

3.1 Reference schematic with external FETs controlled by PCA9485UK

The diagram below shows a recommended schematic of top level connection with all necessary peripheral devices for 1-cell battery. PCCA9485UK provides different number of flying capacitor connections at CP1A and CP1B as described in Figure 2. A number of flying capacitors can be adjusted to max output power and device's target efficiency.

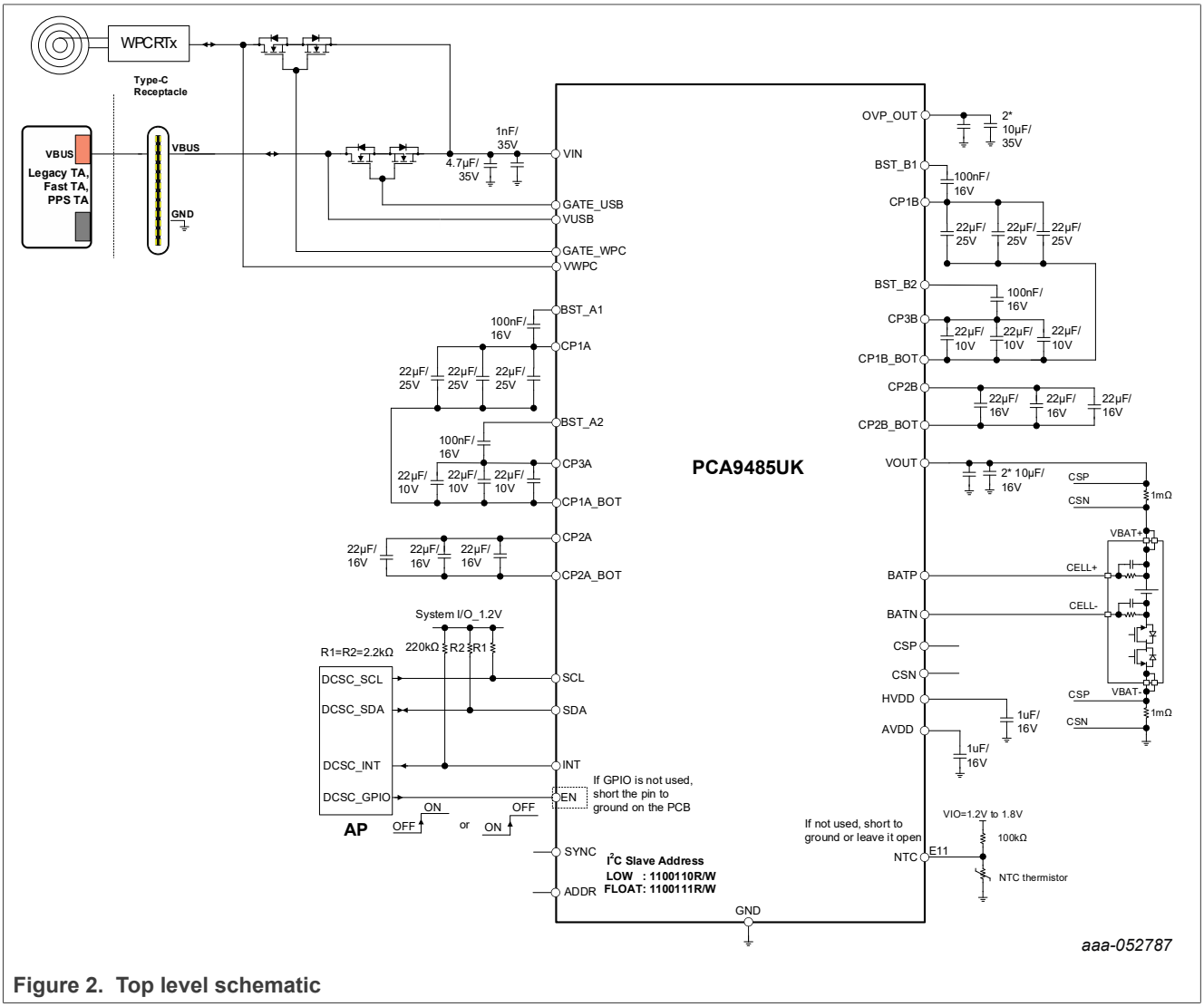

Figure 2. Top level schematic

3.2 Input capacitor selection

In switched capacitor converter application, large AC currents flow through the input/output capacitors. A capacitor should be considered to flow the RMS current. Low ESR ceramic capacitors are highly recommended for this application. Large size X7R MLCC capacitors are normally recommended. Capacitance derating needs to be considered at a DC bias voltage.

3.3 Flying capacitor selection

Large AC currents flow through the flying capacitors. Low ESR ceramic capacitors are highly recommended for this application. The flying capacitor must be selected to accommodate the maximum load current. Large size X7R MLCC capacitors are normally recommended. Capacitance derating needs to be considered at a DC bias voltage.

3.4 Output capacitor selection

A large AC currents flow through the flying capacitors and input/output capacitors. The average output current is given by the formula below.

IOUT = 2 x Frequency x CFLY x ΔVCFLY

The total output voltage ripple is:

$$\frac{I_{OUT}}{2 \times frequency \times \left(C_{FLY} + C_{OUT}\right)}$$

A voltage ripple at CVOUT should be determined by system requirement.

4 Bill of material (BOM)

Table 1 shows all the components for the device.

Table 1. Bill of material

Name	Value	Size (L x W x H mm)	Part Name / Maker	Note
C_{VIN}	4.7µF/35V	1.6 x 0.8 x 0.8	CL10A475KL8NRN	
C_{VIN_IN}	1nF/35V	0.6 x 0.3 x 0.33	GRM033R71H102KA12	For high frequency filter
C_{OVP_OUT}	10µF/35V	1.6 x 0.8 x 0.8	CL10A106ML8NRN	
C_{FLY1}	22µF/25V	2.0 x 1.25 x 1.25 or 1.6 x 0.8 x 0.8	GRM21BR61E226ME44 or GRM188C61E226ME01	Place three or four capacitors.
C_{FLY2}	22µF/16V	1.6 x 0.8 x 0.7	CL10A226MO7FZN	Place three capacitors.
C_{FLY3}	22µF/10V	1.6 x 0.8 x 0.8	CL10A226MP8NUN	Place three capacitors.
C_{BST}	100nF/16V	0.6 x 0.3 x 0.3	GRM033R61C104KE14	Place one capacitor
C_{VOUT}	22µF/10V	1.6 x 0.8 x 0.8	CL10A226MP8NUNE	Place two capacitors. C_{EFF}=5µF at 4.5V
C_{AVDD}	1µF/6.3V	0.6 x 0.3 x 0.3	GRM033D70J105ME01	Place one capacitor. C_{EFF}=0.88µF at 1.5V
C_{HVDD}	1µF/10V	0.6 x 0.3 x 0.3	GRM155C71A105ME11	Place one capacitor.
R_{SENSE}	1mΩ/2mΩ			Place if external current sense is needed for battery current
R_{I2C_PULLUP}	2.2kΩ	0.6 x 0.3 x 0.28		Each on SCL and SDA
R_{nINT_PULLUP}	220kΩ	0.6 x 0.3 x 0.28		
NTC		0.6 x 0.3 x 0.28		Place it if needed
External N-ch FET		2.1 x 2.1 x 0.344 2.05 x 2.05 x 0.75	GaN FET INN040W048AQ1 CMOS FET NVLJWS6D0N04CL	

5 Layout guides

5.1 PCB layout guidelines

The device has a dual phase converter with nine flying capacitors on each phase. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Utilize 8-layer board for optimal layout, and assign one layer as solid ground plane near the device to minimize high-current path
2. Place flying capacitors as close to the relevant bumps as possible. The trace shall be wide enough to carry the charging and discharging current and to minimize trace resistance which affects efficiency directly.
3. Place output capacitor as close as possible to VOUT bumps. Use as wide as possible on the top layer to VOUT bumps of each phase.
4. Input capacitors as close as possible to VIN and OVP_OUT. Should be careful to have symmetrical traces from VIN capacitor to VIN bumps of each phase. VOUT_OUT capacitors should be placed symmetrically as well to avoid unbalanced current distribution on both phases.
5. Decoupling capacitors shall be placed next to the device and make trace connection as short as possible
6. Ensure that there are sufficient thermal vias directly under bumps of the power FETs, power ground, connecting to copper on other layers

Figure 3. Recommended top-layer PCB layout

6 Revision history

Table 2. Revision history

Document ID	Release date	Description
AN14057 v.1.2	12 November 2024	• Added Section 2.3 • Section 4: Updated C_{FLY1}
AN14057 v.1.1	13 May 2024	• Added Section 2.2
AN14057 v.1.0	20 September 2023	• Initial version

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