AN14183

FS2400 product guidelines

Rev. 2.0 — 8 November 2024 **Application note**

Document information

Information	Content
Keywords	Fail-safe system basis chip (SBC), SMPS, LDO, CAN FD transceiver, ultra-wide band (UWB), near-field communication (NFC), Bluetooth Low Energy (BLE) devices, small applications, low power, functional safety, ISO pulses, non-ISO pulses, electromagnetic compatibility (EMC), external components, SPI, hardware
Abstract	This application note provides product guidelines and performance results (ISO pulses, EMC …) for the FS2400 system basis chip family in automotive electronic systems.

1 Introduction

1.1 FS24 safety system basis chip with low power and fit for ASIL B

The FS2400 is a family of automotive safety system basis chip (SBC) devices with multiple power supplies designed to support secure car access applications using ultra-wide band (UWB), near-field communication and Bluetooth Low Energy (NFC-BLE) devices, while maintaining flexibility to fit other small applications requiring low power and CAN FD communication.

This family of devices supports a wide range of applications, offering a choice of output-voltage settings, physical interfaces, and integrated system-level features to address low-power and noise-sensitive applications with automotive safety integrity levels (ASIL) up to ASIL B.

The FS2400 integrates a battery-connected switched-mode regulator (V1) and a battery-connected linear regulator (V3) to supply the microcontroller, communication devices, and other devices . V1 offers a high-performance switching regulator capable of operating in pulse frequency modulation (PFM) mode and forced pulse width modulation (FPWM) mode. The mode of operation can be changed using wake pins to optimize noise management.

The FS2400 is developed in compliance with the ISO 26262:2018 standard. The FS2400 includes enhanced safety features with a fail-safe output, becoming part of a full safety-oriented system, covering ASIL B.

The FS2400 is offered in a 5 mm x 5 mm 32-Ld HVQFN package with wettable flanks.

Operating range

- 40 V DC maximum input voltage.
- Low-power off mode with low-sleep current and multiple wake-up sources.
- Low-power on mode with HVBUCK (V1) active, HVLDO (V3) selectable by OTP and multiple wake-up sources.

1.2 Applications

- UWB anchors
- NFC anchors
- BLE anchors
- Combo anchors (UWB and BLE)
- UWB radar
- All small applications requiring low power and CAN FD
- UWB master anchors

2 Simplified diagram

Figure 1 shows a simplified block diagram for a typical system with an FS2400.

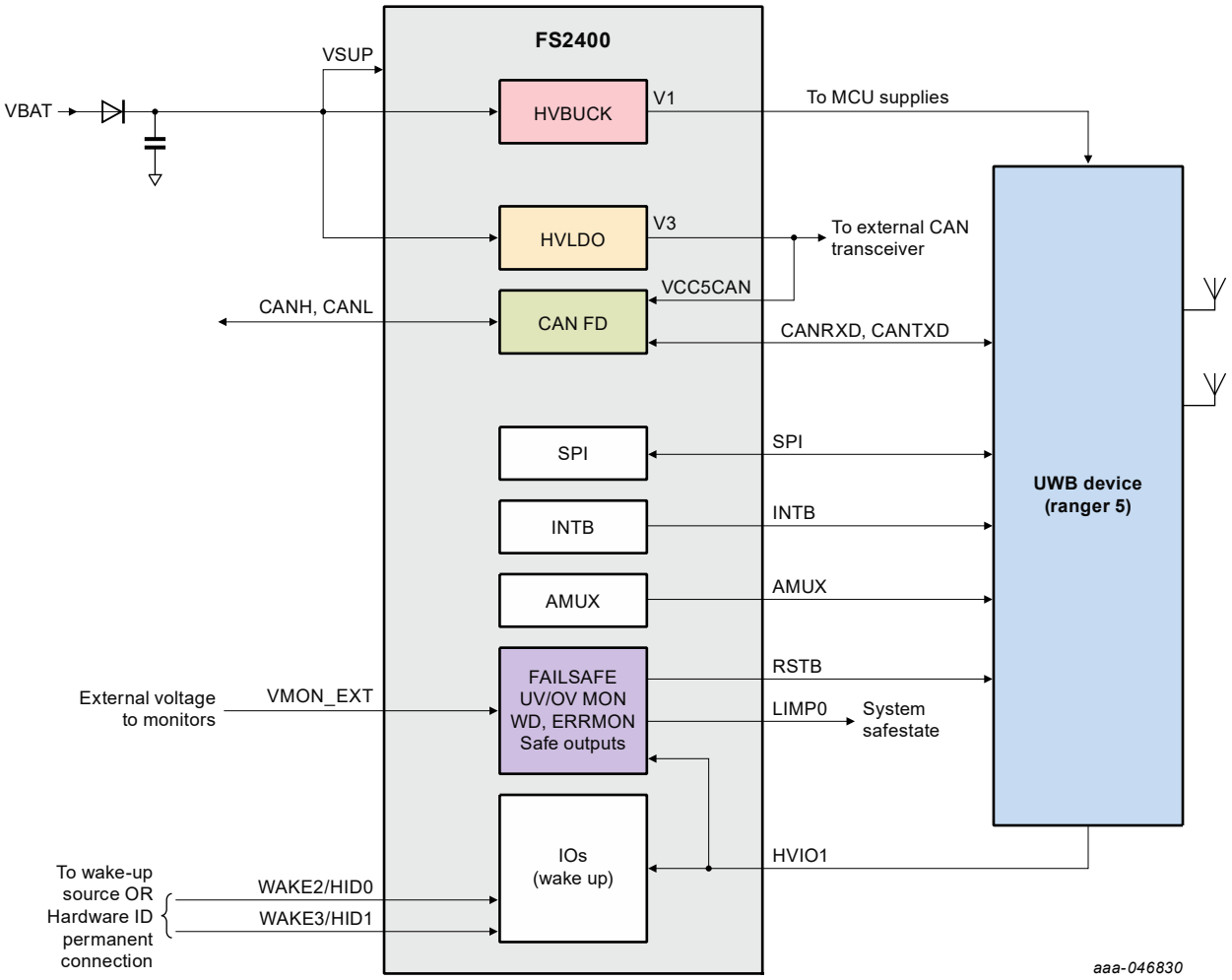

Figure 1. Application diagram

3 Application external components

All external components must be automotive grade, AEC-Q100 (for IC chips), AEC-Q101 (for discrete components), and AEC-Q200 (for passive components).

3.1 VBAT/VSUP components

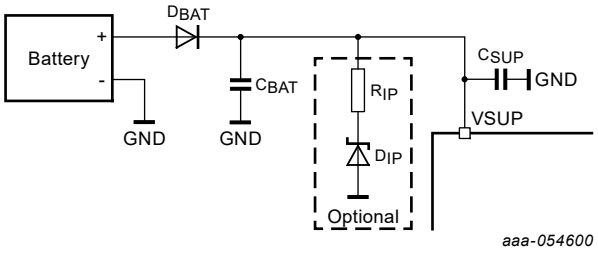

Figure 2. VBAT/VSUP components

Table 1. VBAT/VSUP components description

Components	Description
D_{BAT}	Reverse battery diode protection • Low $V_{FORWARD}$ to minimize the losses • $I_{Forward}$ > 2x maximum input current • $V_{Reverse}$ ≥ 30 V
R_{IP}	Optional component to sustain ISO pulses (slow and fast positive transients) in Low-power modes (only needed if the application requires it) • Resistor 1 kΩ - 0.25 W minimum
D_{IP}	Optional component to sustain ISO pulses (slow and fast positive transients) in Low-power modes (only needed if the application requires it) • 30 V Zener diode
C_{BAT}	• 10 µF nominal ceramic capacitor or more • Minimum voltage rating: 50 V
C_{SUP}	• 100 nF decoupling capacitor, close to the pin • Minimum voltage rating: 50 V

3.2 V1 - HVBUCK regulator

3.2.1 V1 - HVBUCK external components

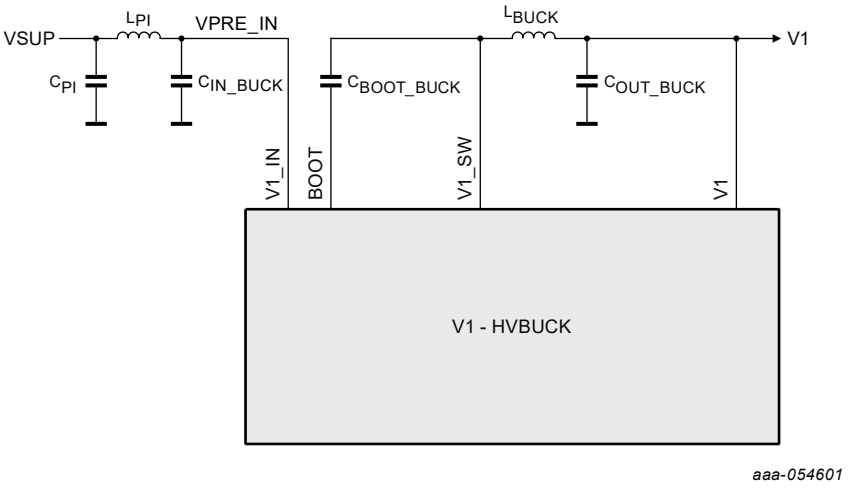

Figure 3. V1 - HVBUCK components

Table 2. V1 - HVBUCK components description

Components	Description
C_{IN_BUCK}	FSW_BUCK = 2.2 MHz: • 4.7 uF nominal decoupling capacitor, close to the pin FSW_BUCK = 450 kHz: • 10 uF nominal decoupling capacitor, close to the pin • Minimum voltage rating: 50 V
L_{PI}	FSW_BUCK = 2.2 MHz: • L_{BUCK} = 1 µH nominal FSW_BUCK = 450 kHz: • L_{BUCK} = 4.7 µH nominal Soft saturation recommended.
C_{BOOT_BUCK}	• Bootstrap capacitor 33 nF nominal • Minimum Voltage rating: 16 V
L_{BUCK}	FSW_BUCK = 2.2 MHz: • L_{BUCK} = 4.7 µH nominal • I_{SAT} > $I_{OC\_PK\_PWM}$ Max* + 20 % FSW_BUCK = 450 kHz: • L_{BUCK} = 22 µH nominal • I_{SAT} > $I_{OC\_PK\_PWM}$ Max* + 20 % * Use $I_{OC\_PK\_PWM}$ maximum value for calculation (refer to the FS2400 data sheet) Soft saturation recommended. ISAT value here is to consider the case of V1 overload (or fault, such as short circuit) and IPRE being limited by current limit feature ILIM_PRE. Shielded, ±20 % tolerance is preferred, but ±30 % is allowed.

Table 2. V1 - HVBUCK components description...*continued*

Components	Description
C_{OUT_V1}	FSW_BUCK = 2.2 MHz: • 10 µF nominal is recommended for 2 V, 2.5 V, and 3.3 V. Minimum effective capacitance is 6.5 µF (derating vs DC bias and temperature included). • 2 x 10 µF nominal is recommended for 5 V. Minimum effective capacitance is 13 µF (derating vs DC bias and temperature included). FSW_BUCK = 450 kHz: • 4 x 10 µF nominal is recommended for 2 V, 2.5 V, and 5 V. Minimum effective capacitance is 25 µF (derating vs DC bias and temperature included). • 5 x 10 µF nominal is recommended for 3.3 V. Minimum effective capacitance is 25 µF (derating vs DC bias and temperature included). Minimum voltage rating: 2 x V1 output voltage (3 x V1 output voltage is preferred to minimize DC bias derating)

3.3 V3 - HVLDO regulator

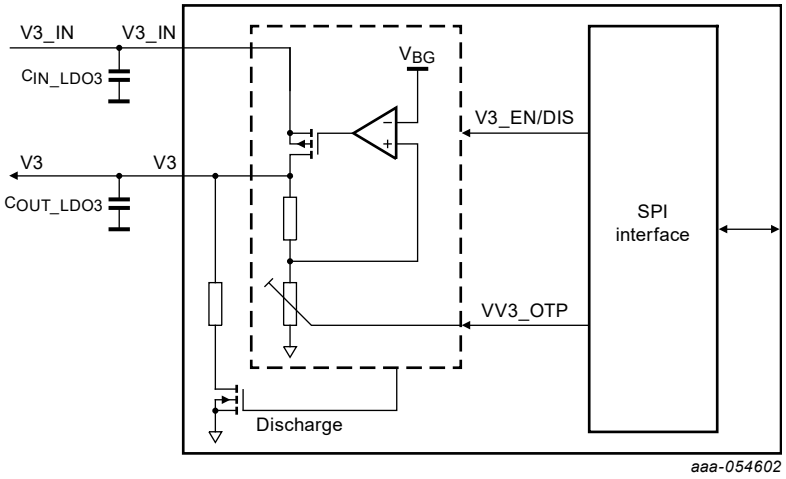

Figure 4. V3 – HVLDO components diagram

Table 3. V3 - HVLDO components description

Component	Description
C_{IN_LDO3}	• 1 µF nominal close to V3_IN pin • Minimum voltage rating: 50 V
C_{OUT_LDO3}	• Minimum effective capacitance is 1.3 µF (derating vs DC bias temperature included). Recommended nominal capacitance value is 2.2 µF. • Minimum voltage rating: 2 x V3 output voltage (3 x V3 output voltage is preferred to minimize DC bias derating)

3.4 WAKE/HID and HVIO pins

3.4.1 Configuration as global input

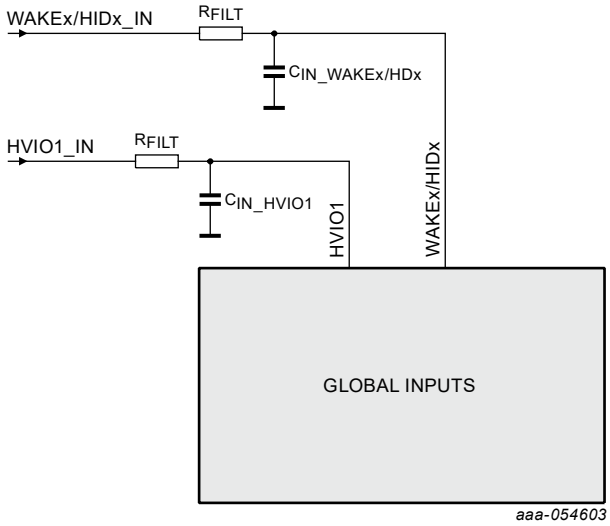

Figure 5. Global inputs components diagram

When configured as global, WAKEx/HIDx pins can either be used as wake-up sources or as a hardware identification (HID) solution. In the HID case, the pin is permanently connected to either VBAT, GND, or a floating node.

Table 4. Global inputs components description

Component	Description
$C_{IN\_WAKEx/HIDx}$	**For WAKEx use case:** Decoupling capacitor close to the pin for immunity • –22 nF nominal value • Minimum voltage rating: 50 V **For HIDx use case:** Decoupling capacitor close to the pin for immunity • –100 nF nominal value • Minimum voltage rating: 50 V
C_{IN_HVIO1}	**For HVIO1:** • –10 nF nominal value • Minimum voltage rating: 50 V
R_{FILT}	**For WAKEx and HVIO1 use cases:** Series resistor to limit the input current • –5.1 kΩ nominal value **For HIDx use case:** • –220 Ω nominal value

Note: *In the case of ground loss of the module, there is a possibility (if HIDx is connected to GND) that the current flows through the HIDx pin. In that case, the current through R_{FILT} creates a ground-shift voltage equal to I_{SUP}*R_{FILT}. In most cases, if the shift is significant enough, the device goes directly in Fail-safe state because of the V_{BOS_UV} triggered.*

3.4.2 Configuration as local input

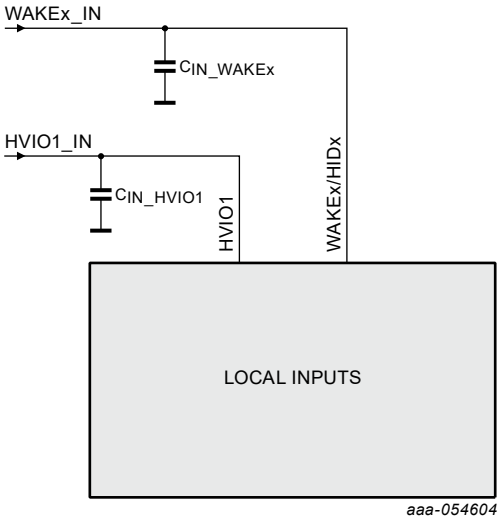

Figure 6. Local input components diagram

When configured as local, WAKEx/HIDx pins can only be used as wake-up sources.

Table 5. Local inputs components description

Component	Description
C_{IN_WAKEx} C_{IN_HVIO1}	Decoupling capacitor close to the pin for immunity • –10 nF nominal value • Minimum voltage rating: 50 V

3.4.3 Configuration as local output

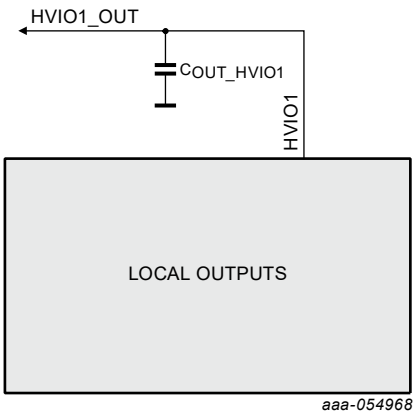

Figure 7. Local output components diagram

Table 6. Local output components description

Component	Description
C_{OUT_HVIO1}	Decoupling capacitor close to the pin for immunity • –10 nF nominal value • Minimum voltage rating: 2 x HVIO1 output voltage (3 x HVIO1 output voltage is preferred to minimize DC bias derating) ***Note:*** *HVIO1 output voltage depends on HVIO1_PU_SEL_OTP bit configuration.*

3.5 Functional safety pins

3.5.1 LIMP0: Configuration as global output

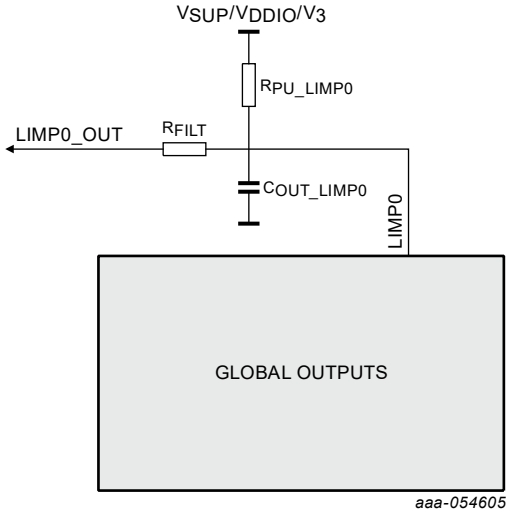

Figure 8. LIMP0 global components diagram

Table 7. LIMP0 global components description

Component	Description
C_{OUT_LIMP0}	Decoupling capacitor close to the pin for immunity • –10 nF nominal value • Minimum voltage rating: 50 V
R_{FILT}	Series resistor to limit the input current • **LIMP0 as a safety output use case:** 5.1 kΩ nominal value • **LIMP0 as a HW ID pin use case:** 220 Ω nominal value
R_{PU_LIMP0}	**LIMP0 as a safety output use case:** Pullup resistor to either VDDIO or VSUP[1] • –10 kΩ nominal value if pulled up to VSUP • –5.1 kΩ nominal value if pulled up to VDDIO **LIMP0 as a HW ID pin use case:** • Pullup resistor to either V3 or VDDIO • Resistor sized for between 1.5 mA and 4 mA nominal current[2]

[1] In Low-power mode, if LIMP0 is asserted, the pin will drain a continuous current from the pullup source.
[2] Current between the pullup source and LIMP0_OUT, when LIMP0 is released and LIMP0_OUT connected to GND + 1 V

3.5.2 LIMP0: Configuration as local output

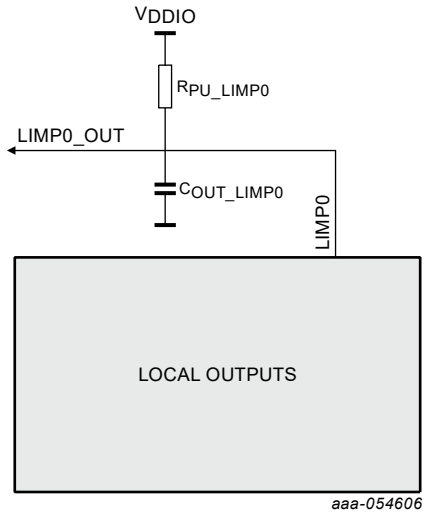

Figure 9. LIMP0 local components diagram

Table 8. LIMP0 local components description

Component	Description
C_{OUT_LIMP0}	Decoupling capacitor close to the pin for immunity • 10 nF nominal value • Minimum voltage rating: 50 V
R_{PU_LIMP0}	Pullup resistor to either VDDIO or VSUP[1] • 10 kΩ nominal value if pulled up to VSUP • 5.1 kΩ nominal value if pulled up to VDDIO

[1] In Low-power mode, if LIMP0 is asserted, the pin will drain a continuous current from the pullup source.

3.5.3 RSTB: Configuration as local output

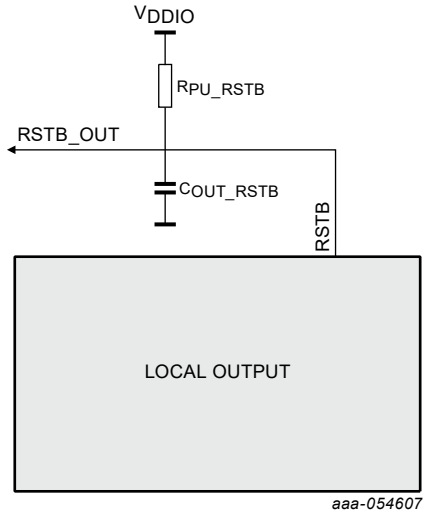

Figure 10. RSTB local components diagram

Table 9. RSTB local components description

Component	Description
C_{OUT_RSTB}	Decoupling capacitor close to the pin for immunity • 1 nF nominal value • Minimum voltage rating: 2 x VDDIO voltage (3 x VDDIO voltage is preferred to minimize DC bias derating)
R_{PU_RSTB}	Pullup resistor to VDDIO • 5.1 kΩ nominal value

3.5.4 INTB: Configuration as local output

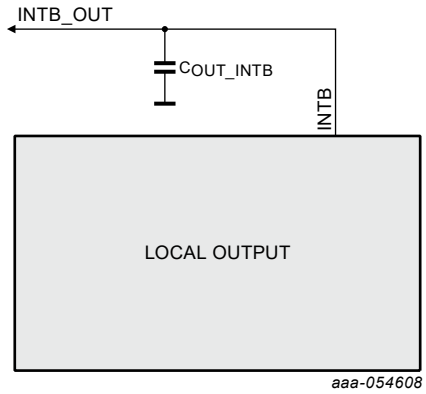

Figure 11. INTB local components diagram

Table 10. INTB local components description

Component	Description
C_{OUT_INTB}	Decoupling capacitor close to the pin • 1 nF nominal value (10 nF can be used for conductive immunity requirements. In this case, an external pullup resistor can be used to reduce the rising time of the pin) • Minimum voltage rating: 2 x VDDIO voltage (3 x VDDIO voltage is preferred to minimize DC bias derating)

3.6 CAN pins

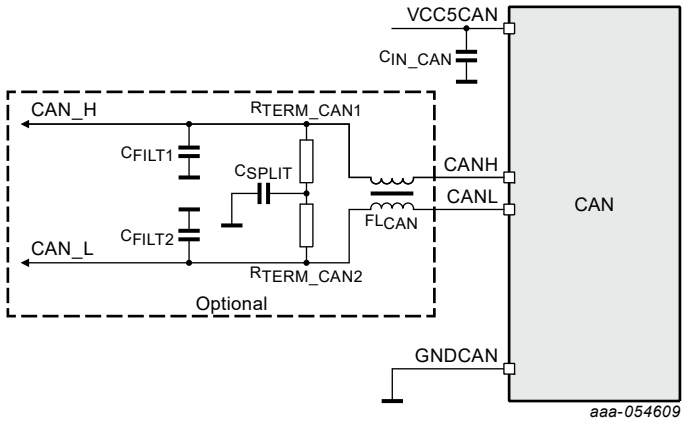

Figure 12. CAN components diagram

Table 11. CAN components description

Component	Description
C_{IN_CAN}	Decoupling capacitor close to the pin for immunity • 100 nF nominal value • Minimum voltage rating: 16 V
FL_{CAN} (Optional)	Common mode choke for noise filtering (Depends on system requirements) • 100 uH @ 100 kHZ nominal value
R_{TERM_CANx} (Optional)	CAN termination resistors • 2 x 60 Ω nominal value or 1 x 120 Ω if C_{SPLIT} is not used. The goal is to have a total resistance of 60 Ω on the CAN bus. (An additional 120 Ω resistor must be populated on another CAN node). • Power rating: 0.5 W total to support short circuit conditions
C_{SPLIT} (Optional)	Filtering capacitor depending on system requirements • 4.7 nF nominal value
C_{FILTx} (Optional)	Filtering capacitor depending on system requirements • 100 pF nominal value

4 Bill of materials (BOM)

4.1 Application schematic used for HVBUCK @ 2.2 MHz

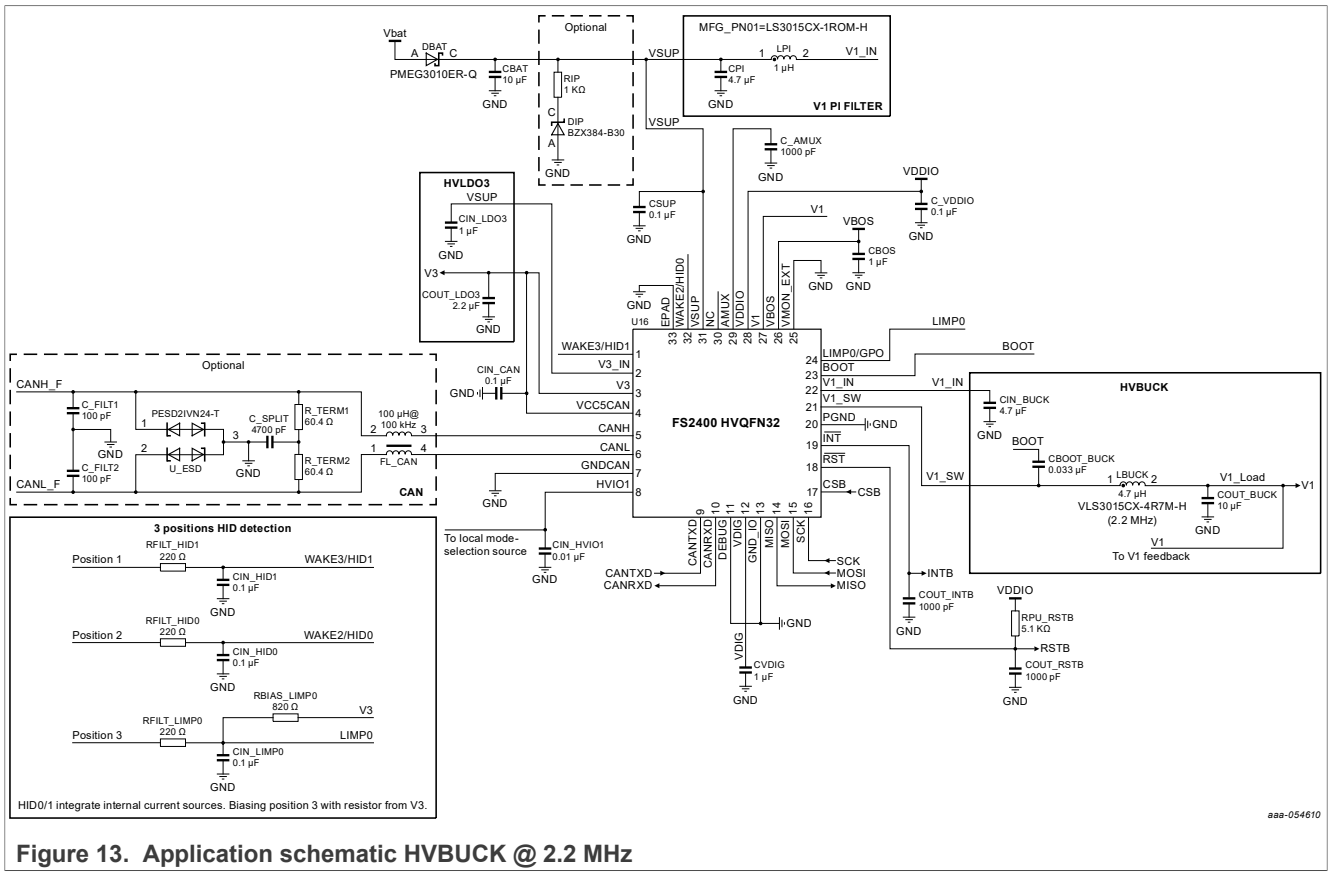

Figure 13. Application schematic HVBUCK @ 2.2 MHz

4.2 BOM for HVBUCK switching frequency at 2.2 MHz

Table 12. BOM reference for HVBUCK @ 2.2 MHz

Reference	Quantity	Description	Vendor	Part number	Value
CBAT	1	CAP CER 10uF 50 V 10 % X7S AEC-Q200 1210	TDK	CGA6P3X7S1H106K250AE	10 µF
DBAT	1	DIODE SCH PWR RECT 1 A 30 V AEC-Q101 SOD123W	NEXPERIA	PMEG3010ER, 115	NA
RIP	1	RES MF 1K 1/10 W 5 % AEC-Q200 0603	VISHAY INTERT ECHNOLOGY	CRCW06031K00JNEA	1 kΩ
DIP	1	DIODE ZNR 30 V 300 mW AEC-Q101 SOD323	NEXPERIA	BZX384-B30, 115	NA
CSUP	1	CAP CER 0.1 uF 50 V 10 % X7R AEC-Q200 0603	TDK	CGA3E2X7R1H104K080AA	0.1 µF
CPI, CIN_BUCK	2	CAP CER 4.7 uF 50 V 10% X7R AEC-Q200 1206	TDK	CGA5L3X7R1H475K160AB	4.7 µF
LPI	1	IND FER 1 uH @ 1 MHz 2.96 A 0.038 OHM 20 % AEC-Q200 SMT	TDK	VLS3015CX-1R0M-H	1 µH
CBOOT_BUCK	1	CAP CER 0.033 UF 16 V 10 % X7R AEC-Q200 0402	TDK	CGA2B2X7R1C333K050BA	0.033 µF

Table 12. BOM reference for HVBUCK @ 2.2 MHz*...continued*

Reference	Quantity	Description	Vendor	Part number	Value
LBUCK	1	IND FER 4.7 uH @ 1 MHz 1.7 A 0.12 OHM 20 % AEC-Q200 SMT	TDK	VLS3015CX-4R7M-H	4.7 µH
COUT_BUCK	1	CAP CER 10 uF 10 V 10 % X7S AEC-Q200 0805	TDK	CGA4J3X7S1A106K125AB	10 µF
CIN_LDO3	1	CAP CER 1.0 uF 50 V 10 % X7R AEC-Q200 0805	TDK	CGA4J3X7R1H105K125AB	1 µF
COUT_LDO3	1	CAP CER 2.2 uF 16 V 10 % X7R AEC-Q200 0805	TDK	CGA4J3X7R1C225K125AB	2.2 µF
CIN_CAN, C_VDDIO	2	CAP CER 0.1 uF 16 V 10 % X7R AEC-Q200 0402	MURATA	GCM155R71C104KA55D	0.1 µF
FL_CAN	1	FILTER COMMON MODE 100 uH @ 100 KHZ 150 mA 30 % AEC-Q200 SMT	TDK	ACT1210-101-2P-TL00	100 µH @ 100 kHz
R_TERM1, R_TERM2	2	RES MF 60.4 OHM 1/4 W 1 % AEC-Q200 0603	PANASONIC	ERJ-PA3F60R4V	60.4 Ω
C_SPLIT	1	CAP CER 4700 pF 50 V 5 % C0G AEC-Q200 0603	TDK	CGA3E2C0G1H472J080AA	4700 pF
U_ESD	1	DIODE 2 CH ESD PROTECTOR 30 KV 24 V AEC-Q101 SOT23-3	NEXPERIA	PESD2IVN24-T	NA
C_FILT1, C_FILT2	2	CAP CER 100 pF 100 V 5 % C0G AEC-Q200 0603	MURATA	GCM1885C2A101JA16D	100 pF
RFILT_HID0, RFILT_HID1, RFILT_LIMP0	3	RES MF 220 OHM 1/10 W 5 % 0603	PANASONIC	ERJ-3GEYJ221V	220 Ω
CIN_HID0, CIN_HID1, CIN_LIMP0	3	CAP CER 0.1 uF 50 V 10 % X7R AEC-Q200 0402	MURATA	GCM155R71H104KE02D	0.1uF
RBIAS_LIMP0	1	RES MF 820 OHM 1/10 W 1 % AEC-Q200 0402	KOA SPEER	RK73H1ETTP8200F	820 Ω
CIN_HVIO1	1	CAP CER 0.01 uF 50 V 10 % X7R AEC-Q200 0603	TDK	CGA3E2X7R1H103K080AA	0.01 µf
RPU_RSTB	1	RES TF 5.1 K 1/4 W 5 % AEC-Q200 0603	ROHM	ESR03EZPJ512	5.1 kΩ
C_AMUX, COUT_RSTB, COUT_INTB	3	CAP CER 1000 pF 25 V 5 % C0G AEC-Q200 0402	Murata Electronics	GRT1555C1E102JA02D	1000 pF
CVDIG, CBOS	2	CAP CER 1 uF 16 V 10 % X7R AEC-Q200 0603	TDK	CGA3E1X7R1C105K080AC	1 µF

4.3 Application schematic used for HVBUCK @ 450 kHz

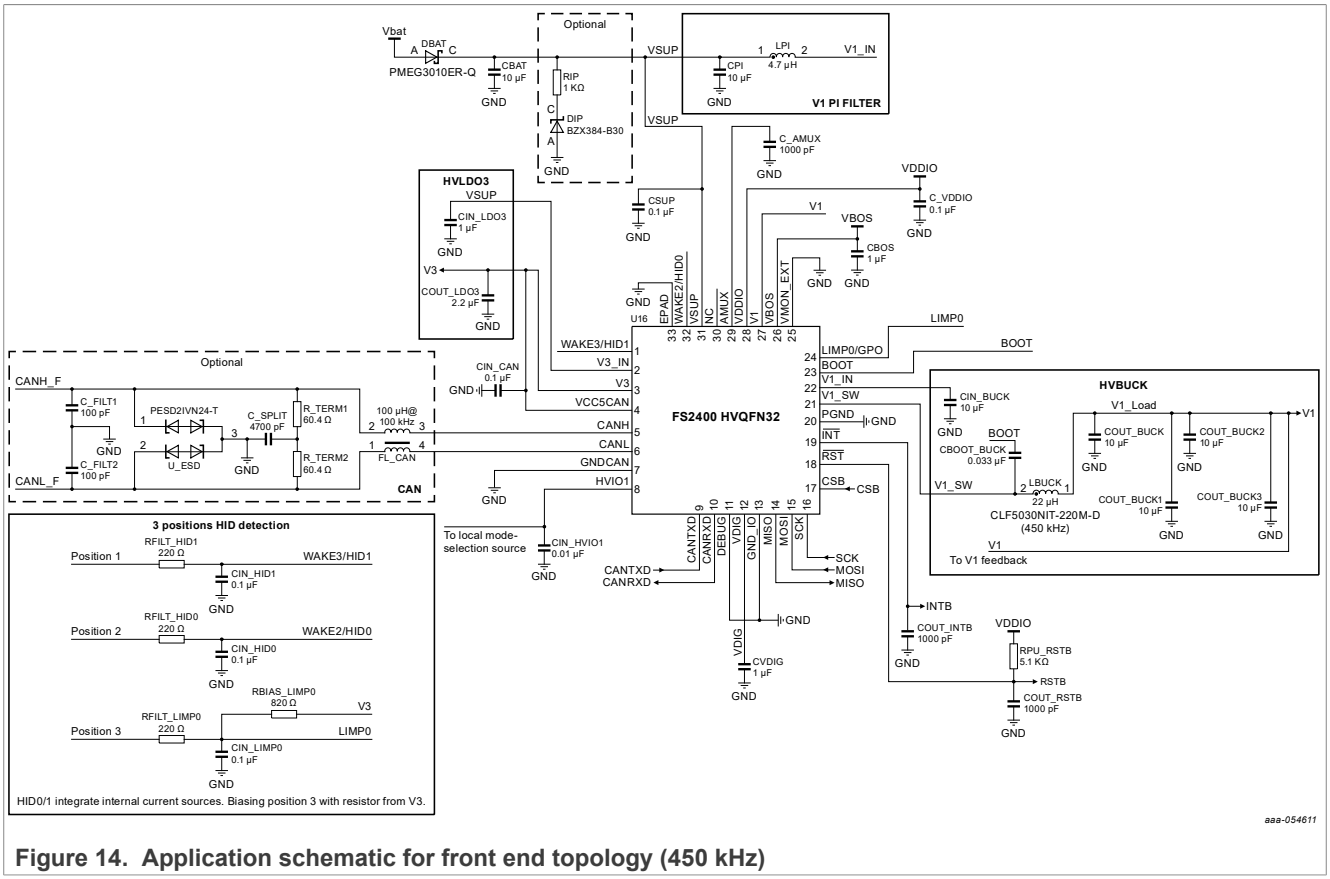

Figure 14. Application schematic for front end topology (450 kHz)

4.4 BOM for HVBUCK switching frequency at 450 kHz

Table 13. BOM reference for HVBUCK @ 450 kHz

Reference	Quantity	Description	Vendor	Part number	Value
CBAT, CPI, CIN_BUCK	3	CAP CER 10 uF 50 V 10 % X7S AEC-Q200 1210	TDK	CGA6P3X7S1H106K250AE	10 µF
DBAT	1	DIODE SCH RECT 30 V 1 A SOD993	NEXPERIA	PMEG3010AESBYL	NA
RIP	1	RES MF 1K 1/10 W 5 % AEC-Q200 0603	VISHAY INTERT ECHNOLOGY	CRCW06031K00JNEA	1 kΩ
DIP	1	DIODE ZNR 30 V 300 mW AEC-Q101 SOD323	NEXPERIA	BZX384-B30,115	NA
CSUP	1	CAP CER 0.1 uF 50 V 10 % X7R AEC-Q200 0603	TDK	CGA3E2X7R1H104K080AA	0.1 µF
LPI	1	IND FER 4.7 uH @ 1 MHz 1.7 A 0.12 OHM 20 % AEC-Q200 SMT	TDK	VLS3015CX-4R7M-H	4.7 µH
CBOOT_BUCK	1	CAP CER 0.033 UF 16 V 10 % X7R AEC-Q200 0402	TDK	CGA2B2X7R1C333K050BA	0.033 µF
LBUCK	1	IND PWR 22 uH @ 100 kHz 1.42 A 20 % AEC-Q200 SMD	TDK	CLF5030NIT-220M-D	22 µH

Table 13. BOM reference for HVBUCK @ 450 kHz*...continued*

Reference	Quantity	Description	Vendor	Part number	Value
COUT_BUCK1, COUT_BUCK2, COUT_BUCK3, COUT_BUCK4	4	CAP CER 10 uF 10 V 10 % X7S AEC-Q200 0805	TDK	CGA4J3X7S1A106K125AB	10 µF
CIN_LDO3	1	CAP CER 1.0 uF 50 V 10 % X7R AEC-Q200 0805	TDK	CGA4J3X7R1H105K125AB	1 µF
COUT_LDO3	1	CAP CER 2.2 uF 16 V 10 % X7R AEC-Q200 0805	TDK	CGA4J3X7R1C225K125AB	2.2 µF
CIN_CAN, C_VDDIO	2	CAP CER 0.1 uF 16 V 10 % X7R AEC-Q200 0402	MURATA	GCM155R71C104KA55D	0.1 µF
FL_CAN	1	FILTER COMMON MODE 100 uH @ 100 KHZ 150 mA 30 % AEC-Q200 SMT	TDK	ACT1210-101-2P-TL00	100 µH @ 100 kHz
R_TERM1, R_TERM2	2	RES MF 60.4 OHM 1/4 W 1 % AEC-Q200 0603	PANASONIC	ERJ-PA3F60R4V	60.4 Ω
C_SPLIT	1	CAP CER 4700 pF 50 V 5 % C0G AEC-Q200 0603	TDK	CGA3E2C0G1H472J080AA	4700 pF
U_ESD	1	DIODE 2 CH ESD PROTECTOR 30 KV 24 V AEC-Q101 SOT23-3	NEXPERIA	PESD2IVN24-T	NA
C_FILT1, C_FILT2	2	CAP CER 100 pF 100 V 5 % C0G AEC-Q200 0603	MURATA	GCM1885C2A101JA16D	100 pF
RFILT_HID0, RFILT_HID1, RFILT_LIMP0	3	RES MF 220 OHM 1/10 W 5 % 0603	PANASONIC	ERJ-3GEYJ221V	220 Ω
CIN_HID0, CIN_HID1, CIN_LIMP0	3	CAP CER 0.1 uF 50 V 10 % X7R AEC-Q200 0402	MURATA	GCM155R71H104KE02D	0.1 uF
RBIAS_LIMP0	1	RES MF 820 OHM 1/10 W 1 % AEC-Q200 0402	KOA SPEER	RK73H1ETTP8200F	820 Ω
CIN_HVIO1	1	CAP CER 0.01 uF 50 V 10 % X7R AEC-Q200 0603	TDK	CGA3E2X7R1H103K080AA	0.01 µf
RPU_RSTB	1	RES TF 5.1 K 1/4 W 5 % AEC-Q200 0603	ROHM	ESR03EZPJ512	5.1 kΩ
C_AMUX, COUT_RSTB, COUT_INTB	3	CAP CER 1000 pF 25 V 5 % C0G AEC-Q200 0402	Murata Electronics	GRT1555C1E102JA02D	1000 pF
CVDIG, CBOS	2	CAP CER 1 uF 16 V 10 % X7R AEC-Q200 0603	TDK	CGA3E1X7R1C105K080AC	1 µF

5 Layout guidelines

The FS2400 integrates multiple functional blocks in a single chip in a way that prevents any functions from disturbing one another. To stay consistent with that, to prevent any external emission or immunity issues and to optimize the function performances, some layout guidelines must be followed while routing the traces between FS2400 components on a printed circuit board (PCB). KITFS2400FRDMEVM rev C board layout can be used as a reference.

5.1 V1 - HVBUCK layout

- V1 – HVBUCK input capacitor is connected as close as possible to the V1_IN pin. The capacitor should be orientated to allow direct connection between the FS2400 PGND pin and the capacitor ground.
- The PGND ground shape should not be connected directly to the top layer's ground (to avoid any coupling of the noise to the battery). It should be connected through vias to an underlying layer (L3)
- V1 – HVBUCK input pi filter should be placed close to the V1_IN pin
- V1 – HVBUCK current loop should be as small as possible with short and wide tracks to optimize regulation loop performances.
- V1 – HVBUCK feedback (connected to V1 pin) line should be shielded by surrounding the trace with GND.
- Connect V1 – HVBUCK feedback close to its output capacitors.
- Place V1 – HVBUCK bootstrap capacitor as close as possible to the FS24 pins.

Figure 15 is an example of a correct layout for HVBUCK. The bootstrap capacitor is placed on the bottom, as this is the closest it can be to the pin with this layout. The trace connecting the V1_SW pin to LBUCK is also routed on the bottom layer.

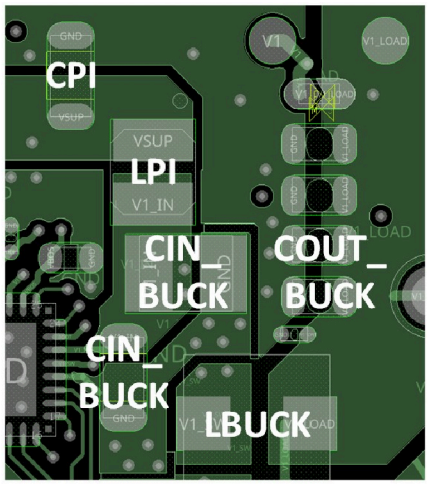

Figure 15. Example of V1 - HVBUCK layout

5.2 CAN layout

- The CAN bus should be routed in differential pairs with 120 Ω impedance.
- The CAN bus should be routed on top.
- The GNDCAN pin should be connected to the FS2400 exposed pad.
- The CAN bus should be shielded with ground planes and ground vias around the traces.

Figure 16 is an example of a correct CAN layout.

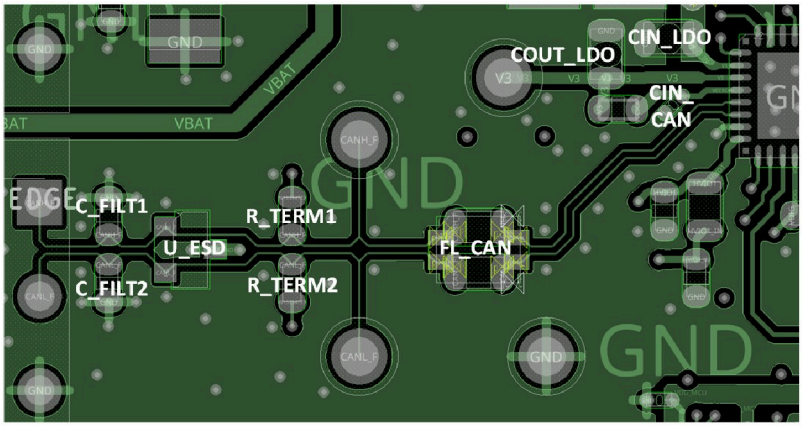

Figure 16. Example of CAN layout

5.3 General guidelines

- Place as many vias as possible below the FS2400 exposed pad (3 x 3 grid minimum).
- The exposed pad should not be directly connected to the different FS2400 GND pins (except GNDCAN).
- If a high-current loop is going through multiple PCB layers, multiple vias are recommended to limit the parasitic resistance and inductance in the high current path.
- When a signal is going through multiple PCB layers, ground vias around the layer interconnection are recommended to contain the electrical field.
- Avoid low-level signals below V1 – HVBUCK power components.
- Connect components with high-impedance signals close to the device pin to avoid noise injection.
- When crossing a sensitive signal with a power trace, have them crossing orthogonally to avoid any coupling.

6 Engineering modes

The FS2400 provides four distinct operation modes (Debug mode, Test mode, OTP mode, and Normal mode) with direct impact on device functionalities. All of these modes can operate in parallel. Understanding these modes helps to use the product properly.

For the first use, it is recommended to start the device in Debug mode. Debug mode disables the watchdog and other functional safety features, making engineering and debugging easier.

The voltage level on the FS2400 DEBUG pin is one condition for entering any given operation mode.

Figure 17 gives an overview of the device modes and actions to do in order to navigate through these.

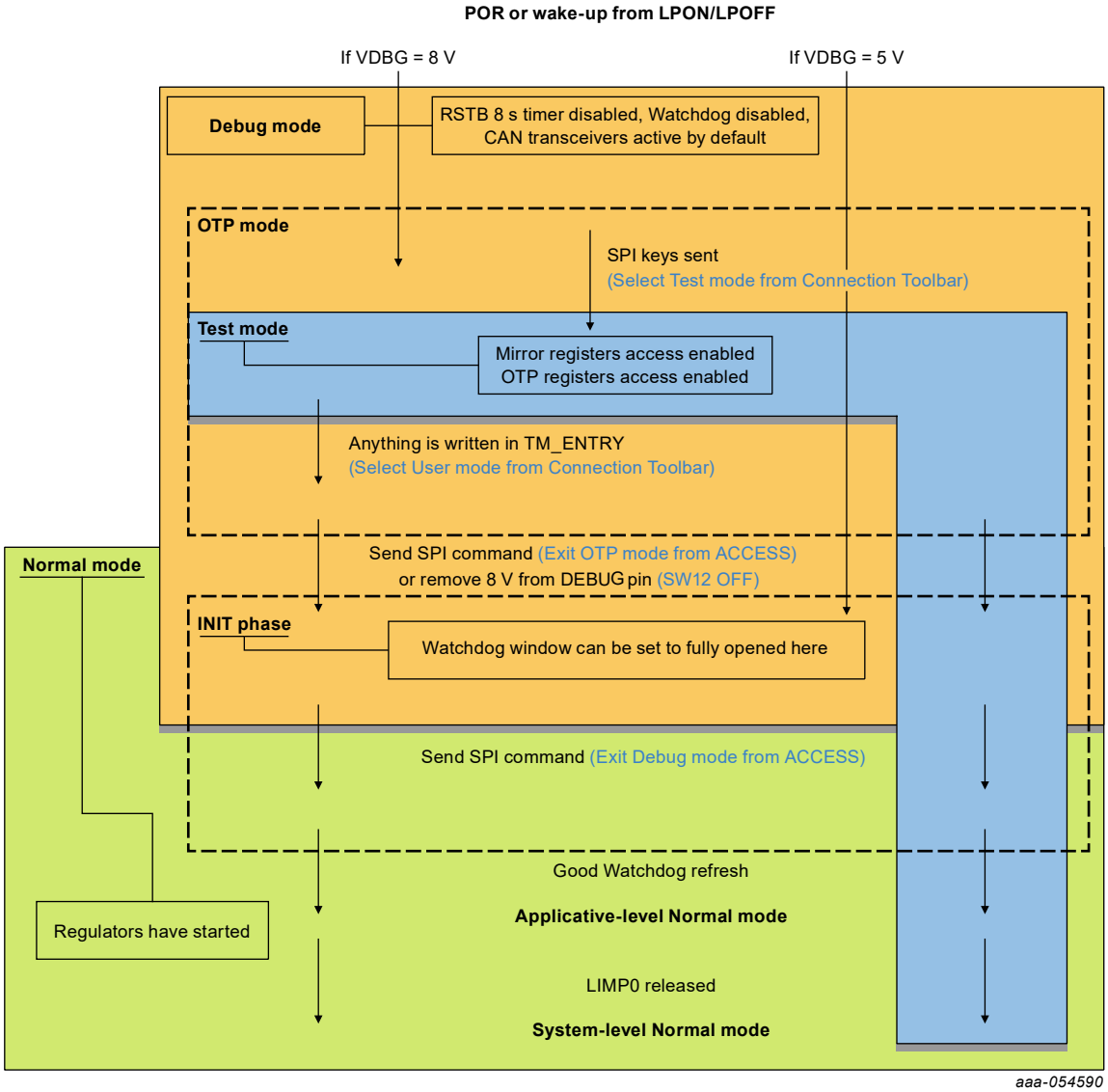

Figure 17. Overview of the different modes

6.1 Detailed state machine

In order to better understand the behavior of the device, Figure 18 illustrates the conditions for entering or exiting any state. The number of the state where the product is can be read inside the SPI register M_SYS1_CFG(0x06) -> M_FSM_STATE[4:0]. For more detailed information, see the FS2400 data sheet.

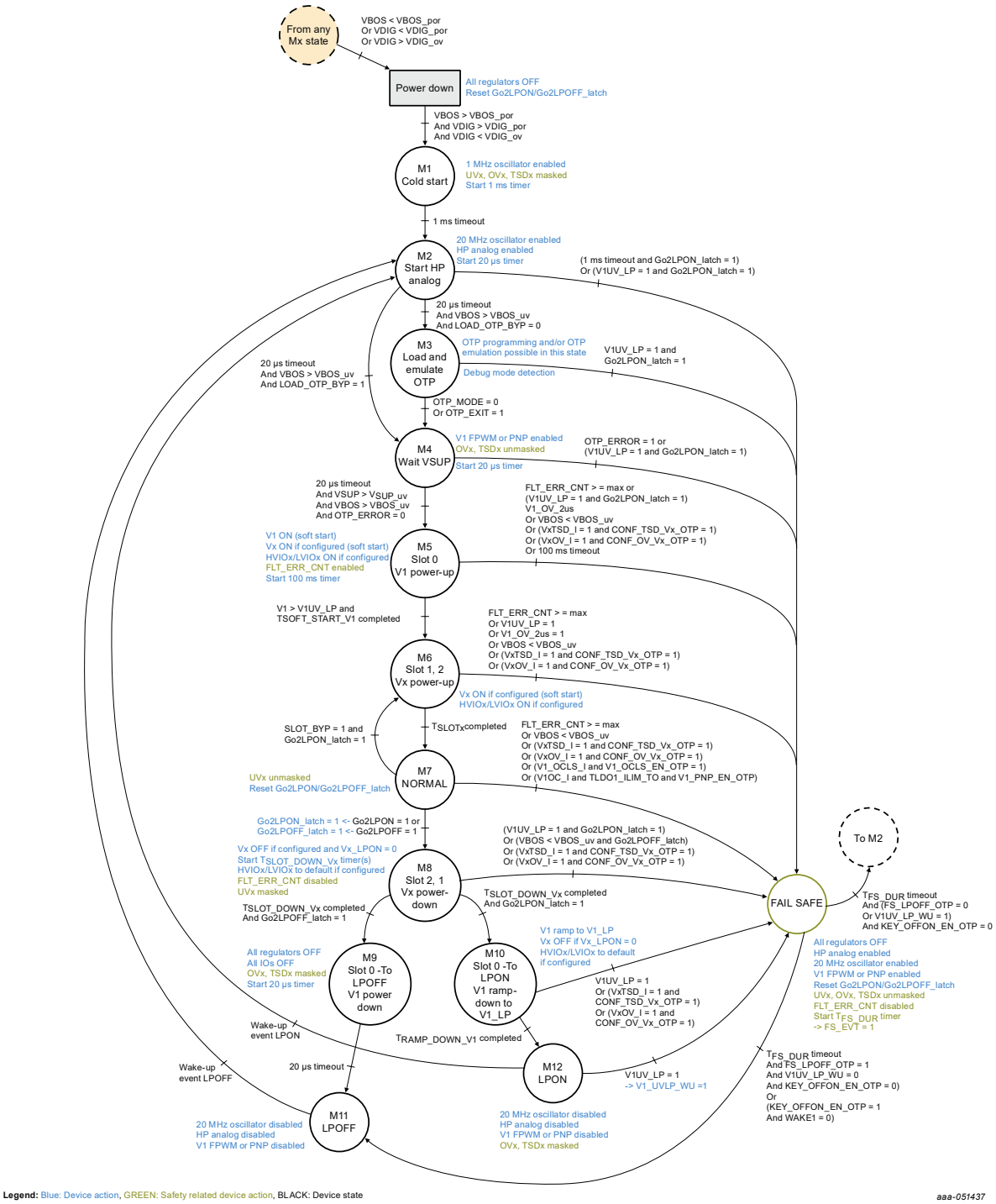

Figure 18. Simplified state machine

6.2 OTP mode

OTP mode is intended for OTP emulation and OTP programming. It is Intended for use during the engineering development process and not in the production application condition or in the vehicle.

To enter OTP mode, the voltage on the DEBUG pin must be set at V_{OTP} (7.75 V < DEBUG pin < 8.15 V) prior to apply any voltage on VSUP pin.

In OTP mode:

- No watchdog refresh is required as the watchdog is configured with infinite timeout and the watchdog window is fully opened.
- RSTB 8 s timer is disabled.
- Transition to fail-safe because of the fault error counter reaching its max value is disabled.
- CAN transceiver is set to active by default.

The CAN transceiver being set to active by default in OTP mode allows an easy debug of the hardware and software routines. It is possible to emulate an OTP configuration and to start the power-up sequence while benefiting from Debug mode.

Figure 19 shows the sequence to emulate an OTP configuration, or if already programmed, to start the power-up sequence without watchdog refresh.

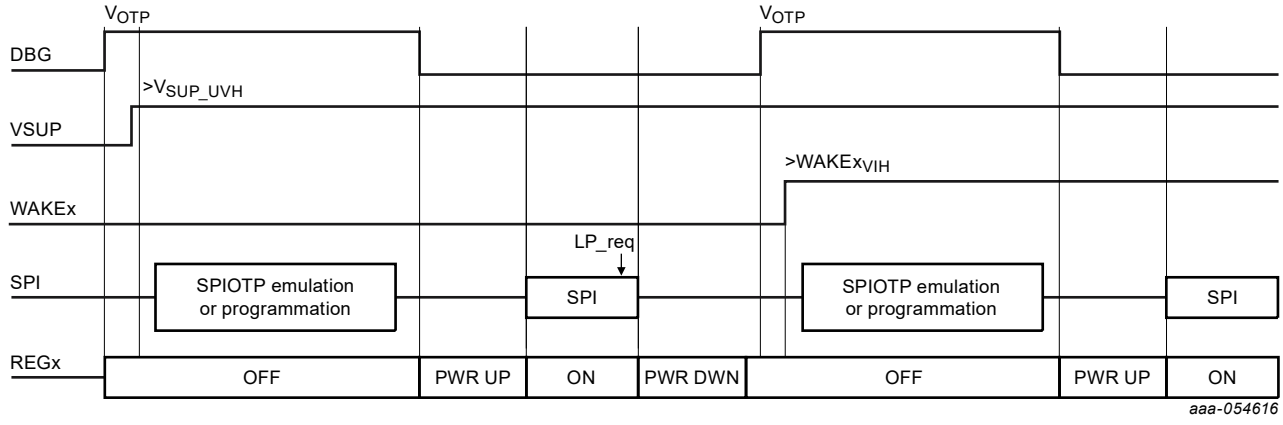

Figure 19. OTP entry/emulation of programming sequence

To enter OTP mode, use the following steps. Start from device power off or Low-power mode.

1. Apply V_{OTP} (7.75 V < DEBUG pin < 8.15 V).
2. Turn on the power supply higher than the V_{SUP_UVH} threshold.

OTP mode can also be entered when waking up from Low-power modes. The state machine will pass through the OTP mode entry state and verify the threshold again.

6.2.1 OTP emulation

Enter OTP mode and Test mode to emulate an OTP configuration. Follow the instructions using KITFS2400FRDMEVM or KTFS24SKTFRDMEVM. Start from device power off or Low-power mode.

1. Apply V_{OTP} (7.75 V < DEBUG pin < 8.15 V) SW12 on in EVB.
2. Turn on the power supply higher than the V_{SUP_UVH} threshold.
3. Send Test mode keys. A programming script usually contains Test mode keys.
4. Run a TBB script using the NXP GUI.
5. Pull the DEBUG pin below the OTP mode threshold. (SW12 off in EVB)

6. The device power-up sequence will start, and the device will remain in Debug mode and in Test mode. OTP configuration emulation will remain until device POR.

6.2.2 OTP programming

OTP mode and Test mode are required to permanently program an OTP configuration. Follow the instructions using KITFS2400FRDMEVM or KTFS24SKTFRDMEVM. The user can program device sectors twice. Make sure sectors are available. Start from device power off or Low-power mode.

1. Apply V_{OTP} (7.75 V < DEBUG pin < 8.15 V) SW12 on on the EVB.
2. Turn on the power supply higher than the V_{SUP_UVH} threshold.
3. Send Test mode keys. A programming script usually contains Test mode keys.
4. Program the device using the programming tool of the NXP GUI and a TBB script. Below is a script example.
5. Pull the DEBUG pin below the OTP mode threshold. (On the EVB, is SW12 off.)
6. The device power-up sequence will start and the FS24 will remain in Debug mode and Test mode.
7. Restart the device without entering OTP mode (DEBUG pin < 7.75 V) to verify the OTP has been programmed. The regulators should start automatically.

```
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 terms found at https://www.nxp.com/LA_OPT_NXP_SW. Only the "internal use
 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.
//FS2400-B0 - OTP Editor
//file generated on Thu Oct 19 13:57:03 2023
//Device Type : QM
//OTP ID : A1
//OTP Revision : B
//Part Marking : PFS2400AVMA1ES
//Customer : NXP

//Write main registers

//Test mode entry
SET_MODE:FS2400-B0:test-mode
//Verify test mode entry
GET_REG:FS2400-B0:M_TestMode:M_TM_STATUS1

//Configure OTP Mirror Registers
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0008
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x011C
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0001
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x011D
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x003a
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x011E
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x00a8
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x011F
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0017
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0120
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0057
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0121
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0034
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0122
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0012
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0123
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x00fc
```

```
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0124
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x00bc
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0125
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x000c
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0126
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0040
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0127
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0000
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0128
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0080
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0129
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0022
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x012A
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x00cf
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x012B
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x00cf
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x012C
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x00f0
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x012D
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0022
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x012E
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0000
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x012F
SET_REG:FS2400-B0:OTP:M_MIRRORDATA:0x0030
SET_REG:FS2400-B0:OTP:M_MIRRORCMD:0x0130
//OTP Command CRC_Fill + GO
SET_REG:FS2400-B0:M_OTP:M_OTPCMD:0x0125

//OTP Command CRC_Check + GO
SET_REG:FS2400-B0:M_OTP:M_OTPCMD:0x0124

//Verify test mode entry
GET_REG:FS2400-B0:M_TestMode:M_TM_STATUS1

//----------------------------- END MAIN --------------------------
```

6.3 Debug mode

Debug mode can be used during the customer production process. In Debug mode, no watchdog refresh is required as the watchdog is disabled along with other safety features. This mode can be accessed by applying V_{DBG} (3.5 V < DEBUG pin < 5.5 V) on the DEBUG pin prior to applying any voltage to the VSUP pin.

Once the VSUP pin is supplied properly, the device will start its power-up sequence and allow MCU programming or easy debug.

It is assumed that an OTP configuration was programmed into the device before Debug mode entry.

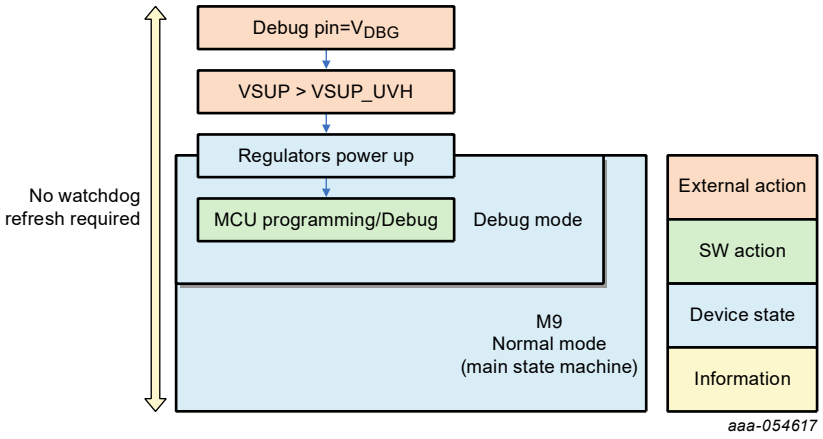


Figure 20. Debug mode flow chart

The FS24 can exit Debug mode using the DBG_EXIT bit from the M_SYS1_CFG SPI register. The procedure is detailed in Section 7.3.

6.4 Debug entry circuitry

To enter OTP mode or Debug mode, the proposed circuitry, shown in Figure 21, powered from VBOS can be used. The VBOS regulator manages the best of supply from VSUP (or V1 in LPON mode) to efficiently generate the power to supply the internal biasing of the device, in all device modes.

For Debug mode, to start the power-up sequence without need for watchdog refresh, place a jumper between signal DBG_5V and the DEBUG pin. This will apply ~4.3 V to the DEBUG pin.

To get to OTP mode for emulation or programming, a switch (DBG_SW in Figure 21) can be added to apply ~8 V on the DEBUG pin. Once the OTP script has been sent, DBG_SW should be opened to start the power-up sequence.

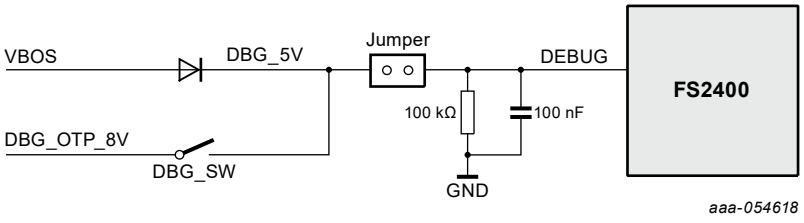


Figure 21. Debug entry external circuitry

7 Operation modes

7.1 INIT state

7.1.1 INIT registers configuration

After power up, the INIT state machine waits in INIT state. In this state, the MCU must configure FS_I_xxx registers and then perform a good watchdog refresh to get out of the INIT state.

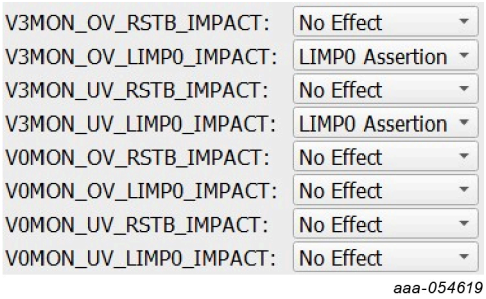
During this phase, the following features should be configured.

1. **Configure** all overvoltage and undervoltage impact on RSTB and LIMP0 with VxMON_OV_XXXX_IMPACT and VxMON_UV_XXXX_IMPACT SPI bits.
2. **Configure** the WD window period, the WD counters limits and its impact on RSTB and LIMP0. Ensure the configuration does not violate the FTTI requirement at system level.
   Note: *INIT state is the only state where you can configure the WD period to infinite. Once out of the INIT state you can only configure the WD period using the values defined between 1 and 16384 ms.*
3. **Configure** the fault error counter limit and its impact on RSTB and LIMP0 at intermediate value
4. **Configure** the RSTB pulse duration, RSTB request enablement, external RSTB monitoring enablement, RSTB 8 sec timer enablement
5. **Configure** Ext. IC error monitoring and its impact on RSTB

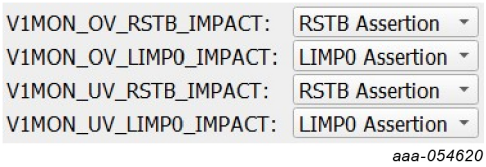
When all FS_I_xxx registers are written, the MCU should send a good WD refresh to get out of the INIT state and close the FS2400 initialization phase. By default, the WD period is configured to 256 ms. If the good WD refresh is not sent before those 256 ms, the WD error counter will be incremented. Incrimenting will eventually lead the device to generate RSTB pulses and/or main state machine transition to Fail-state state.

The figures in Table 14 shows an example of an INIT registers' configuration for the VMONs reaction for V0MON, V1MON, V3MON :

Table 14. VMON OV/UV reaction configuration example



aaa-054619



aaa-054620

SPI registers to write: FS_I_OVUV_CFG1 : 0x1680

FS_I_OVUV_CFG2 : 0x0480

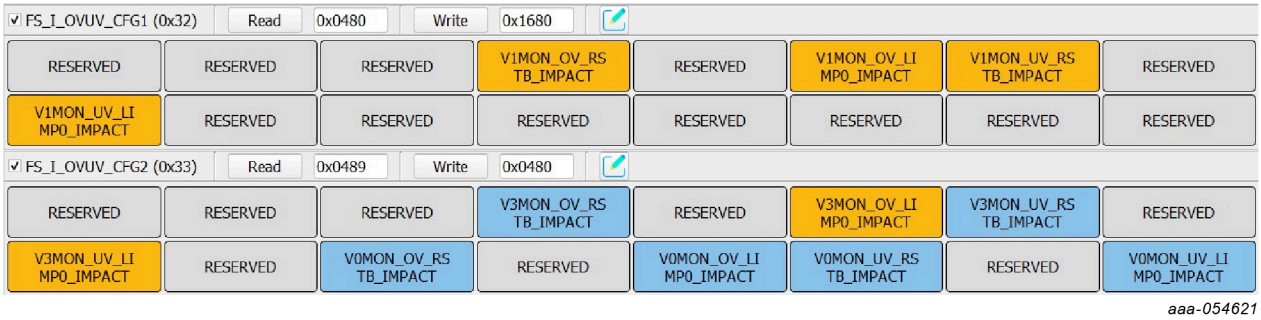


Figure 22. VMON OV/UV reaction configuration in the associated registers

7.1.2 INIT CRC

If the feature is enabled by OTP, the FS2400 provides a cyclic 8-bit CRC to verify the integrity of the INIT registers. Refer to the FS2400 data sheet for more information.

7.1.2.1 Computing the CRC

The 8-bit CRC is computed on the result of the concatenation of the following register bits:

- FS_I_OVUV_CFG1[15:0]
- FS_I_OVUV_CFG2[15:0]
- FS_I_ERRMON_LIMP0_CFG[15:0]
- FS_I_FSSM_CFG[15:4]
- FS_I_WD_CFG[15:7]

Reserved bits are not part of the concatenation

The calculation to apply on the result of the concatenation is the same as the SPI CRC, using x^8+x^4+x^3+x^2+1 polynomial. The MCU must write the obtained CRC in the FS_CRC register before closing the INIT phase, after the modification of the INIT registers.

Figure 23 an example of INIT CRC computation based on a given configuration of the INIT registers.

FS_I_OVUV_CFG1[15:0] concatenated	V1MON_OV_RSTB_IMPACT	1
	V1MON_OV_LIMP0_IMPACT	1
	V1MON_UV_RSTB_IMPACT	0
	V1MON_UV_LIMP0_IMPACT	1
FS_I_OVUV_CFG2[15:0] concatenated	VMON_OV_RSTB_IMPACT	1
	V3MON_OV_LIMP0_IMPACT	1
	V3MON_UV_RSTB_IMPACT	1
	V3MON_UV_LIMP0_IMPACT	1
	V0MON_OV_RSTB_IMPACT	1
	V0MON_OV_LIMP0_IMPACT	1
	V0MON_UV_RSTB_IMPACT	1
	V0MON_UV_LIMP0_IMPACT	1
FS_I_ERRMON_LIMP0_CFG[15:0] concatenated	LIMP0_GPO	0
	ERRMON_M	0
	ERRMON_FLT_POLARITY	0
	ERRMON_ACK_TIME[1]	0
	ERRMON_ACK_TIME[0]	0
	ERRMON_FS_REACTION	1
FS_I_FSSM_CFG[15:4] concatenated	RSTB_REQ_EN	0
	EXT_RSTB_DIS	0
	RSTB8S_DIS	0
	RSTB_DUR	0
	FLT_ERR_LIMIT[1]	0
	FLT_ERR_LIMIT[0]	1
	FLT_MID_RSTB_IMPACT	1
	FLT_MID_LIMP0_IMPACT	1
FS_I_WD_CFG[15:7] concatenated	WD_RSTB_IMPACT	1
	WD_LIMP0_IMPACT	1
	WD_DIS_LPON	0
	WD_RFR_LIMIT[1]	0
	WD_RFR_LIMIT[0]	0
	WD_ERR_LIMIT[1]	0
	WD_ERR_LIMIT[0]	1

CRC

FS_CRC[7:0]							
0b	0	0	1	0	1	0	1	1
0x	2				B			

aaa-054622

Figure 23. INIT CRC computation example

The FS24 GUI provides a tool to compute the INIT CRC result.

7.1.2.2 INIT CRC fault reaction

The reaction to an INIT CRC error can be configured using the INIT_CRC_LIMP0_IMPACT bit. When set to 0, there is no reaction upon an INIT CRC error event. When set to 1, an INIT CRC error will lead to LIMP0 pin assertion (if enabled) and an incrementation of the fault error counter.

When LIMP0 is disabled by OTP, INIT_CRC_LIMP0_IMPACT is set to 0. Otherwise, the fault error counter is incremented at each CRC cycle and lead to a transition to fail-safe (when the fault error counter limit is reached).

7.2 Normal applicative mode

When the device is in Normal applicative mode (Main state machine in normal mode, INIT state machine is in INIT_0 state and FS2400 is not in debug mode), the system is fully functional with all power supplies enabled and the device is providing full monitoring and operation of all the safety features in the device.

The FS2400 main state machine enters normal mode once regulators are powered-up without any error detected. No additional SPI commands are required to get the state machine to normal mode. As long as the WD is correctly configured/refreshed and no error occurs, the main state machine will remain in normal mode.

To stay in normal mode without having the MCU refreshing the WD, the MCU can configure the WD period to infinite by writing WDW_PERIOD[3:0] = 0b0000 in the FS_WDW_CFG SPI register.

Figure 24 shows how to correctly power-up the FS2400 (without Debug mode) to keep the main state machine in normal mode.

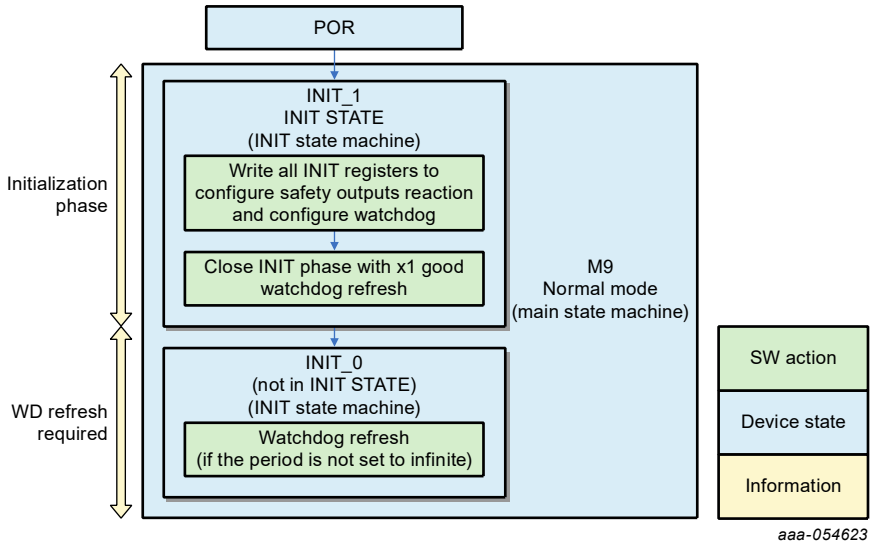


Figure 24. Normal mode entry diagram

The following sequence can be used to get to Normal applicative mode after powering-up the device.

```
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 NXP and may only be used strictly in accordance with the applicable license
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 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.
//Clear RSTB event flag
SET_REG:FS2400:SAFETY:FS_SAFETY_OUTPUTS:0x3804
//Clear POR and BAT_FAIL
SET_REG:FS2400:FUNCTIONAL:M_SYS_CFG:0x5000
//Set WD to infinite
SET_REG:FS2400:SAFETY:FS_WDW_CFG:0x0000
//Configure INIT OVUV reaction
SET_REG:FS2400:WRITE_INIT_SAFETY:FS_I_OVUV_CFG2:0x16ad
//Get out of INIT by sending one good WD refresh
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0x5ab2
//Get Fault error counter to 0 by refreshing the WD
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0xd564
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0x5ab2
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0xd564
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0x5ab2
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0xd564
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0x5ab2
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0xd564
```

7.3 Normal mode using Debug mode

In order to get the device to stay in normal mode without any action required from the MCU, the Debug mode can be used. To start the device in Debug mode : before powering the device, 5 V must be applied to the FS2400 DEBUG pin. Once the device is started by applying 12 V to the VSUP pin, the power-up sequence will start the V1 and V3 regulators.

It is possible to get to Normal applicative mode (thus out of the Debug mode) without shutting down the device. Using the “DBG_EXIT” bit from the M_SYS1_CFG SPI register, the device will exit the Debug mode. Before doing so, the MCU has to:

1. Make sure that the WD period has correctly been set (to either infinite or to the desired period).
2. Get out of the INIT state by sending a good WD refresh.

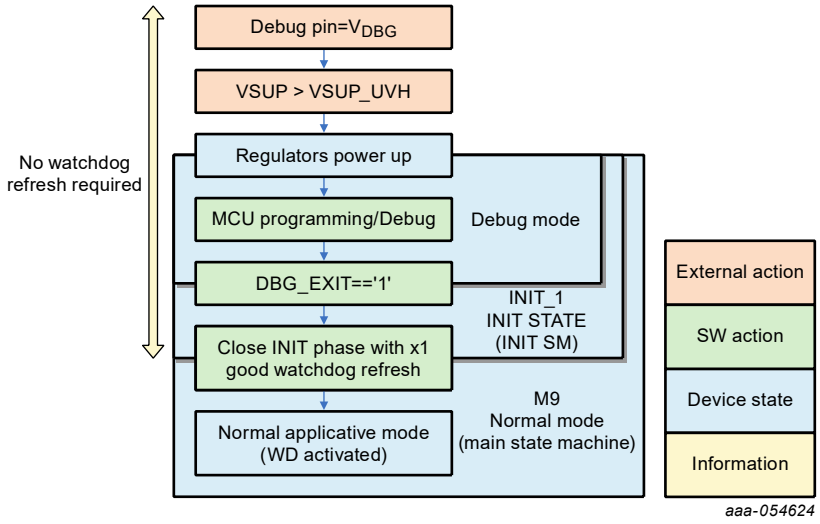

Figure 25. Normal applicative mode entry steps diagram using debug mode

The folllowing sequences can be used to get to normal applicative mode after powering up the device in Debug mode.

```
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 terms found at https://www.nxp.com/LA_OPT_NXP_SW. Only the "internal use
 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.//The device main state machine is in Normal mode
//The device INIT state machine is in INIT state
//The WD is enabled by OTP
//The device starts in Debug mode
//Set the WD period to infinite
SET_REG:FS2400:SAFETY:FS_WDW_CFG:0x0000
//Exit Debug mode
SET_REG:FS2400:FUNCTIONAL:M_SYS1_CFG:0x4818
//Get out of the INIT state by writing a good WD refresh
SET_REG:FS2400:SAFETY:FS_WD_ANSWER:0x5ab2
```

7.4 LPON mode

The LPON mode is a Low-power on mode, providing support to the minimum system requirements with low current consumption from the battery. During LPON mode, only the V1 (HVBUCK) regulator remains enabled by default to supply the microcontroller. V3 (HVLDO) regulator can be enabled in this mode depending on “V3ON_LPON” bit from M_REG_CTRL SPI register.

LPON mode can be accessed using two different methods while in Normal mode:

1. Writing the “GO2LPON” bit from the M_SYS_CFG SPI register
2. Setting the HVIO1 pin function as “mode selection” (using the HVIO1_WUCFG[1:0] bits) and applying a falling edge to the pin
   Before making the transition to LPON, be sure to correctly configure the desired wake-up sources to wake-up from LPON. This is done by configuring bits from M_IOWU_EN and M_WU1_EN SPI registers.

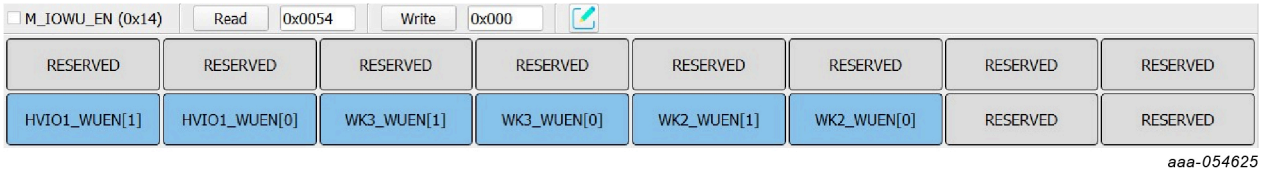


Figure 26. M_IOWU_EN register to select wake up event

7.5 LPOFF mode

This mode is intended to place the system in a fully off state with no system supplies active. Logic circuitry is supplied internally to allow proper wake-up from any of the available wake-up mechanism, with the minimum current consumption possible.

While in Normal mode, LPOFF mode can be accessed by writing the “GO2LPOFF” bit from the M_SYS_CFG SPI register.

Before making the transition to LPOFF, be sure to correctly configure the desired wake-up sources to wake-up from LPOFF. This is done by configuring bits from M_IOWU_EN and M_WU1_EN SPI registers.

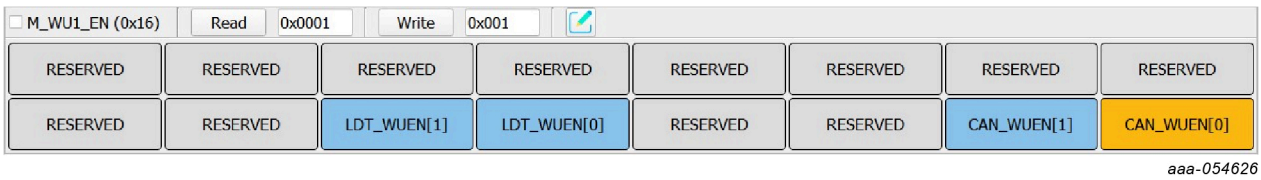


Figure 27. M_WU1_EN register to select wake up event

7.6 CAN operation

7.6.1 Enabling the CAN transceiver

The CAN transceiver integrated in the FS2400 has four different mode: Offline, Wake-up capable, Listen only, and Active. Active is the mode that allows to send and receive CAN frames.

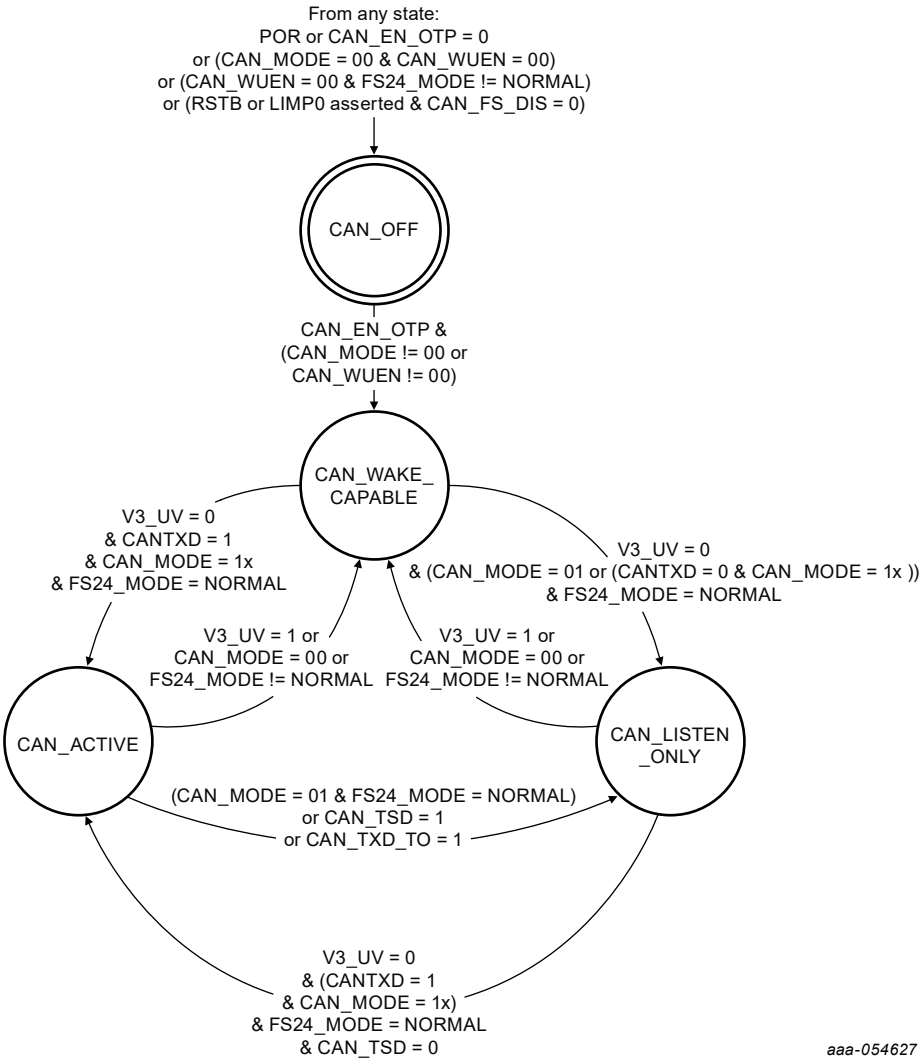


Figure 28. CAN transceiver simplified state machine

When the FS2400 is not in Debug mode, in order to use the CAN transceiver, the MCU needs to get the CAN state to CAN_ACTIVE. In order to do this, the FS2400 should be in Normal mode and the MCU should set the CAN_MODE[1] bit from the M_CAN SPI register.

When the FS2400 is in Debug mode, the CAN transceiver is active regardless of the CAN_MODE[1:0] bits state.

The MCU can control that the CAN transceiver is in active mode by reading the CAN_ACTIVE_MODE_S status bit in the same SPI register.

The following sequence shows is an example of a commands sequence to activate the CAN transceiver:

```
Copyright 2024 NXP. NXP Confidential. This software is owned or controlled by
 NXP and may only be used strictly in accordance with the applicable license
 terms found at https://www.nxp.com/LA_OPT_NXP_SW. Only the "internal use
 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.
//The device main state machine is in Normal mode
//Transceiver active mode
SET_REG:FS2400:FUNCTIONAL:M_CAN:0x0220
//Configuration CAN wake-up and interrupt capability
SET_REG:FS2400:FUNCTIONAL:M_WU1_EN:0x0003
//Read CAN state machine state
GET_REG:FS2400:FUNCTIONAL:M_CAN_MSK
```

7.6.2 CAN transceiver supply undervoltage

In most application use cases, the CAN transceiver is supplied through the VVCC5CAN by V3 regulator. That is why when the transceiver is set to ACTIVE mode or LISTEN ONLY mode, it is shut down on a V3 undervoltage event.

Nevertheless in some application use cases, the CAN transceiver can be supplied using V1 regulator. In this case, to guaranty that the CAN transceiver is shut down on a V1 undervoltage event, NXP recommends to configure the FS2400 to assert LIMP0 on a V1 undervoltage and that the MCU sets CAN_FS_DIS bit to 0. Additionally, the MCU must set CAN_MODE = 0b00 when the FS2400 reports an undervoltage on V1 regulator.

7.6.3 Mode change and CAN wake-up capability

When transitioning to LPON, the CAN state machine transitions automatically to Wake-up capable mode. It takes 4 µs for the state machine to change state and for FS24 to be capable to detect any wake-up event.

This structural blind spot can be prevented by changing the CAN state to “wake-up capable” by SPI using CAN_MODE[1:0] bits, before sending the “GO2LPON” request.

8 MCU programming

8.1 SPI communication

The FS24 provides a 32-bit SPI interface with the following arrangement:

Primary output secondary input bits (MOSI):

- Bits 31 to 25: register address
- Bit 24: read/write (For reading Bit 24 = 0; For writing Bit 24 = 1)
- Bits 23 to 8: control bits
- Bits 7 to 0: cyclic redundant check (CRC)

Primary input secondary output bits (MISO):

- Bits 31 to 24: general device status
- Bits 23 to 8: device internal control register content
- Bits 7 to 0: cyclic redundant check (CRC)

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

The MCU is the master driving MOSI. FS24 is the slave driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge. MSB is sent first.

In write command, MISO [31:24] bits are the general status flags, [23:8] bits are all 0 and MISO [7:0] is the CRC of the message sent by the FS24. In read command, MOSI [23:8] bits are all 0 and MOSI [7:0] is the CRC of the message sent by the MCU.

Table 15 describes SPI communication protocol for writing data into the FS24. Table 16 describes reading data from the FS24.

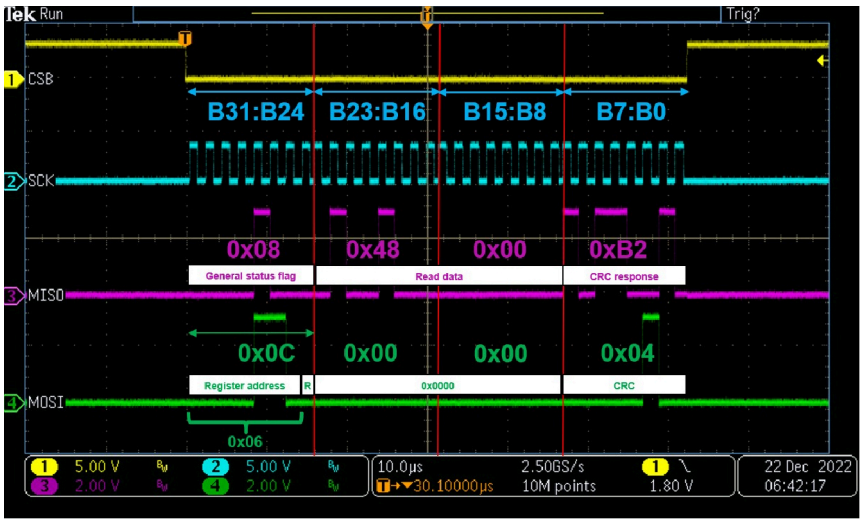
Table 15. SPI write command message construction

	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
MOSI	**Register address [6:0]**							**R/W**	**Write data [15:8]**							
MISO	0	WD_G	PHYG	WUG	IOG	COMG	VSUPG	VXG	**Read data [15:8]**							
	B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
MOSI	**Write data [7:0]**								**CRC [7:0]**							
MISO	**Read data [7:0]**								**CRC [7:0] - response**							

Table 16. SPI read command message construction

	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
MOSI	**Register address [6:0]**							**R/W**	**0x00**							
MISO	0	WD_G	PHYG	WUG	IOG	COMG	VSUPG	VXG	**Read data [15:8]**							
	B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
MOSI	**0x00**								**CRC [7:0]**							
MISO	**Read data [7:0]**								**CRC [7:0] - response**							

SPI with CRC frame examples:



aaa-054628

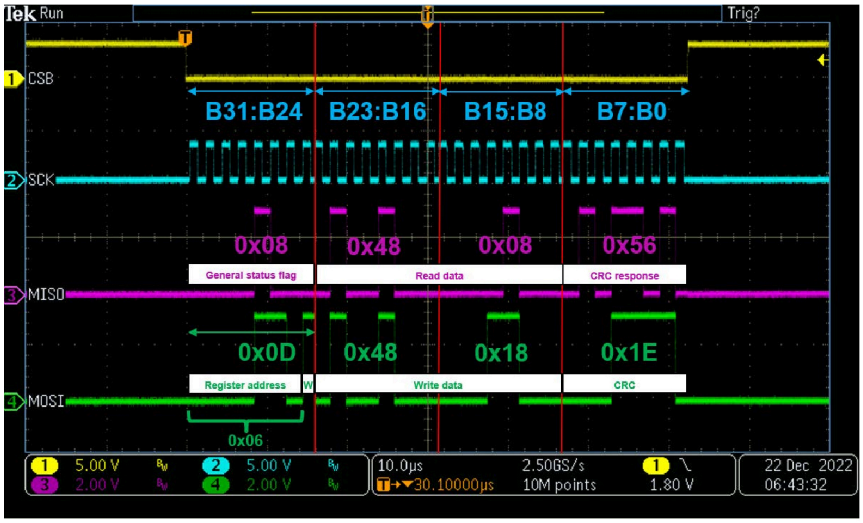
Figure 29. Read example M_SYS1_CFG(0x06)

The waveform shown in Figure 29 is obtained after clicking the **Read** button in the GUI, as shown in Figure 30:

aaa-054629

Figure 30. Read button

Write example M_SYS1_CFG(0x06) => Debug mode exit :



aaa-054630

Figure 31. Write example M_SYS1_CFG(0x06)

The waveform shown in Figure 31 is obtained after clicking the **Write?** button in the GUI as shown in Figure 32:

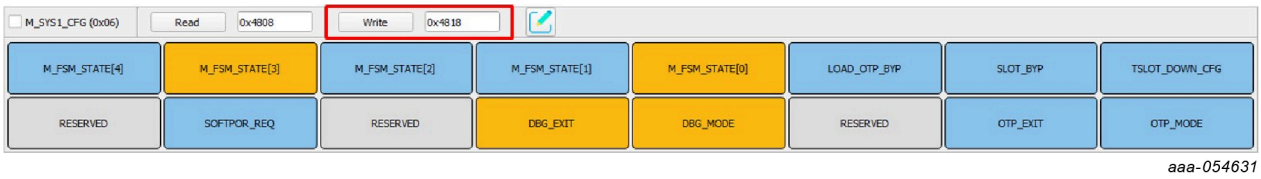


Figure 32. Write button

8.1.1 CRC calculation

An 8-bit CRC is required for each write and read SPI command. Computation of a CRC is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a seed value of hexadecimal '0xFF'.

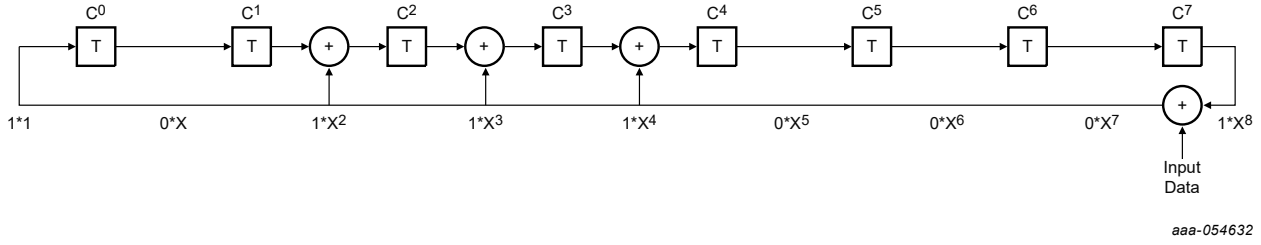


Figure 33. CRC encoder example

The effect of CRC encoding procedure is shown in Table 17. The seed value is appended into the most significant bits of the shift register.

Table 17. Data preparation for CRC encoding

Seed	Register address	Read/Write	Data_MSB	Data_LSB
0xFF	Bits[31:25]	Bit[24]	Bits[23:16]	Bits[15:8]

Table 18. Data preparation for CRC encoding

Seed ...	… padded with the message to encode	… padded with 8 zeros

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted.
   Note: *The 32-bits message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).*
3. Once the CRC is calculated, it replaces the CRC byte initially set to all zeros and is transmitted.

Procedure for CRC decoding

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
   - If the shift register contains all zeros, the CRC is correct.
   - If the shift register contains a value other than zero, the CRC is incorrect.

8.1.2 Cycle redundancy code example

```
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 NXP and may only be used strictly in accordance with the applicable license
 terms found at https://www.nxp.com/LA_OPT_NXP_SW. Only the "internal use
 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.
* Definitions
*****************************************************************************/
/* Assert macro does nothing */
#define FS_ASSERT(x) ((void)0)
/* Data frame (SPI or I2C). */
#define FS24_COMM_FRAME_SIZE 0x04U /* Length of the communication frame */
#define FS24_REG_ADDR_MASK 0x3FU /* Register address mask */
#define FS24_REG_ADDR_SHIFT 0x01U /* SPI register address shift */
/* CRC polynomial used for SPI communication. */
#define FS24_CRC_TBL_SIZE 256U /* Size of CRC table. */
#define FS24_COM_CRC_POLYNOM 0x1DU /* CRC polynom. */
#define FS24_COM_CRC_INIT 0xFFU /* CRC initial value.
* Constants
*****************************************************************************/
/* CRC lookup table. */
static const uint8_t FS24_CRC_TABLE[FS24_CRC_TBL_SIZE] = {
0x00U, 0x1DU, 0x3AU, 0x27U, 0x74U, 0x69U, 0x4EU, 0x53U, 0xE8U, 0xF5U, 0xD2U,
 0xCFU, 0x9CU,
0x81U, 0xA6U, 0xBBU, 0xCDU, 0xD0U, 0xF7U, 0xEAU, 0xB9U, 0xA4U, 0x83U, 0x9EU,
 0x25U, 0x38U,
0x1FU, 0x02U, 0x51U, 0x4CU, 0x6BU, 0x76U, 0x87U, 0x9AU, 0xBDU, 0xA0U, 0xF3U,
 0xEEU, 0xC9U,
0xD4U, 0x6FU, 0x72U, 0x55U, 0x48U, 0x1BU, 0x06U, 0x21U, 0x3CU, 0x4AU, 0x57U,
 0x70U, 0x6DU,
0x3EU, 0x23U, 0x04U, 0x19U, 0xA2U, 0xBFU, 0x98U, 0x85U, 0xD6U, 0xCBU, 0xECU,
 0xF1U, 0x13U,
0x0EU, 0x29U, 0x34U, 0x67U, 0x7AU, 0x5DU, 0x40U, 0xFBU, 0xE6U, 0xC1U, 0xDCU,
 0x8FU, 0x92U,
0xB5U, 0xA8U, 0xDEU, 0xC3U, 0xE4U, 0xF9U, 0xAAU, 0xB7U, 0x90U, 0x8DU, 0x36U,
 0x2BU, 0x0CU,
0x11U, 0x42U, 0x5FU, 0x78U, 0x65U, 0x94U, 0x89U, 0xAEU, 0xB3U, 0xE0U, 0xFDU,
 0xDAU, 0xC7U,
0x7CU, 0x61U, 0x46U, 0x5BU, 0x08U, 0x15U, 0x32U, 0x2FU, 0x59U, 0x44U, 0x63U,
 0x7EU, 0x2DU,
0x30U, 0x17U, 0x0AU, 0xB1U, 0xACU, 0x8BU, 0x96U, 0xC5U, 0xD8U, 0xFFU, 0xE2U,
 0x26U, 0x3BU,
0x1CU, 0x01U, 0x52U, 0x4FU, 0x68U, 0x75U, 0xCEU, 0xD3U, 0xF4U, 0xE9U, 0xBAU,
 0xA7U, 0x80U,
0x9DU, 0xEBU, 0xF6U, 0xD1U, 0xCCU, 0x9FU, 0x82U, 0xA5U, 0xB8U, 0x03U, 0x1EU,
 0x39U, 0x24U,
0x77U, 0x6AU, 0x4DU, 0x50U, 0xA1U, 0xBCU, 0x9BU, 0x86U, 0xD5U, 0xC8U, 0xEFU,
 0xF2U, 0x49U,
0x54U, 0x73U, 0x6EU, 0x3DU, 0x20U, 0x07U, 0x1AU, 0x6CU, 0x71U, 0x56U, 0x4BU,
 0x18U, 0x05U,
0x22U, 0x3FU, 0x84U, 0x99U, 0xBEU, 0xA3U, 0xF0U, 0xEDU, 0xCAU, 0xD7U, 0x35U,
 0x28U, 0x0FU,
0x12U, 0x41U, 0x5CU, 0x7BU, 0x66U, 0xDDU, 0xC0U, 0xE7U, 0xFAU, 0xA9U, 0xB4U,
 0x93U, 0x8EU,
0xF8U, 0xE5U, 0xC2U, 0xDFU, 0x8CU, 0x91U, 0xB6U, 0xABU, 0x10U, 0x0DU, 0x2AU,
 0x37U, 0x64U,
0x79U, 0x5EU, 0x43U, 0xB2U, 0xAFU, 0x88U, 0x95U, 0xC6U, 0xDBU, 0xFCU, 0xE1U,
 0x5AU, 0x47U,
```

```
0x60U, 0x7DU, 0x2EU, 0x33U, 0x14U, 0x09U, 0x7FU, 0x62U, 0x45U, 0x58U, 0x0BU,
 0x16U, 0x31U,
0x2CU, 0x97U, 0x8AU, 0xADU, 0xB0U, 0xE3U, 0xFEU, 0xD9U, 0xC4U
};
* Private Functions - Implementation
*****************************************************************************/
/* This function calculates CRC value of passed data array.
* Takes bytes in inverted order due to frame format. */
static uint8_t FS24_CalcCRC(const uint8_t* data, uint8_t dataLen)
{
uint8_t crc; /* Result. */
uint8_t tableIdx; /* Index to the CRC table. */
uint8_t dataIdx; /* Index to the data array (memory). */
FS_ASSERT(data != NULL);
FS_ASSERT(dataLen > 0);
/* Set CRC token value. */
crc = FS24_COM_CRC_INIT;
for (dataIdx = dataLen - 1; dataIdx > 0; dataIdx--)
{
tableIdx = crc ^ data[dataIdx];
crc = FS24_CRC_TABLE[tableIdx];
}
return crc;
}
/* Set CRC token value. */
crc = FS24_COM_CRC_INIT;
for (dataIdx = dataLen - 1; dataIdx > 0; dataIdx--)
{
tableIdx = crc ^ data[dataIdx];
crc = FS24_CRC_TABLE[tableIdx];
}
```

Using a lookup table to compute the CRC allows is faster than using the standard XOR operation bit to bit.

The principle of the lookup table is to store in advance all possible XOR operations between one byte of data and the CRC polynomial. That is to say 256 values.

Figure 34, Figure 35, and Figure 36 are examples of CRC computations for a single byte that can be found in the look-up table:

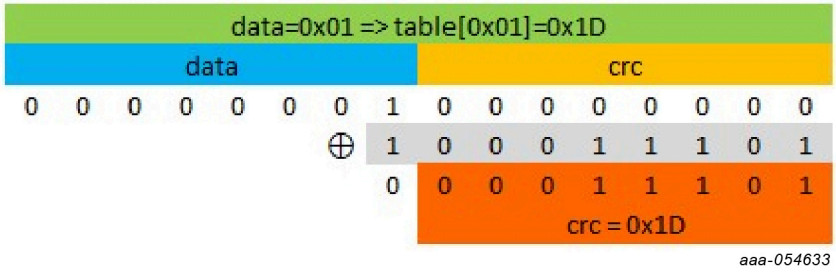

Figure 34. CRC of 0x01

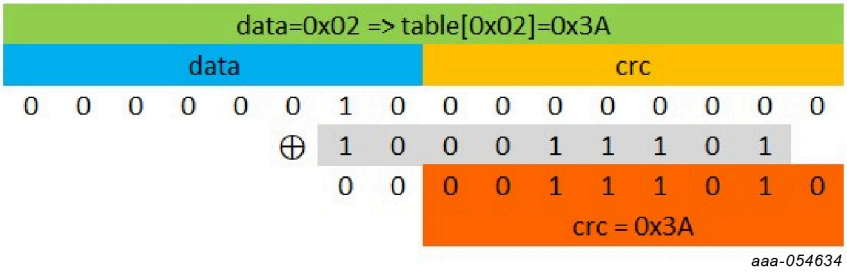

Figure 35. CRC of 0x02

Figure 36. CRC of 0xFF

8.2 LIMP0 release

To release LIMP0 after it was asserted because of a fault, several exit conditions must be validated before allowing the pin to be released:

- Fault is removed, fault error counter = 0
- SPI write to FS_LIMP0_REL [15:0] register:
  - Bits 15 to 8 filled with ongoing FS_WD_TOKEN[15:8] reversed and complemented
  - Bits 0 set to 1

Below is the procedure to compute the FS_LIMP0_REL [15:0] value to release the safety outputs. Table 19 illustrates all these steps with an example:

1. Get the FS_WD_TOKEN[15:8] value.
2. Swap MSB/LSB of the value get in Step 1.
3. Invert all computed bits at Step 2.
4. Write bits 15 to 8 computed in Step 3 into FS_LIMP0_REL [15:8] register. Bits 0 (LIMP0_REL) must be set to 1.

Table 19. FS_LIMP0_REL bits code to release LIMP0

Step 1	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Read FS_WD_ TOKEN [15:8]	0	1	0	1	1	0	1	0	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Step 2	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Reverse LSB/MSB	0	1	0	1	1	0	1	0	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Step 3	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Complement bits	1	0	1	0	0	1	0	1	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Step 4	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Write to FS_LIMP0_REL [15:8] and set B0 to 1	**1**	**0**	**1**	0	0	1	0	1	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**1**

LIMP0 release example:

FS_WD_TOKEN : 0x5AB2 → FS_LIMP0_REL : 0xA501

FS_WD_TOKEN : 0xD564 → FS_LIMP0_REL : 0x5401

Note: *Bits B0 to B7 from the FS_WD_TOKEN are not considered to compute the FS_LIMP0_REL register.*

8.3 Watchdog

8.3.1 Watchdog general information

To continuously check the microcontroller software activity and its ability to perform basic computing, a watchdog is implemented through the SPI bus. The FS2400 checks by awaiting a specific answer from the microcontroller during a pre-defined period called window. The first half of the window is closed and the second half is open.

A good watchdog refresh is a good watchdog answer during the open window.

A bad watchdog refresh is a bad watchdog answer during the open window, no watchdog refresh during the open window, or a good watchdog answer during the closed window.

There are two types of watchdog: window watchdog and timeout watchdog. In FS2400, the window watchdog uses a fixed 50 % duty cycle window, whereas the timeout watchdog uses a fully opened window (duty cycle of 100 %).

To send a good watchdog answer, the MCU must read the value from the FS_WD_TOKEN SPI register and write it back to the FS_WD_ANSWER SPI register. The FS2400 uses two tokens that alternate each time the watchdog is correctly refreshed : 0x5AB2 and 0xD564.

Table 20. Watchdog types

SPI	**Window WD**		**Timeout WD**
	CLOSED	**OPEN**	**(always open)**
Bad key	WD_NOK	WD_NOK	WD_NOK
Good key	WD_NOK	**WD_OK**	**WD_OK**
None (timeout)	NA	WD_NOK	WD_NOK

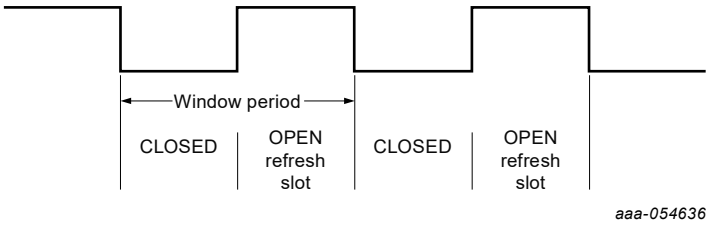

Figure 37. Watchdog refresh versus time window

The first good watchdog refresh closes the initialization phase of the FS2400. Then the watchdog is running, and the microcontroller must refresh the watchdog in the open window of the watchdog window period. The duration of the watchdog window is configurable from 1.0 ms to 16384 ms with the WDW_PERIOD [3:0] SPI bits.

When a RSTB event occurs, the watchdog is disabled and its configuration is reset as it would be after a POR of the device. The watchdog token is set to 0x5AB2, the window period is set to 256 ms and the watchdog type is set to timeout.

8.3.2 Watchdog in LPON

Depending on the application requirements, the timeout watchdog can be enabled or disabled in LPON using the WD_DIS_LPON bit while in INIT phase.

When the FS2400 state machine makes its transition to LPON and WD_DIS_LPON = 0 (watchdog enabled in LPON), the MCU continues to refresh the watchdog.

When the FS2400 state machine makes its transition to LPON and WD_DIS_LPON = 1 (watchdog disabled in LPON), the watchdog configuration is reset: the watchdog token is set to 0x5AB2, the window period is set to 256 ms and the watchdog type is set to timeout. This implies that after waking up the FS2400 from LPON mode, the MCU must configure the watchdog. To make sure that the MCU is synchronized with the FS2400 watchdog window, the MCU sends the WD_RST_REQ command to reset the watchdog window before configuring the watchdog.

Note: *When sending the WD_RST_REQ command, the first watchdog window period will always be 256 ms, as this is the default configuration.*

Figure 38 illustrates how to handle the watchdog configuration during wake-up from the FS2400 LPON mode.

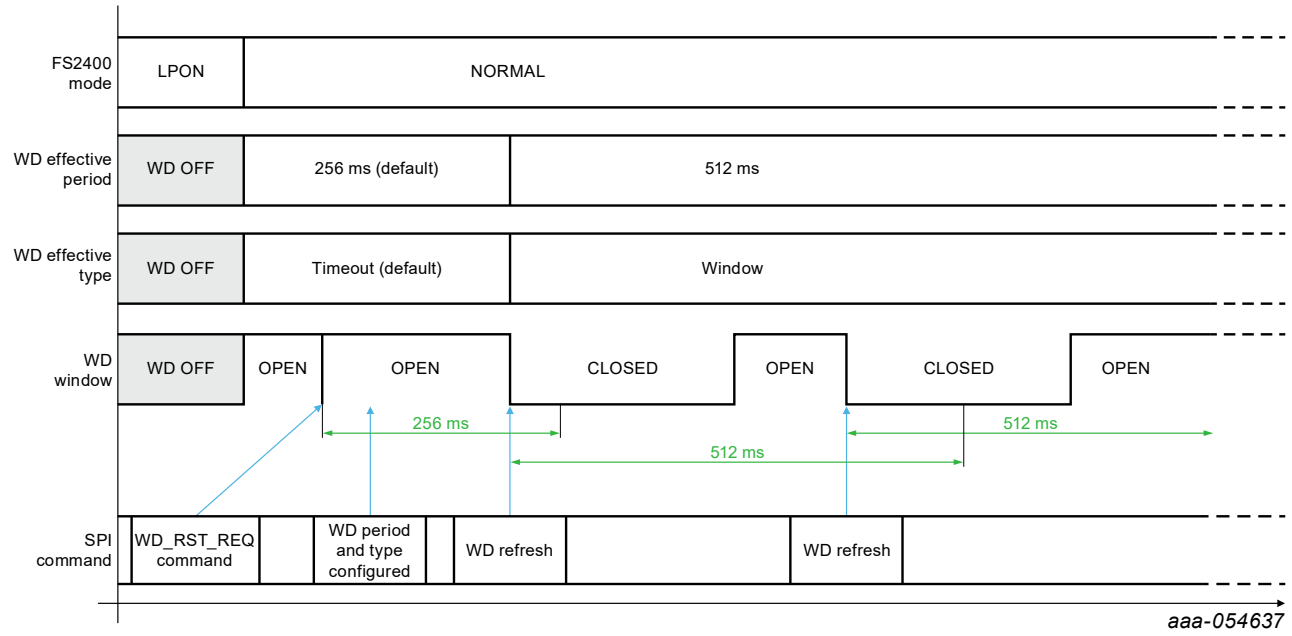

Figure 38. Watchdog configuration during wake-up from LPON

8.4 Hardware identification (HID)

8.4.1 Using WAKEx/HIDx pins

The HID feature comes on top of the WAKE 2 pin and the WAKE 3 pin to allow the electronic control unit (ECU) location in the car based on the WAKEx/HIDx pins hardware connection.

The WAKEx/HIDx pin state can be:

- Connected to VBAT
- Connected to GND
- Open

Using the two WAKEx/HIDx pins allows up to nine different HID combinations.

The HID is only available in Normal mode and is activated by writing HIDWx_ENABLE = 1 in the M_HW_ID SPI register.

ECU identification is done by controlling the HID pullup and pulldown current sources (HIDWxPU/PD_EN or HIDWxPU/PD_DIS) and reading the associated WAKEx pin status using the WKx_S bits of the M_STATUS SPI register.

The pin threshold (HIDWx_TH_SEL), and pullup/pulldown current values (HIDWx_10MA_EN) are programmable via the M_HW_ID SPI register to allow integration into different systems.

The script below is an example showing how to determine the hardware connection of the HID0 pin.

```
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 NXP and may only be used strictly in accordance with the applicable license
 terms found at https://www.nxp.com/LA_OPT_NXP_SW. Only the "internal use
 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.
//Enable HID0 (WAKE2) pull-down circuitry, disable pull-up circuitry
SET_REG:FS2400:FUNCTIONAL:M_HW_ID:0x0260
//Get WAKE2 pin status
GET_REG:FS2400:FUNCTIONAL:M_STATUS
// Enable HID0 (WAKE2) pull-up circuitry, disable pull-down circuitry
SET_REG:FS2400:FUNCTIONAL:M_HW_ID:0x0290
//Wait for the pin to change level (min 20 µs)
//Get WAKE2 pin status
GET_REG:FS2400:FUNCTIONAL:M_STATUS
```

Based on the circuitry enabled and the status read from the pin status bits, the hardware connection of the pin can be determined by Table 21.

Table 21. HID pin truth table

	HIDxPD_EN = 1 & HIDxPU_EN = 0	HIDxPD_EN = 0 & HIDxPU_EN = 1		Pin hardware connection
WKx_S value	0	0	⇒	Pin is connected to GND
WKx_S value	0	1	⇒	Pin is open
WKx_S value	1	1	⇒	Pin is connected to VBAT

8.4.2 Using LIMP0 pin

The input buffer on the LIMP0 pin may be used as an additional HID pin if needed. In this case, an external bias current may be applied using a resistor connected to a supply.

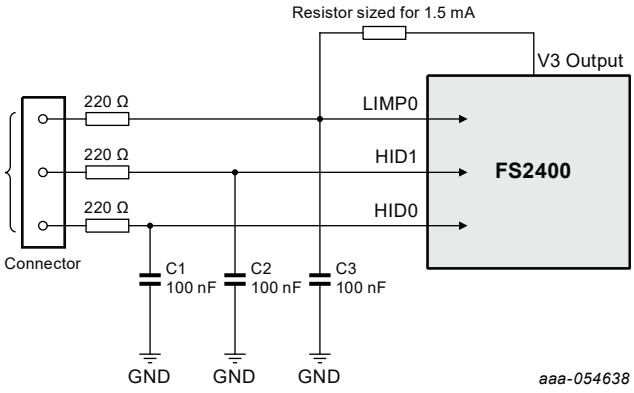

Figure 39. LIMP0 pin used as hardware identification

To use LIMP0 as a HID pin, the FS2400 must be programmed with LIMP0_EN_OTP = 0 and the MCU must configure LIMP0_GPO = 1 during the INIT phase. The pin state is controlled using LIMP0_REQ (to assert the pin to low level) and LIMP0_REL (to release the pin to high level) control bits. Its state can be read using LIMP0_SNS bit from FS_SAFETY_OUTPUTS SPI register

The script below is an example showing how to determine the hardware connection of the LIMP0 pin.

```
Copyright 2024 NXP. NXP Confidential. This software is owned or controlled by
 NXP and may only be used strictly in accordance with the applicable license
 terms found at https://www.nxp.com/LA_OPT_NXP_SW. Only the "internal use
 license" in Section 2.2 in the NXP SOFTWARE LICENSE AGREEMENT is granted for
 this software.
//During INIT phase, configure LIMP0 as GPO
SET_REG:FS2400:WRITE_INIT_SAFETY:FS_I_ERRMON_LIMP0_CFG:0x8000


//Assert LIMP0 pin low
SET_REG:FS2400:SAFETY:FS_SAFETY_OUTPUTS:0x0001
//Get LIMP0 pin status
GET_REG:FS2400:SAFETY:FS_SAFETY_OUTPUTS

//Release LIMP0 pin to high level
SET_REG:FS2400:SAFETY:FS_LIMP0_REL:0x0001
//Wait for the pin to change level (min 200 µs)
//Get LIMP0 pin status
GET_REG:FS2400:SAFETY:FS_SAFETY_OUTPUTS
```

Based on the circuitry enabled and the status read from the pin status bits, the hardware connection of the pin can be determined by Table 22.

Table 22. LIMP0 pin as HID truth table

	LIMP0_REQ = 1 & LIMP0_REL = 0	LIMP0_REQ = 0 & LIMP0_REL = 1		Pin hardware connection
LIMP0_SNS value	0	0	⇒	Pin is connected to GND
LIMP0_SNS value	0	1	⇒	Pin is open
LIMP0_SNS value	1	1	⇒	Pin is connected to VBAT

8.5 ABIST

Running the ABIST requires the following four-step procedure:

1. Always clear the previous ABIST results before launching a new ABIST.
2. Select one or more comparators to run the ABIST: V0MON, V1MON, V3MON, V1UVLP. Read the ABIST status: ABIST ready, ABIST ongoing.
3. Launch the ABIST.
4. Once the ABIST is done, read the diagnosis.

In addition to that procedure, the following are good practices when running the ABIST:

- When ABIST_READY or ABIST_DONE is stuck at 0, it is recommended to check that the VMONs are not reporting any overvoltage or undervoltage by reading the flags. It is also recommended to try to run the ABIST again by starting at Step 1.
- When the ABIST fails for some voltage monitoring, it is recommended to rerun the ABIST from Step 1 to make sure that the failure is permanent. If it is, the LIMP0 pin should not be released.

Figure 40 shows this procedure in the form of a diagram, integrating the register bits that ares read and written at each step.

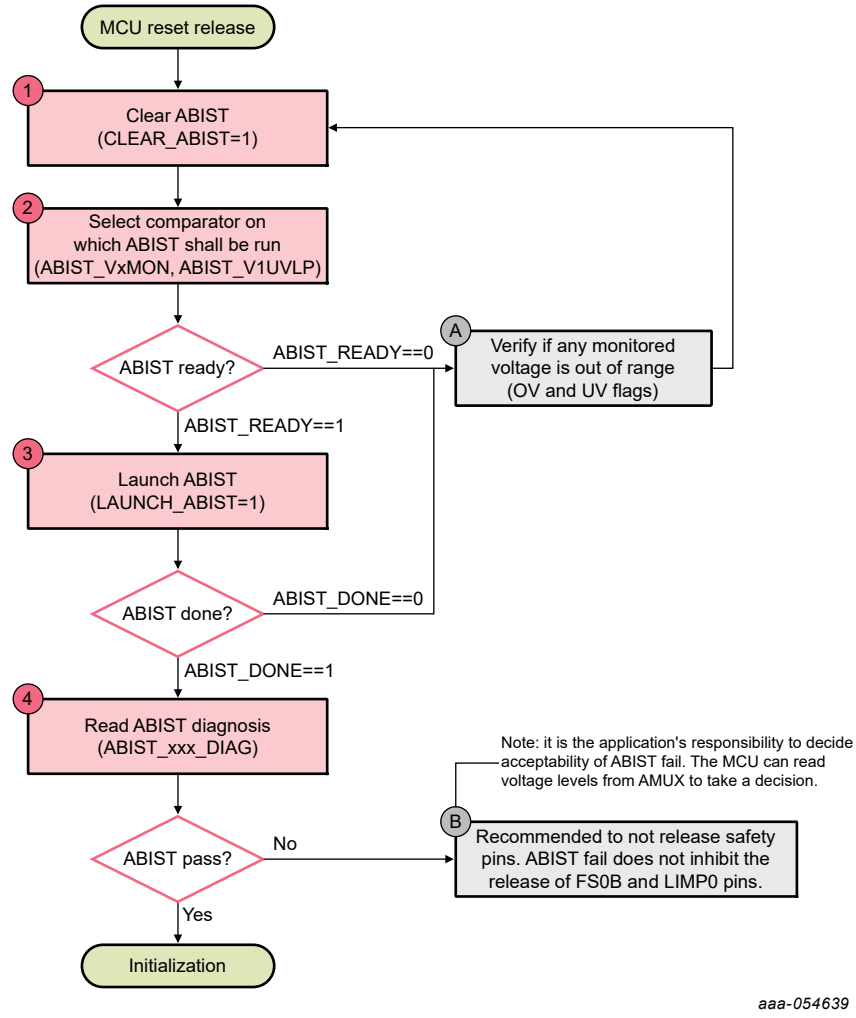

Figure 40. ABIST procedure

8.6 Long duration timer (LDT) functions implementation

The FS2400 provides five long duration timer (LDT) functions to count, enter, or exit from a Low-power mode. This feature provides a wide range of configurable counting periods. The LDT can count up to 194 days with a 1 s resolution, or 36 minutes with a 128 µs resolution.

8.6.1 Function 1

Function 1 generates a flag and an interrupt pulse (INTB) once the counter has reached its target value defined in LDT_AFTER_RUN.

Steps:

1. Start from INIT_FS or Normal mode
2. Configure M_LDT_CTRL
   a. Clean LDT with LDT_EN = 0
   b. Select Function 1 with LDT_FNCT[2:0] = 0
   c. Select short count (LDT_MODE = 1) or long count (LDT_MODE = 0)
   d. Configure the real-time timer with LDT_SEL = 1 (read real-time value of 24-bit timer)

3. LDT_EN = 1

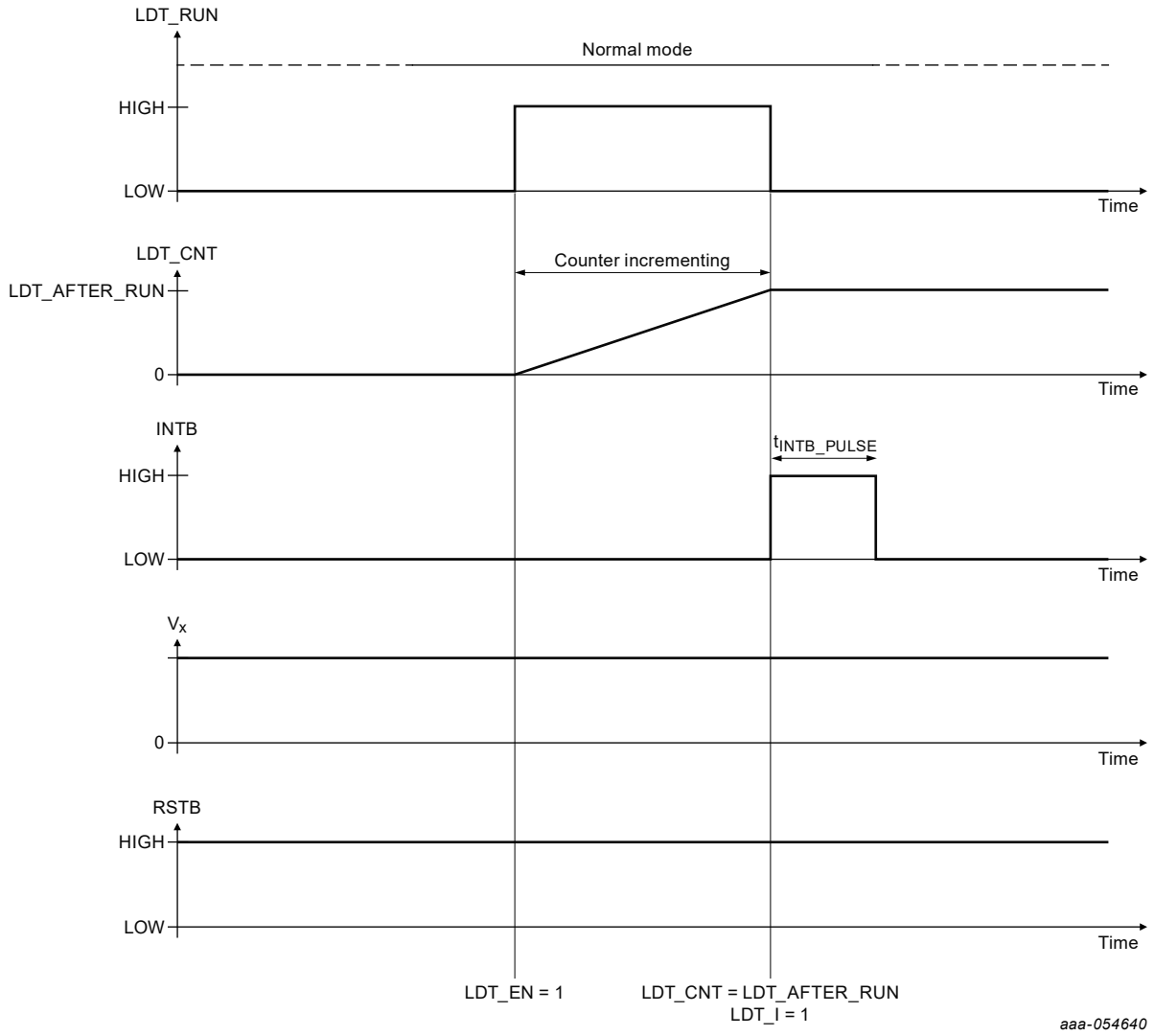

Figure 41. LDT function 1

Note: *LDT_CNT will be reset when re-enabled again: LDT_EN = 0 # 1.*

8.6.2 Function 2

Function 2 allows the user to enter a Low-power mode once a counter has reached its target value. As soon as the LDT_EN bit is enabled, the counter starts. While running, the LDT_RUN bit is set to 1. Once the counter has reached the target value set in LDT_AFTER_RUN, the device goes to the selected Low-power mode in the M_LDT_CTRL register.

Steps:

1. Start from INIT or Normal mode
2. Configure M_LDT_CTRL
   a. Clean LDT with LDT_EN = 0
   b. Select Function 2 with LDT_FNCT[2:0] = 1
   c. Select short count (LDT_MODE = 1) or long count (LDT_MODE = 0)

d. Configure the real-time timer with LDT_SEL = 1 (read real-time value of 24-bit timer)

3. Set LDT_AFTER_RUN[15:0] counter value in the M_LDT_CFG1 register
4. Set LDT2LP to select either LPON mode or LPOFF mode
   - For LPON mode: write LDT2LP = 1
   - For LPOFF mode: write LDT2LP = 0
5. Send LDT_EN = 1

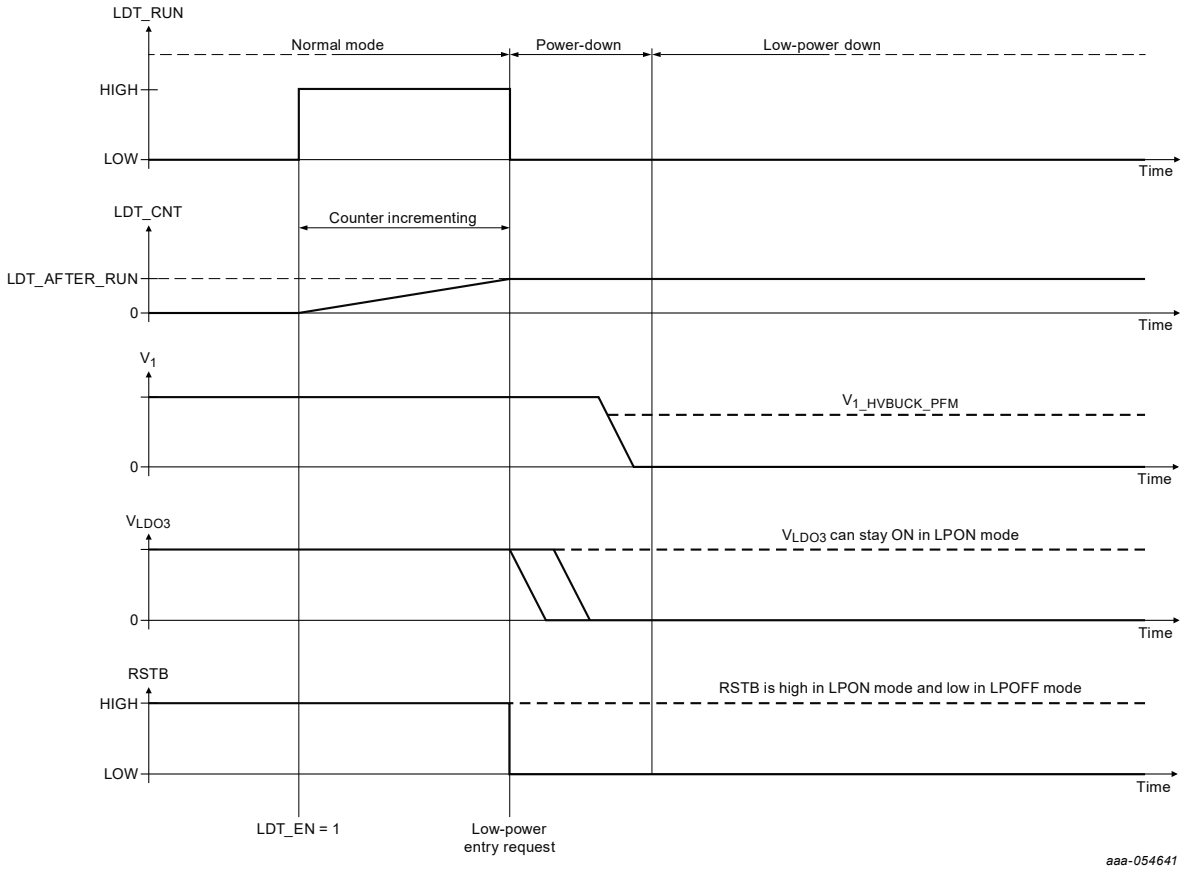

Figure 42. LDT function 2

8.6.3 Function 3

Function 3 allows the user to enter and exit from a Low-power mode, using two configurable counter target values. In Normal mode, the LDT counts up to the after-run value configured in the LDT_AFTER_RUN[15:0] bits and enters the selected Low-power mode. Once in Low-power mode, the LDT will count to the wake-up target value set with bits LDT_WUP_L[15:0] and LDT_WUP_H[7:0] and wake the FS24 up, unless another wake-up event occurred before.

Steps:

1. Start from INIT or Normal mode
2. Set LDT_WUEN[1:0] = x1 in M_WU1_EN
3. Configure M_LDT_CTRL
   a. Clean LDT with LDT_EN = 0
   b. Select Function 3 with LDT_FNCT[2:0] = 2
   c. Select short count (LDT_MODE = 1) or long count (LDT_MODE = 0)

d. Configure the real-time timer with LDT_SEL = 0 (reads/sets target value of wake-up LDT timer)

4. Set LDT_AFTER_RUN[15:0] counter value in M_LDT_CFG1
5. Set LDT_WUP_L[15:0] and LDT_WUP_H[7:0] in M_LDT_CFG2 and M_LDT_CFG3
6. Set LDT2LP to select either LPON mode or LPOFF mode
   - For LPON mode: write LDT2LP = 1
   - For LPOFF mode: write LDT2LP = 0
7. Send LDT_EN = 1

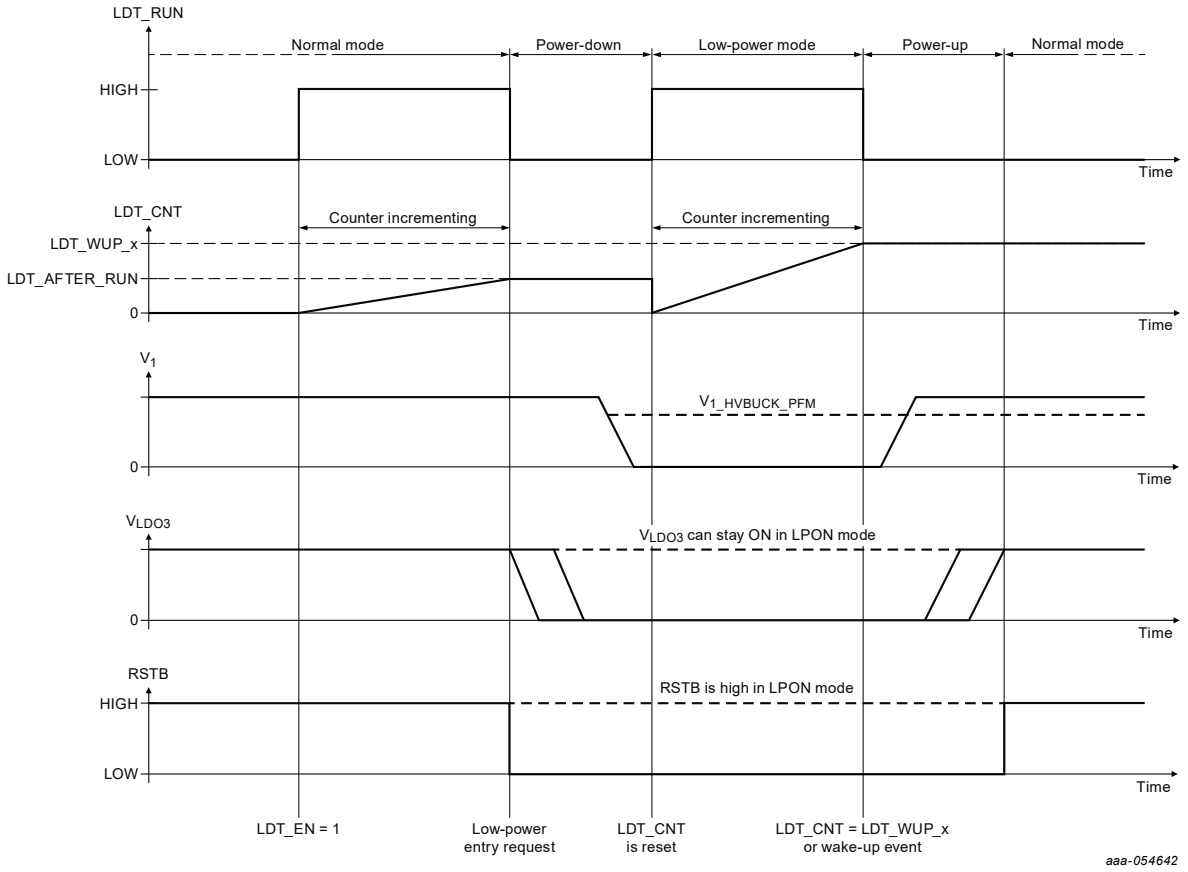

Figure 43. LDT function 3

Note: *LDT_CNT will be reset when re-enabled again: LDT_EN = 0 # 1.*

8.6.4 Function 4

Function 4 allows the user to exit a Low-power mode after the counter has reached its wake-up target value. Low-power mode should be entered with an SPI command or HVIO1 mode selection function. Once in Low-power mode, the LDT will count up to the wake-up target value set with LDT_WUP_L[15:0] and LDT_WUP_H[7:0] bits and wake the FS24 up, unless another wake-up event occurred before.

Steps:

1. Start from INIT or Normal mode
2. Set LDT_WUEN[1:0] = x1 in M_WU1_EN
3. Configure M_LDT_CTRL
   a. Clean LDT with LDT_EN = 0
   b. Select Function 4 with LDT_FNCT[2:0] = 3

c. Select short count (LDT_MODE = 1) or long count (LDT_MODE = 0)
d. Configure the real-time timer with LDT_SEL = 0 (reads/sets target value of wake-up LDT timer)

4. Set LDT_WUP_L[15:0] and LDT_WUP_H[7:0] in M_LDT_CFG2 and M_LDT_CFG3
5. Send LDT_EN = 1
6. Send SPI command to go to LPON mode (GO2LPON = 1) or LPOFF mode (GO2LPOFF = 1)

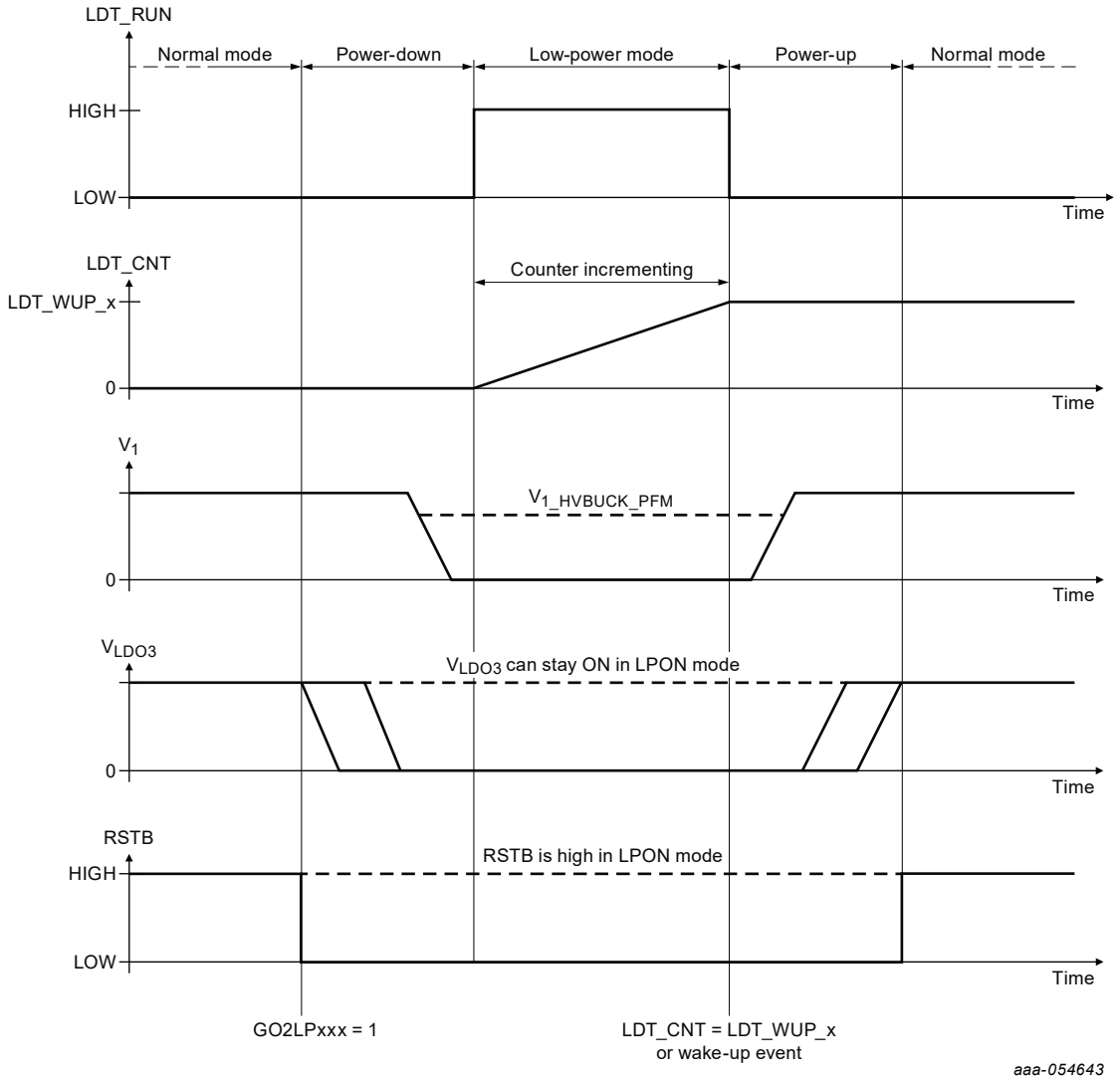

Figure 44. LDT function 4

Note: *LDT_CNT will be reset when re-enabled again: LDT_EN = 0 # 1.*

8.6.5 Function 5

Function 5 allows the user to configure the LDT to count once in Low-power mode and to not wake up unless the counter overflows or if another wake-up event occurs. Low-power mode should be entered with SPI command.

Steps:

1. Start from INIT or Normal mode
2. Set LDT_WUEN[1:0] = x1 in M_WU1_EN
3. Configure M_LDT_CTRL
   a. Clean LDT with LDT_EN = 0
   b. Select Function 5 with LDT_FNCT[2:0] = 4
   c. Select short count (LDT_MODE = 1) or long count (LDT_MODE = 0)
   d. Configure the real-time timer with LDT_SEL = 1 (read real time value of 24-bit timer)
4. Send LDT_EN = 1
5. Send SPI command to go to LPON mode (GO2LPON = 1) or LPOFF mode (GO2LPOFF = 1)

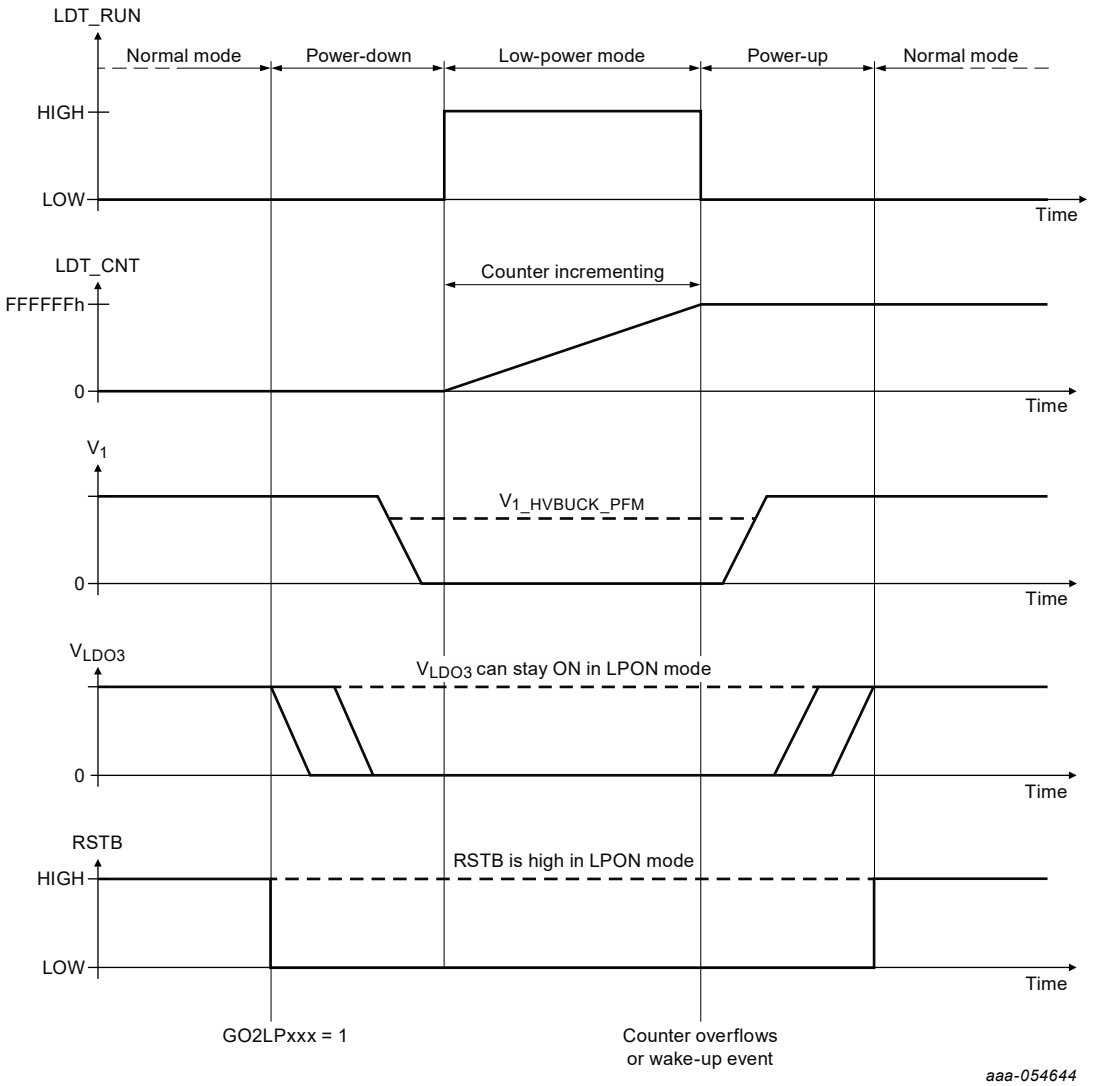

Figure 45. LDT function 5

Note: *LDT_CNT will be reset when re-enabled again: LDT_EN = 0 # 1.*

9 HVBUCK OTP configuration guidelines

The HVBUCK is a block with a complex configuration. This section gives guidelines to design the different parameters based on the application use case.

9.1 BUCK_RCOMP_OTP, BUCK_CCOMP_OTP, and BUCK_SC_OTP

The HVBUCK compensation network (BUCK_RCOMP_OTP and BUCK_CCOMP_OTP) and slope compensation (BUCK_SC_OTP) recommendations are optimized for the application main use cases. The recommendations cover all ranges of output capacitor and inductor defined in the FS2400 data sheet.

Table 23. Recommended configuration for the HVBUCK compensation parameters

BUCK_CLK	2.2 MHz			450 kHz		
VV1_BUCK	2 V - 2.5 V	3.3 V	5 V	2 V - 2.5 V	3.3 V	5 V
BUCK_RCOMP	975 kΩ			650 kΩ	975 kΩ	
BUCK_CCOMP	33.5 pF			44.5 pF	23 pF	23 pF
BUCK_SC	0x0A : 4345 mV/µs	0x17 : 3275 mV/µs	0x1C : 2865 mV/µs	0x07 : 918 mV/µs	0x25 : 426 mV/µs	0x29 : 360 mV/µs

9.2 BUCK_LP_DVS_OTP

The BUCK_LP_DVS_OTP parameter defines the DVS voltage ramp when using the DVS functionality in Normal mode or transitioning from VV1_BUCK voltage to VV1_LP_BUCK voltage during transition between Normal mode and LPON. The design of this parameter is constrained by the output capacitor of the regulator. As the regulator voltage is controlled during this phase, it is important that the current drained from or by that capacitor and going to the HVBUCK block does not exceed 300 mA.

The maximum DVS value is given by: $DVS_{max} = \frac{300\ \text{mA}}{C_{out\_max}}$, with DVS_{max} in mV/µs and C_{out_max} in µF.

Figure 46 shows the recommended configuration for HVBUCK DVS value depending on the switching frequency.

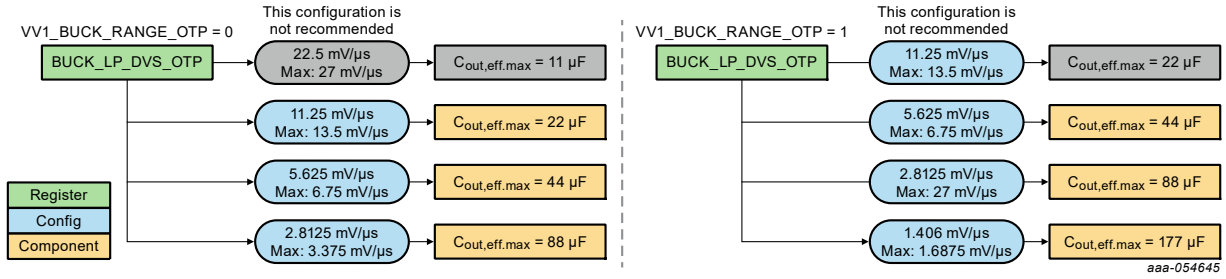

Figure 46. BUCK_LP_DVS_OTP configuration recommendations

9.3 BUCK_PFM_TON_OTP and BUCK_PFM_TOFF_OTP

In LPON mode, HVBUCK runs in pulse frequency modulation (PFM) mode. By definition, the pulse width is constant in PFM mode. For the HVBUCK, the off time is constant with a variable on time.

Table 24 shows the recommended configuration for PFM T_{ON} and T_{OFF} values depending on the switching frequency of 450 kHz and the selected output voltage in LPON.

Table 24. Recommended configuration for T_{ON} and T_{OFF} in PFM mode

f_{SW}	450 kHz		2.2 MHz	
$V_{out,LPON}$	3.3 V	5.0 V	3.3 V	5.0 V
T_{ON}	**10** : 1221 ns	**11** : 1772.5 ns	**11** : 305 ns	**11** : 386 ns
T_{OFF}	**10** : 1725 ns	**01** : 605 ns	**01** : 250 ns	**01** : 250 ns

9.4 BUCK_SS _OTP

The HVBUCK soft start (SS) represents the length of the time in microseconds allocated for the HVBUCK start during the power-up sequence. The available values for HVBUCK SS are 269 µs, 538 µs, 1077 µs, and 2150 µs.

The minimum SS duration to be used is given by: $SS_{min} = \frac{V_{out} * C_{out\_max}}{i_{SS,max}}$, with SS in µs, $i_{SS,max}$ = 0.3 A, and C_{out_max} in µF.

Figure 47 shows the recommended configuration for HVBUCK SS value for a maximum SS current of 300 mA, and 3.3 V or 5.0 V as output voltage.

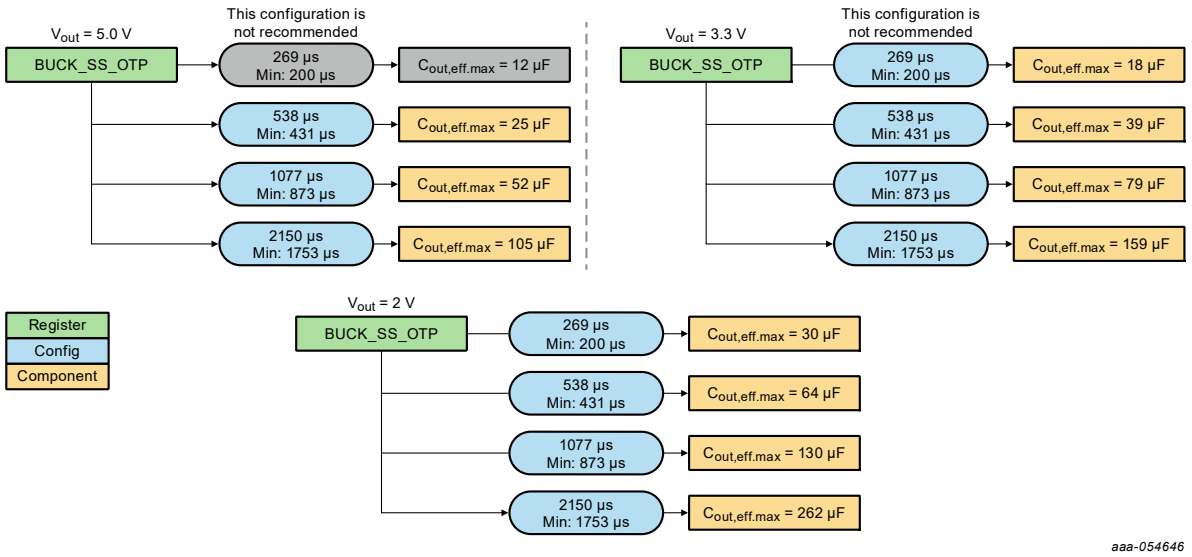

Figure 47. BUCK_SS_OTP configuration recommendations

As an example, the current limit would be reached if the fastest SS (BUCK_SS_OTP set to 00) was selected when the HVBUCK is used at 450 kHz operating frequency with a 40 µF output capacitor, therefore it should not be used.

9.5 BUCK_SRHSOFF_OTP and BUCK_SRHSON_OTP

The HVBUCK high-side turn-on slew rate and turn-off slew rate is configured as a suitable compromise between efficiency and electromagnetic compatibility (EMC) considerations on emissions. These values are set in OTP registers, and can be reconfigured by SPI in the course of the product's life using the BUCK_SRHSOFF and BUCK_SRHSON bits in M_REG_CTRL register.

The EMC validation was performed using BUCK_SRHSOFF and BUCK_SRHSON equal to 10 ns. Efficiency results shown in the FS2400 data sheet were also performed using these settings. Therefore, NXP recommends using these values as best compromise between EMC and efficiency performance.

When $V_{SUP} > V_{SUP\_OV}$, high-side slew rates automatically switch to the fastest values in order to ensure a proper T_{ON} of the high-side MOSFET.

When using the switching frequency of 2.2 MHz:

- the slowest slew-rate values should not be used as T_{ON} is very small,
- the fastest slew-rate values are not recommended for EMC considerations.

9.6 BUCK_AVG_OC_PWM and BUCK_PK_OC_PWM_OTP

The HVBUCK average current sensing uses successive sensing during the T_{ON} and T_{OFF} phases of the switching to compute a mean and compares it with the average limit. The HVBUCK peak limit detection compares the inductor current during the T_{ON} phase and compares it with the peak limit.

The HVBUCK average and peak overcurrent threshold selection is done considering the use-case requirements for the average current load, and the current ripple to determine the peak current limit. The current ripple depends on the inductor value and derating. To select the peak current limit, add $\frac{\Delta I_L}{2}$ to the average current load.

The inductor ripple is computed as: $\Delta I_L = DC \times \frac{V_{in\_max} - V_{out} - I_{AVG\_OC,typ} \times \left(R_{DS,on\_min} + R_{DCR,L}\right)}{f_{sw} \times L}$. The worst case should be considered. This calculation will, in most of the cases, result in picking a peak current limit two codes above the average current limit. For example, if BUCK_AVG_OC_PWM_OTP is set to 0b100 (600 mA typ.), then BUCK_PK_OC_PWM_OTP is set to 0b110 (800 mA typ.).

Figure 48 illustrates how the peak and the average current limit behaves in the case of a short circuit on the regulator output. Figure 48 shows that picking a peak current limit two codes above the average current limit is a good compromise to detect the short circuit fast enough and to allow the loop to regulate without hitting the limit in normal conditions.

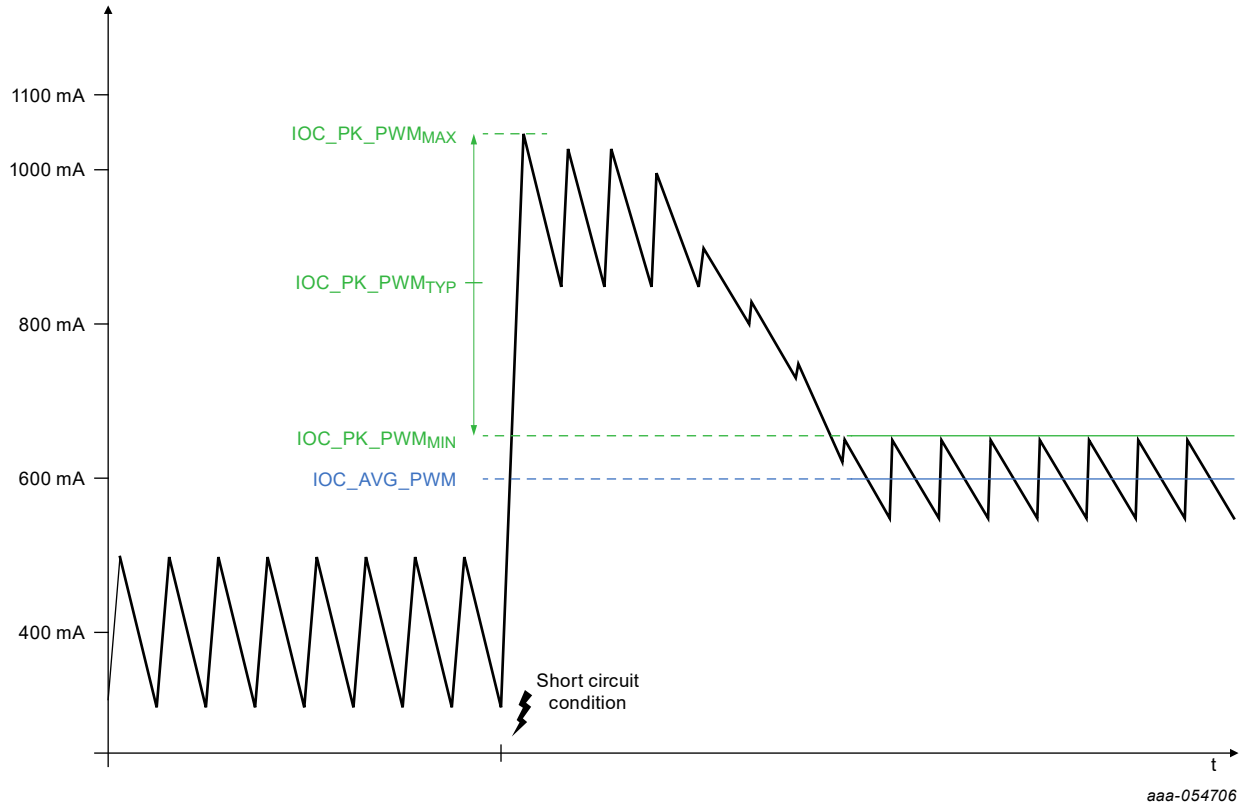

Figure 48. Peak and average current limit

In a short circuit condition, the observed current limit is above the typical limit value. The delay between the comparator triggering at the typical threshold and the high-side MOSFET closing lets the current flow through the high-side.

When using the 2.2 MHz switching frequency, the observed peak current limit is close to $I_{OC\_PK\_PWMMAX}$. As the inductor value is lower for 450 kHz, the current rising slope is bigger and the current increase between the detection of the overcurrent and the opening of the high-side MOSFET will be higher.

9.7 VBOS2V1_SW_LP_EN_OTP

This bit allows the user to close a switch between V1 and VBOS in LPON mode. When supplying VBOS with V1, VBOS benefits from the efficiency of the V1 regulator in PFM mode, and therefore improves the overall current consumption performance of the system.

This bit should be set to 1 only when V1 is set to 3.3 V (or above) in LPON.

NXP recommends setting V1 voltage in LPON to 3.3 V (or above) to reduce the overall system-current consumption.

10 Validation results

This section presents the performance of the FS24 for EMC, ESD, immunity to ISO pulses, and immunity to non-ISO pulses.

10.1 EMC/ESD performances

Compliance with ISO 10605.2008, IEC 62228-3 (2019), IEC61000-4-2, and SAEJ2962-2 (2019) was validated and certified on the FS24 family using the BOM described in Section 4 with a CAN running up to 5 Mbps. The FS24 family was validated in three different use cases described in Table 25.

Table 25. Use-case validations

Use case	V1 voltage	V1 switching frequency	V1 load	V3 voltage	V3 load	CAN supply
2.2M_3.3V_V3	3.3 V	2.2 MHz	0.33 A	5.0 V	0.123 A[1]	V3
2.2M_5.0V_V1	5.0 V	2.2 MHz	0.31 A[1]	3.3 V	0.122 A	V1
450k_3.3V_V3	3.3 V	450 kHz	0.33 A	5.0 V	0.123 A[1]	V3

[1] Current on the regulator = CAN Current (~33.5 mA in Normal mode) + Current in the load.

10.2 Immunity to ISO pulses performances

The following specifications detail test methods and procedures to ensure compatibility to conduct electrical transients of equipment installed on commercial vehicles fitted with 12 V electrical systems.

ISO 7637-2:2011, Road vehicles – Electrical disturbances from conduction and coupling

Part 2: Electrical transient conduction along supply lines only

- Pulse 1
- Pulse 2a, 2b
- Pulse 3a, 3b

ISO 16750-2:2012, Road vehicles – Environmental conditions and testing for electrical and electronic equipment

Part 2: Electrical loads

- LV124 Pulse Cranking profile, formerly pulse 4a, 4b
- Load Dump Test B (previously listed as ISO 7637-2 Pulse 5b)

ISO test pulses are applied to the FS24's global pins. The FS24 was tested with the reference 2.2 MHz BOM presented in this application note. The regulators were loaded at 50 % of their maximum current capability.

10.2.1 General description

Table 26. Regulator pulses description

Regulator pulses description	Type specification
Pulse reference documents Figure 5 — Test pulse 1, page 12. Figure 6 — Test pulse 2a, page 13. Figure 8 — Test pulse 3a, page 15. Figure 9 — Test pulse 3b, page 16.	ISO 7637-2:2011(E)
Figure 11: Cold start test pulse, page 29. 4a, 4b (former cranking pulses).	VW 80000: 2009-10

Table 26. Regulator pulses description*...continued*

Regulator pulses description	Type specification
Figure 9: — Test with centralized load dump suppression, (Test pulse 5b), page 12.	ISO 16750-2:2012(E)

- **Pulse 1:** Ua = 13.5 V, Us = –150 V, Ri = 10 Ω, Td = 2 ms, Tr = 1 µs, T 1 = 0.5 s, T2 = 200 ms, T3 < 100 µs, 500 pulses
- **Pulse 2a:** Ua = 13.5 V, Us = 112 V, Ri = 2 Ω, Td = 50 µs, Tr = 1 µs, T1 = 0.2 s, 500 pulses
- **Pulse 3a:** Ua = 13.5 V, Us = –220 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 hour
- **Pulse 3b:** Ua = 13.5 V, Us = 150 V, Ri = 50 Ω, Td = 150 ns, Tr = 5 ns, T1 = 100 µs, T4 = 10 ms, T5 = 90 ms, 1 hour
- **Pulse 4a:** Ub = 11 V, Ut = Us = 4.5 V, Ua = 6.5V, Ur = 2 V, Tf = 1 ms, T4 = T5 = 0, T6 = 19 ms, T7 = 50 ms, T8 = 10 s, Tr = 100 ms, F = 2 Hz, 10 cycles at intervals of 2 s
- **Pulse 4b:** Ub = 11 V, Ut = 3.2 V, Us = 5.0 V, Ua = 6.0 V, Ur = 2 V, Tf = 1 ms, T4 = 19 ms, T5 = 1 ms, T6 = 329 ms, T7 = 50 ms, T8 = 10 s, Tr = 100 ms, F = 2Hz, 10 cycles at intervals of 2 s
- **Pulse 5b:** Ua = 12 V, Us = 35 V, Ri = 4 Ω, Td = 400 ms, Tr = 5 ms, 5 pulses at intervals of 1 min

10.2.2 Test setup

The ISO test campaign is performed at room temperature. The FS24 is used with all regulators loaded except in Low-power mode.

In Low-power mode, the positive energy from pulses 2a and 3b are stored in the input capacitors and cannot be discharged because of low-power consumption. Therefore, external components are mandatory to discharge the input capacitors and protect the FS24. The external circuitry used on the VSUP line is described in Section 3.

The FS24 regulators are loaded according to Table 27:

Table 27. ISO pulse regulator settings in Normal mode

Regulators	Output voltage (V)	Load (A)
V1 – HVBUCK	3.3 V	200 mA
V3 - HVLDO	5 V	50 mA

10.2.3 Results

Table 28. ISO pulse results

FS24 mode	Pulse pins	ISO spec pulse	Description	Severity level	Class
Normal	VSUP (Pulse applied to VBAT)	**1**	Negative transient, inductive parallel load	–150 V	**Class C**
		2a	Positive spikes, current interruption	112 V	**Class A**
		3a	Negative transients influenced by L and C of wiring harness	–220 V	**Class A**
		3b	Positive transients, influenced by L and C of wiring harness	150 V	**Class A**
		4a LV124	Cold cranking	Normal	**Class C** (As V3 = 5 V)
		4b	Cold cranking	Severe	**Class C**
		5b ISO 16750-2:2012	Load dump suppressed	79 V Suppressed 35 V	**Class A**

Table 28. ISO pulse results*...continued*

FS24 mode	Pulse pins	ISO spec pulse	Description	Severity level	Class
Normal	WAKE2, HID1, HVIO1, LIMP0	**1**	Negative transient, inductive parallel load	–150 V	**Class A**
		2a	Positive spikes, current interruption	112 V	**Class A**
		3a	Negative transients influenced by L and C of wiring harness	–220 V	**Class A**
		3b	Positive transients, influenced by L and C of wiring harness	150 V	**Class A**
	CANH, CANL (CAN FD 2M without CMC)	**1**	Negative transient, inductive parallel load	–80 V –100 V	**Class A** **Class C**
		2a	Positive spikes, current interruption	75 V	**Class A**
		3a	Negative transients influenced by L and C of wiring harness	–100 V –150 V	**Class A** **Class C**
		3b	Positive transients, influenced by L and C of wiring harness	100 V	**Class A**
Low power	VSUP (Pulse applied to VBAT)	**2a**	Positive spikes, current interruption	112 V	**Class A**[1]
		3b	Positive transients, influenced by L and C of wiring harness	150 V	**Class A**[1]

[1] External components required on VSUP line.

Class A: All functions stay within the specification limits during all the exposure.

- RSTb and/or LIMP0 activation can’t occur

Class C: All functions return automatically to Normal mode and within the specification limits after exposure is removed

- RSTb and/or LIMP0 activation can occur

10.3 Immunity to non-ISO pulses performances

These non-standard transient pulses have been included to produce transient waveforms that are absent from ISO 7637-2, but are prevalent in the vehicle’s electrical-power distribution system.

Each pulse simulates a noisy battery environment. While a signal is applied, the FS24 needs to ensure product functionalities. Pulses are coming from car industry experience (carmakers, NXP, and so.).

NXP has built an additional pulse database on top of the ISO 7637-2:2011, ISO 16750-2:2012 standards based on:

- Standards, such as LV124 and in part ISO 7637
- OEM, such as VW8000, FMC1278
- OEM and Tier1 specific

The FS24 was tested with the reference 2.2 MHz BOM presented in this application note. The pulses have been run at an ambient temperature of -40 °C, 25 °C, and 125 °C. At 25 °C, the tests have been done at both no load and 50 % load conditions. For other temperatures, it has been done at 50 % load of the regulator's max current capability.

10.3.1 Test results

Table 29 shows all the pulses run during the non-ISO test campaign.

Table 29. Test results

Pulse name	Signal Description	No. of cycles	Result
Overvoltage	36 V for one hour	1	A/C (HT)
VW80000 E03b (LV124)	**Cold cranking** V1 10.8 V, V2 6 V, V3 8 V, V4 9 V. T1 5 ms, t2 20 ms, t3 2 s, t4 180 ms, t5 1 ms, t6 300 ms, t7 2 ms, t8 1 s	1	A
VW800000-E04 (LV124)	Jumpstart from 0 V to 26 V	1	C
VW80000 E-07 (LV124)	Ubmax = 16 V Ubmin = 6 V, minimum voltage = 0 V. dv/dt = 0.5V/min Slope 0.5 V/min	1	C
VW80000 E-07b (LV124)	Slow decrease and increase of the supply voltage with a superimposed 50 Hz sinus	1	C
VW80000 E-08 (LV124)	Ubmax = 16V Ubmin = 6V Slope = 0.5 V/min Holding at 0 V = 1 min Tr < 0.5 s	1	C
VW80000 E-10 (LV124)	T1 = 100 µs to 1 ms with interval of 100 µs T1 = 1 ms to 10 ms with interval of 1 ms T1 = 10 ms to 100 ms with interval of 10 ms T1 = 100 ms to 2 s with interval of 100 ms	1	C
FORD CI260A (FMC1278)	Up = 13.5V T= **100 µs / 300 µs / 500 µs** / 2 ms / 5 ms / 10 ms / 30 ms / 50 ms	3	**A**/C
FORD CI260B (FMC1278)	Up = 13.5V T= 100 µs / 300 µs / 500 µs / 2 ms / 5 ms / 10 ms / 30 ms / 50 ms	3	C
FORD CI260C (FMC1278)	Up = 13.5V T= 100 µs / 300 µs / 500 µs	3	A
FORD CI260D (FMC1278)	Up = 13.5V / U1 = 5V T= **100µs / 300 µs / 500 µs** / 2 ms / 5 ms / 10 ms / 30 ms / 50 ms	10	**A**/C
FORD CI230B (FMC1278)	U1 = 5V	1	C
FORD CI231 (FMC1278)	Ub = 12V, Us = -6V	1	A
JLR CI265 FTBN	Pseudo-random interruption Tmin = 2 ms Tmax = 3 ms, 6 ms, 9 ms, 12 ms, 18 ms, 24 ms, 36 ms, 48 ms, 60 ms, 100 ms, 200 ms, 1 s, 20 s	1	C
Triangular pulse 1 (1801_TRI) VBAT_start = 12 V, VBAT_stop = 0V, VBAT_max = 13.5 V	Slope = 0.1 V / µs	3	A
	Slope = 1 V / s	3	C
	Slope = 1 V / min	1	C
Triangular pulse 2 (NXP07_TRI) VBAT_start = 12 V, VBAT_stop = 0 V	Fall time from 2 min to 30 min by step of 5 min	1	C
	Fall time from 1 h to 3 h by step of 2 h	1	C
	Rise time from 2 min to 30 min by step of 5 min	1	C
	Rise time from 1 h to 3 h by step of 2 h	1	C
Triangular pulse 3 (2001_TRI)	Vbat_init=Vbat_final = 12 V, Four successive triangular signal between 4.5 V and 5.5 V Periods = 0.4 s, 0.6 s, 1 s, 1.4 s	1	C
Triangular pulse 4 (1804_TRI)	Vbat_init = Vbat_final = 12 V, Triangular signal between 5 and 6 V during 20 s Periods = 0.2 s, 0.5 s, 0.75 s, 1 s	1	C
Slow brownout/recovery (NXP03_BO) VBAT_high = 9 V, VBAT_low = 0 V	Tf = 28800 s Tr = 7200 s	1	C

Table 29. Test results...*continued*

Pulse name	Signal Description	No. of cycles	Result
Fast brownout (1805_BO)	Drop from 12 V to 5 V in 5 ms Ramp to 6 V in 50 ms 20 s step at 6 V Recovery to 12 V in 100 ms	1	C
Brownout (1811_BO)	Drop from 12 V to U1 in 20 ms Steady at V1 for 20 s Ramp to 12 V in 100 ms Steady at 12 V for 1 s Ramp to 13.5 V in 100 ms U1 is 2.7 V to 5 V by step of 100 mV	1	C
Re-init pulses 1 (NXP02_RI) VBAT = 13.5 V	tr/tf = 1 ms, td = 5 s, T = 10 s, 20 steps by 5 %	1	C
Re-init pulses 2 (NXP05_RI)	Vbat_high = 13.5 V, ΔV = 0.5 V T_high = 10s, T_low = 5s/100ms/40ms	1	C
Square cranking pulse (1601_SQR)	Vbat_init = 12 V, Vbat_high = 9 V, Vbat_low = 2 V to 6 V (0.2 V step), Vbat_end = 12 V F = 2.5 Hz, 10 Hz, 20 Hz during 2 s at each frequency,	1	A (from 5.4 V)
Square pulse (1810_SQR)	V_high = 12 V, V_low = 0 V Frequency = 10, 1, 0.5, 0.25 Hz, Duty cycle = 0.5 for 10 cycles	1	C
Sinusoidal Cranking Pulse (1803_SIN)	Vbat_init = 12 V, Vbat_low = 4.5 V to 5 V, Vac = 2 Vpp with 100 mV sweep up to 6.5 V, Freq = 30 Hz, Vbat_end = 12 V	1	C
Slow Ramp-up Pulse (1901_SR)	10 ramp up from 0 V to 13.5 V dV/dt = 1 V/µs, 10 mV/µs, 10 mV/ms	1	C
Battery voltage dropout (NXP01_DO) U_{ON} = 13.5 V, U_{OFF} = 0 V, tr/f ≤ 1 µs, Ri = 0.01 Ω	tON = 0.9 ms, tOFF = 0.1 ms	4000	A
	tON = 9 ms, tOFF = 1 ms	10	C
	tON = 9 ms, tOFF = 6 ms	10	C
	tON = 200 ms, tOFF = 10 ms	10	C
	tON = 200 ms, tOFF = 100 ms	10	C
Dropout pulse (2201_DO)	30 Dropout shapes from 12 V to 0 V: T_init = 100 ms, T_final = 2 s • **T_low from 50 µs to 500 µs (step of 50 µs)** • T_low from 1 ms to 20 ms (step of 1 ms)	1	**A**/C
Successive dropout pulse (0401_DO)	Four successive dropout from 13 V to 0 V T_high = 40 ms, T_low = 3 ms	1	C

11 Revision history

Table 30. Revision history

Document ID	Release date	Description
AN14183 v2.0	8 Nov 2024	• Changed security status from confidential to public • Updated legal information
AN14183 v.1.0	20 March 2024	Initial version

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