AN14420

On-The-Fly Audio PLL Frequency Change

Rev. 1.0 — 22 October 2024 Application note

Document information

Information	Content
Keywords	AN14420, Audio PLL, clock synchronization, i.MX RT1170
Abstract	In this application note, Audio PLL is introduced to realize clock synchronization on the i.MX RT1170 family.

1 Introduction

In any audio streaming system, where audio source and destination have different clock source as shown in Figure 1, there must be clock drift to some extent. Therefore, the buffer eventually overruns or underruns, which lead to bad audio quality like audio skipping or dropout.

To avoid these troubles, the destination clock must be synchronized with the audio source clock, by changing the PLL frequency occasionally on the fly. It is called clock synchronization. In this application note, Audio PLL is introduced to realize clock synchronization on the i.MX RT1170 family.

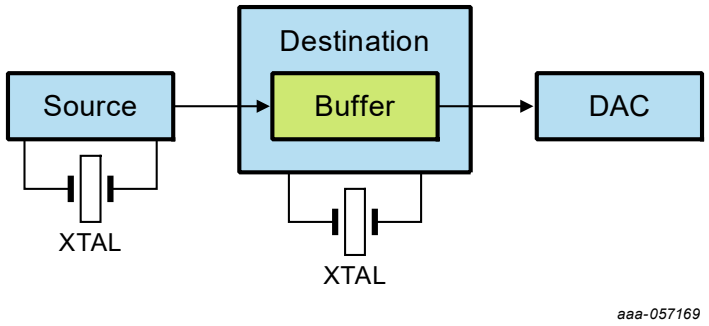

Figure 1. Audio streaming system working on different clock source

2 Audio PLL

Audio PLL is a fractional PLL (Figure 2), whose frequency is expressed in Equation (1):

$$f_{out} = f_{ref}\left(\text{DIVIDER} + \frac{\text{NUMERATOR}}{\text{DENOMINATOR}}\right)\frac{1}{\text{POST DIVIDER}} \quad (1)$$

To adjust the frequency accurately, the fractional part can be used. The valid range is -2 to +2. The numerator is signed 30 bits and the denominator is unsigned 30 bits.

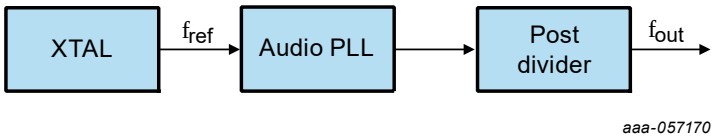

Figure 2. Audio PLL inputs the crystal's reference clock and outputs to the post divider

One of the big characteristics of the Audio PLL is that the numerator can be changed on the fly. With this feature, the destination clock can be synchronized with the audio source clock on the fly.

Note: *The numerator cannot be changed more frequently than f_{ref}/200 times per second because the maximum lock time is 200/f_{ref}.*

The frequency of Audio PLL cannot be changed more than 200 kHz on the fly without significant glitch.

3 Software implementation

This section explains how to read/write Audio PLL in your software.

3.1 Analog IP interface

The chip has various analog IP and components that are controlled via an AI interface. Audio PLL is one of them. To perform register accesses through the AI interface, follow the following steps:

- To perform a write operation of an analog component AI interface, perform the following steps:
  1. Write *AI_CTRL register
  2. Write *AI_WDATA
  3. Write *CTRL IP Toggle
- To perform a read operation of an analog component AI interface, perform the following steps:
  1. Write *AI_CTRL register
  2. Write *CTRL IP Toggle
  3. Read *CTRL
  4. Read *AI_RDATA

For more details, refer to the *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM). The ANATOP_AI_Read() and ANATOP_AI_Write() functions in our SDK can be used to read/write Audio PLL registers instead of implementing it on your own.

3.2 Source code

In the project associated with this document, the Audio PLL's numerator is swept every second by an interrupt while playing 220 Hz sound via I2S on MIMXRT1170-EVKB. By doing so, the SYNC signal (sampling rate) is swept between 15.98 kHz to 16.02 kHz on the fly.

Concretely, the handler of the GPT is called every second while playing the 220 Hz sound via I2S. The GPT handler is shown as follows:

```
void EXAMPLE_GPT_IRQHandler(void)
{
    uint32_t numer;
    GPT_ClearStatusFlags(EXAMPLE_GPT, kGPT_OutputCompare1Flag);

    if (ANADIG_PLL->PLL_AUDIO_CTRL &
 ANADIG_PLL_PLL_AUDIO_CTRL_PLL_AUDIO_STABLE_MASK == 0)
    {
        assert(false);
    }
    numer = ANATOP_AI_Read(kAI_Itf_Audio, kAI_PLLAUDIO_CTRL2) &
 ANADIG_PLL_PLL_AUDIO_NUMERATOR_NUM_MASK;
    numer = ANADIG_PLL_PLL_AUDIO_NUMERATOR_NUM(get_next_numer(numer));
    ANATOP_AI_Write(kAI_Itf_Audio, kAI_PLLAUDIO_CTRL2, numer);
    PRINTF("%d Hz\n", CLOCK_GetRootClockFreq(kCLOCK_Root_Sai1) / (24 *
 DEMO_AUDIO_BIT_WIDTH * DEMO_AUDIO_DATA_CHANNEL));

#if defined __CORTEX_M && (__CORTEX_M == 4U || __CORTEX_M == 7U)
    __DSB();
#endif
}
```

At first, the PLL_AUDIO_STABLE register is read to check if the PLL is locked or not. It must be locked because the period of the interrupt is bigger than the maximum lock time. If PLL is locked, the numerator is read and written via an AI Interface. At last, the frequency of the SYNC signal is logged in the serial console.

4 Running the demo

To run the demo, perform the following steps:

1. Install the MCUXpresso SDK 2.13.1 in the MCUXpresso IDE and open the project.
2. Connect a USB cable between the host PC and the MIMXRT1170-EVKB.

3. Ensure that the below registers are mounted:
   R2001, R2002, R2003, R2004, R2005, R2006, and R2007
4. To observe the I2S and analog signals, connect an oscilloscope to the signals in Table 1.
5. Build and download the program to the target board.

Table 1. I2S and analog signal

Pin	Signal
J97	BCLK
J98	SYNC
J101-1	R
J101-4	L
J101-5	GND

You can observe in Figure 3 that the SYNC signal is swept between 15.98 kHz to 16.02 kHz on the fly.

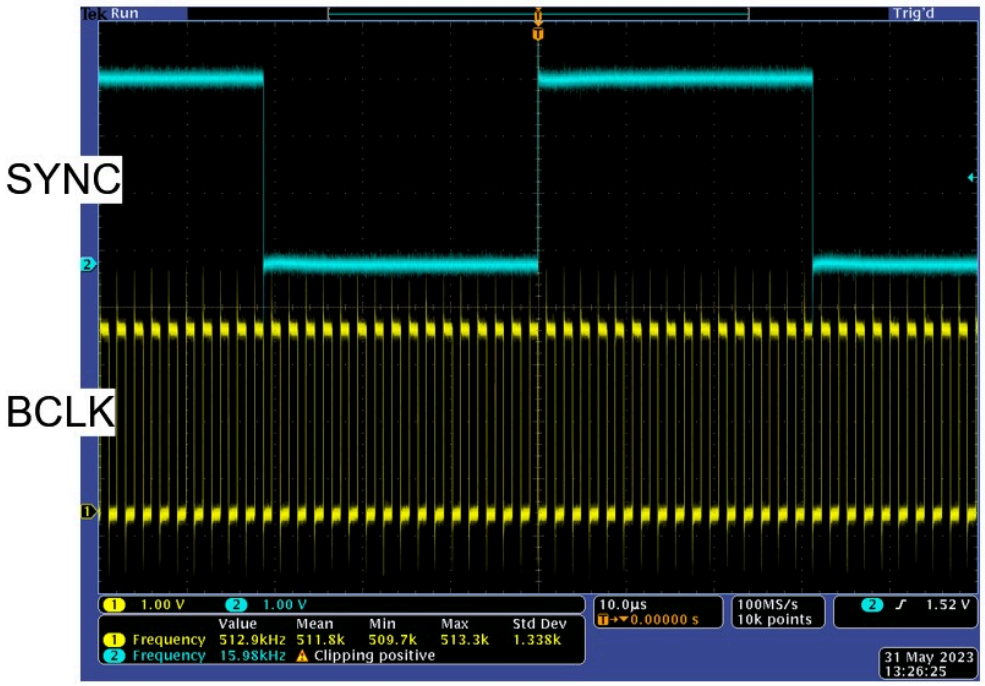

Figure 3. SYNC signal swept between 15.98 kHz to 16.02 kHz on the fly

You can observe in Figure 4 that the analog signal is also swept depending on the SYNC signal on the fly.

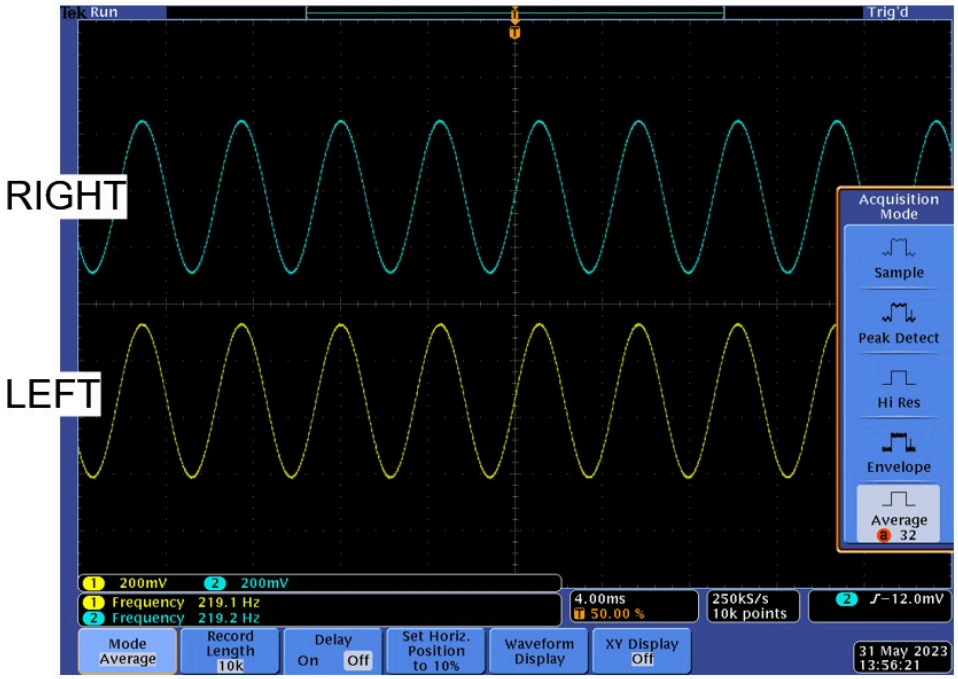

Figure 4. Analog signal is also swept depending on the SYNC signal on the fly

5 Conclusion

This application note concludes that the clock synchronization can be realized by changing the Audio PLL's numerator on the fly.

6 Note about the source code in the document

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7 Revision history

Table 2 summarizes the revisions to this document.

Table 2. Revision history

Document ID	Release date	Description
AN14420 v.1.0	22 October 2024	Initial public release

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