AN14450

i.MX RT117x ADC Clocks and IO Selection

Rev. 2.0 — 5 November 2024 Application note

Document information

Information	Content
Keywords	AN14450, i.MX RT117x, clock sources, ADC
Abstract	This document covers design considerations to avoid possible issues related to synchronicity and noise contamination.

1 Introduction

The i.MX RT117x chips feature two integrated 12-bit ADCs and a managing peripheral known as the ADC external trigger controller (ADC_ETC). To achieve maximum performance and avoid possible issues, use of these peripherals requires consideration of several design factors.

This document covers design considerations to avoid possible issues related to synchronicity and noise contamination. Under certain circumstances, the flexibility of the ADC_ETC/ADC1/ADC2 setups can have aspects that can affect accuracy and crosstalk, although to a small degree. These effects are easily mitigated with awareness and up-front design.

2 Clocking architecture

The ADC_ETC is well suited for motor controller designs using the PWM peripherals. These designs typically use multiple ADC channels and managing the triggering and FIFO can complicate the software.

2.1 Clock sources

As shown in Figure 1, the ipg_clk (bus_clk) clocks the ADC_ETC. Each ADC has its own clock and can have different clock sources.

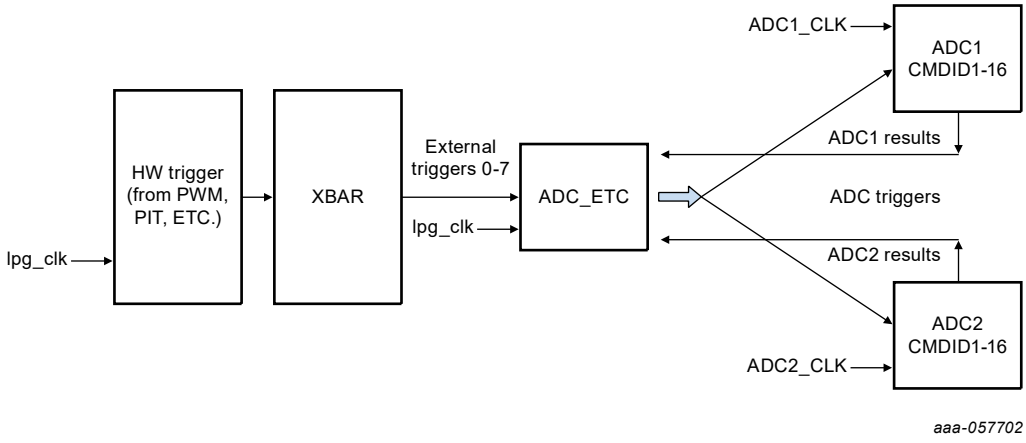

Figure 1. HW trigger/ADC_ETC/ADC1/ADC2 clock sources

3 Clock selection considerations

Selecting the clock sources for the ADCs requires the recognition of the attributes of highly synchronous systems. The ipg_clk and its equivalent clocks synchronize many peripherals. The ipg_clk also clocks the ADC_ETC.

3.1 ADC_ETC and ADC clocks

The ADCs have clock branches and the triggers from the ADC_ETC are synchronized to the ADC clock when a trigger is received. The exact clock-synchronized output depends on the phase relationship between the ipg_clk and the adc_clk. This relationship can change slightly after a reset or power cycle, but remains consistent after the systems are up and running.

The ipg_clk also clocks the external trigger sources to the ADC_ETC (PWM, PIT, and so on).

3.2 Noise synchronicity

Depending on the layout of the board and how peripherals are used, a small amount of unavoidable noise can be coupled into the ADC conversion. Nevertheless, the ADC still meets its accuracy specifications. This noise from the peripherals can be data or clock noise that is synchronized to the ipg_clk.

If the clock sources (ipg_clk and adc_clk) are in phase and the hardware trigger generated to the ADC_ETC is also derived from the ipg_clk and is repetitive in terms of timing, then the sample times of the ADC are precise from conversion to conversion.

However, this precision in sample times can sometimes cause an issue. The precise timing of the conversion can capture low-level noise that can be synchronized to the ipg_clk. It generates the appearance of a low-level repetitive signal in the ADC data, which can be observed in an FFT of the ADC.

3.3 Crosstalk synchronicity

Another possible issue arises from the signals between the two ADCs. If both ADCs are using the same clock source, it is possible to experience some crosstalk between two ADC inputs (ADC1 and ADC2). The level of crosstalk can vary from reset-to-reset or after a power cycle due to the slight timing variations in the relative clock phases.

The ADC trigger can occur in two cases as follows:

1. The ADC_ETC is executing a synchronized conversion, where both ADCs receive a trigger simultaneously. The two channels that are converting simultaneously are possibly susceptible.
2. The ADCs are triggered in some other way, at approximately the same time, and a high conversion rate.

4 Mitigation of noise and crosstalk synchronicity

This section explains the method to minimize the effects of noise synchronicity and crosstalk synchronicity requiring careful planning.

4.1 Noise synchronicity mitigation

To avoid the impact of noise synchronicity, a simple method can be used. This effect depends on precise synchronization between the clock sources of the noise, the trigger, and the ADC conversion. Therefore, the easiest approach is to employ a clock source for the ADC that is not phase-locked to the ipg_clk.

The ipg_clk is typically derived from one of the PLLs, which are sourced from the 24 MHz crystal oscillator. All the PLLs are driven from the crystal oscillator, therefore, they are all phase-locked after a reset or power up.

The i.MX RT1170 has two other built-in oscillators, the RC48 and the RC400. These oscillators are internal that are not sourced or referenced to the crystal oscillator. Using either of these two oscillators for the adc_clk prevents the noise synchronicity.

4.2 Crosstalk synchronicity mitigation

A solution similar to the noise synchronicity also helps mitigate the crosstalk synchronicity.

The IOs also play a role in the crosstalk synchronization. Avoid simultaneous conversion for the IOs, GPIO_AD_12 through GPIO_AD_17, inclusive.

Both ADCs share these IOs. They are ADC inputs 3A, 3B, 4A, 4B, 5A, and 5B on each ADC.

To mitigate any changes in crosstalk between the referenced channels, the following two items are recommended:

1. Use IOs GPIO_AD_12 through GPIO_AD_17 for ADC inputs, but do not use them in a mode that is simultaneously triggered with another channel.
2. Use a different clock source that is different for each ADC. For example, the use of a PLL on ADC1 and the RC400 on ADC2 eliminates this issue.

5 Conclusions

These minor issues involve low-level signal levels and have minimal impact on most implementations. Addressing these issues requires careful planning and detailed implementation.

6 Revision history

Table 1 summarizes the revisions to this document.

Table 1. Revision history

Document ID	Release date	Description
AN14450 v.2.0	5 November 2024	• Updated RT117x to i.MX RT117x • Minor editorial changes
AN14450 v.1.0	28 October 2024	Initial public release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

1 Introduction 2
2 Clocking architecture 2
2.1 Clock sources 2
3 Clock selection considerations 2
3.1 ADC_ETC and ADC clocks 2
3.2 Noise synchronicity 3
3.3 Crosstalk synchronicity 3
4 Mitigation of noise and crosstalk synchronicity 3
4.1 Noise synchronicity mitigation 3
4.2 Crosstalk synchronicity mitigation 3
5 Conclusions 4
6 Revision history 4
Legal information 5