AN14452

TJA1446, TJA1466 application note

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Application note

Document information

Information	Content
Keywords	TJA1446, TJA1466, CAN transceiver, GPIO, CAN FD, CAN XL passive, CAN SIC, partial networking, selective wake-up, watchdog, V_{IO} monitoring
Abstract	This application note covers hardware and software application aspects of the TJA1446 and TJA1466 CAN transceivers for automotive applications. It assumes that the reader is familiar with the TJA1446 and TJA1466 data sheets, which describe the functionality of these devices.

1 Introduction

The TJA1446 [1] and TJA1466 [2] are high-speed CAN transceiver ICs that provide an interface between a controller area network (CAN) or CAN FD (flexible data rate) protocol controller and the physical two-wire CAN bus. These products implement the CAN physical layer as defined in ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5, making them fully interoperable with high-speed classical CAN and CAN FD transceivers.

Both devices support CAN partial networking (PN) by means of selective wake-up functionality, making them the ideal choice for CAN system implementations where only nodes that are needed can be activated at any time. Nodes that are not needed for the function being performed can be powered down to minimize system power consumption, even when CAN bus traffic is running.

Table 1 provides an overview of the device variants supported by this application note.

Table 1. Transceiver variants

Feature	TJA1446A	TJA1446B	TJA1446C	TJA1466A	TJA1466B	TJA1466C
CAN transceiver type	HS-CAN	HS-CAN	HS-CAN	CAN SIC	CAN SIC	CAN SIC
Selective wake-up for partial networking	✓	✓	✓	✓	✓	✓
Option 'CAN FD passive'	✓	✓	✓	✓	✓	✓
Option 'CAN XL passive'				✓	✓	✓
Watchdog and V_{IO} under/ overvoltage detection	✓	✓	✓	✓	✓	✓
Reset and fail-safe/limp home output	✓	✓	✓	✓	✓	✓
2 x GPIO	✓	✓	✓	✓	✓	✓
V_{IO} voltage range	1.8 V	3.3 V	3.3 V - 5 V	1.8 V	3.3 V	3.3 V - 5 V

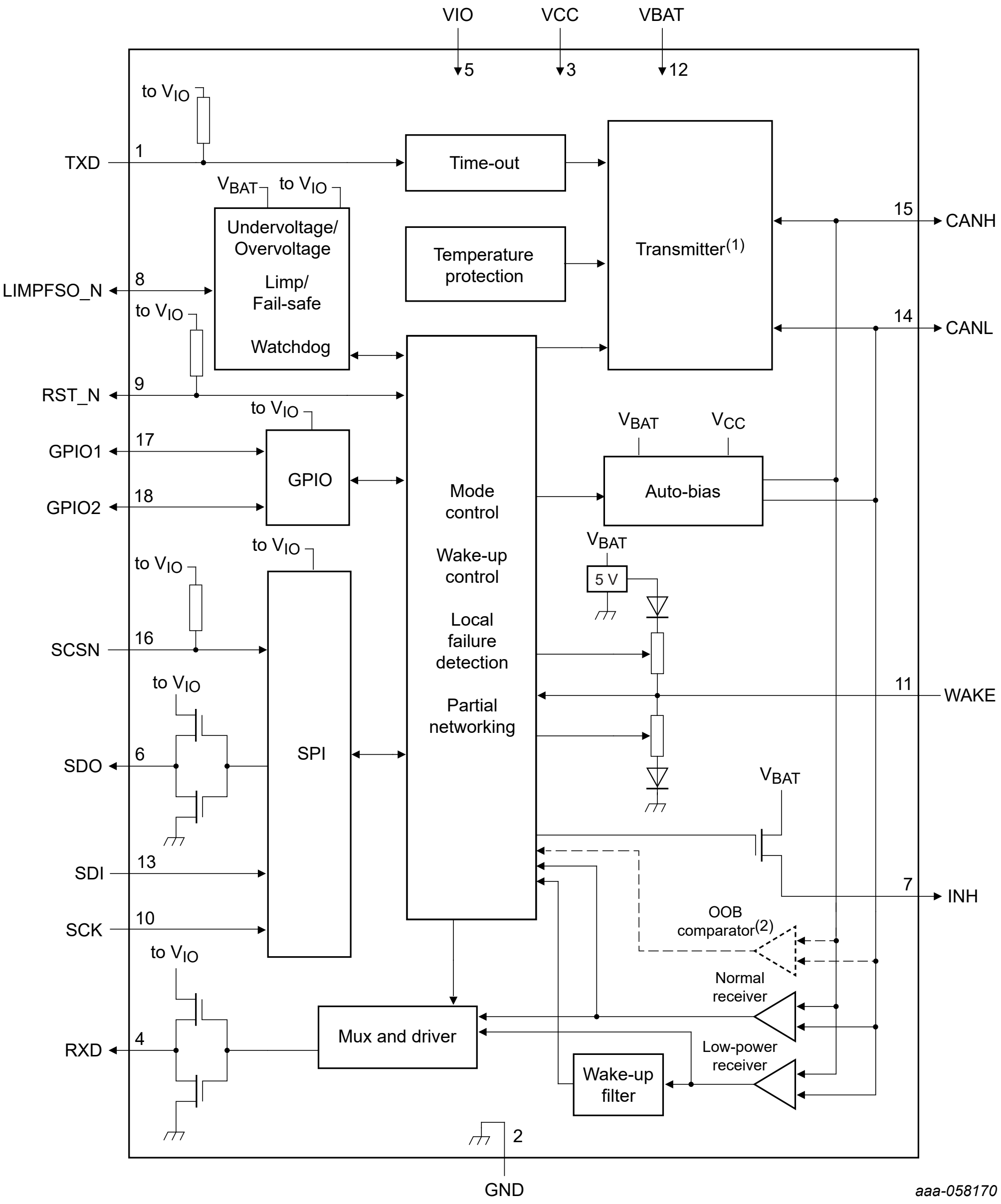
The TJA1446/66 includes a comprehensive set of features including two configurable general-purpose I/O pins (GPIO), an SPI for configuration, mode control and diagnostics, a question & answer (Q&A) watchdog with dedicated reset and failsafe/limp home pins and accurate V_{IO} undervoltage and overvoltage monitoring.

The TJA1446/66 can be configured to ignore CAN FD frames while waiting for a valid wake-up frame. This additional feature of partial networking, called CAN FD passive, is the perfect fit for networks that support a mix of classical CAN and CAN FD communications. The TJA1466 features an additional option that allows CAN XL frames to be ignored, even when they are transmitted in FAST mode. This ‘CAN XL passive’ feature supports a mix of all three, classical CAN, CAN FD and CAN XL communications.

The TJA1466 features CAN signal improvement capability (SIC), as defined in ISO 11898-2:2024. CAN signal improvement significantly reduces signal ringing on a network, allowing for reliable 2 Mbit/s and 5 Mbit/s CAN FD communication in larger and more complex topologies. Tight bit timing symmetry enables CAN FD communication up to 8 Mbit/s.

The type number suffix A, B or C indicates which MCU port interface V_{IO} voltage the variant was designed to be used with.

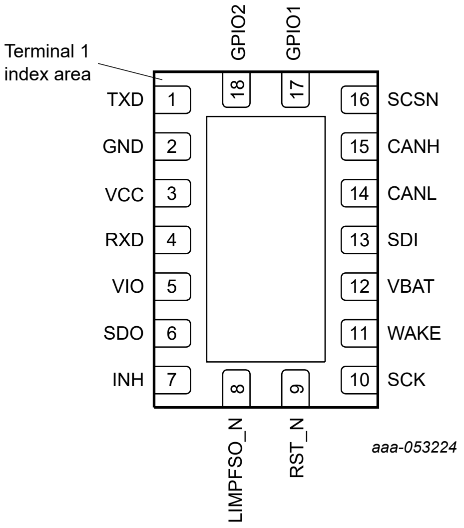
The TJA1446 and TJA1466 share the same block diagram (Figure 1) and pinning (Figure 2).



(1) TJA1446: HS CAN transmitter; TJA1466: CAN SIC transmitter

(2) TJA1466 only, for optional CAN XL FAST mode tolerance

Figure 1. TJA1446/TJA1466 block diagram



Transparent top view

Figure 2. Pin configuration diagram - TJA1446/66, DHVQFN18

2 Hardware design

In this section, typical hardware applications using the transceiver are discussed. For functional safety aspects, see the related safety manual [4].

2.1 Power supply

2.1.1 Power supply configuration

2.1.1.1 Supply pins VBAT, VCC and VIO

A TJA1446/66 device needs power supply connections on three pins:

- Pin VCC must be connected to a regulated 5 V supply (V_{CC}). Optionally, V_{CC} can be turned off while the device is in a low-power mode (Standby, Sleep or low-power ListenOnly mode).
- Pin VBAT can be connected to the rectified and filtered 12 V car battery (V_{BAT}), or to V_{CC} (5 V). It is the main power supply pin for the device and must be supplied in all operating modes. When V_{CC} is expected to be turned off in a low-power mode, V_{BAT} must be higher than 5.5 V for proper CAN bias generation.
- Pin VIO should be connected to the same regulated 1.8 V, 3.3 V or 5 V V_{IO} supply rail supplying the port pins of the connected microcontroller (MCU). The device variant (type number A, B or C) must be selected to match the intended V_{IO} level (see Table 2). In a typical application, V_{IO} is turned off while the device is in Sleep mode.

The power supply rails can be ramped up or down in arbitrary order. However, to ensure the device powers up without ending up in Sleep/Fail-safe mode at an arbitrary V_{BAT} ramp-up speed:

- V_{IO} must have ramped up within $t_{to(rst)}$ after V_{BAT} exceeded the undervoltage detection threshold, $V_{uvd(VBAT)}$ and
- the voltage regulator used for V_{IO} must provide an output voltage higher than the maximum undervoltage release threshold ($V_{uvr(max)}$ = 3.135 V for B/C variants) while V_{BAT} is at the minimum undervoltage detection threshold ($V_{uvd(min)}$ = 4.25 V).

Otherwise, the transceiver could start up in Sleep/Fail-safe mode if V_{BAT} ramp-up is very slow.

Table 2. Device variant selection based on V_{IO}

Combinations marked '-' are not feasible

V_{IO}	A variant	B variant	C variant
1.8 V	recommended	-	-
3.3 V	-	recommended	not recommended
5 V	-	-	recommended

2.1.1.2 INH output pin

The INH output should be used for automatic direct on/off control of the voltage regulator(s) (see also Section 2.1.4).

However, when pins VBAT and VCC are both supplied from V_{CC}, V_{CC} must be available while the device is in Sleep mode. Otherwise, the wake-up functionality of the device would be lost.

When the V_{BAT} supply level sits at, or around, the undervoltage detection threshold $V_{uvd(VBAT)}$ for some time, the INH signal may switch frequently on and off. The application must tolerate this behavior.

When INH is not used, it can be left unconnected or connected to pin VBAT.

2.1.1.3 Power supply configuration examples

Figure 3 and Figure 4 illustrate typical power supply configuration examples for, respectively, V_{IO} = 3.3 V/1.8 V and V_{IO} = 5 V. In both cases, the INH pin controls the voltage regulators directly and pin VBAT is powered independently of INH.

TJA1446/66 devices could be used with other supply configurations - for example, a common 5 V supply for pins VBAT and VCC, with INH only controlling the VIO regulator, which is the MCU supply.

Not using the INH pin to control the MCU supply would also be possible. However, since transceiver Sleep mode means RST_N = LOW, it may then become difficult to achieve low system quiescent current with this configuration. Simply not using Sleep mode in the application software would not cover system failures that cause the device to enter Fail-safe, then Sleep mode, independently of the software.

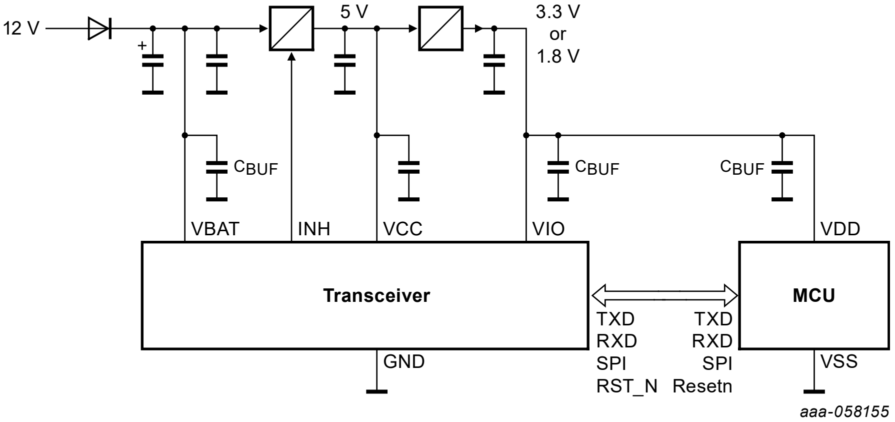


Figure 3. Illustration of a configuration with V_{IO} = 1.8 V or 3.3 V, with unpowered MCU in low-power mode

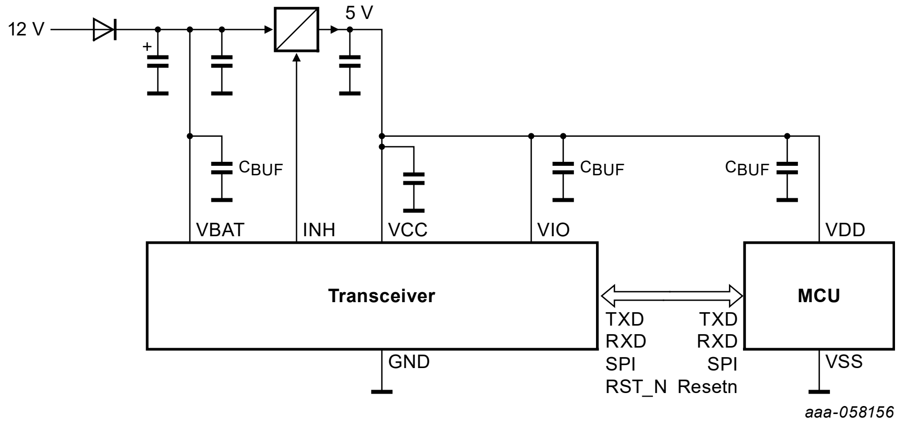


Figure 4. Illustration of a configuration with V_{IO} = 5 V, with an unpowered MCU in low-power mode

2.1.2 Battery reverse-polarity protection, filter and clamping circuitry

The circuitry for rectifying and filtering the car battery supply must ensure that V_{BAT} remains within the boundaries specified in the limiting values section of the data sheet. Any application circuitry that may generate transients on the battery supply, such as electric motors, must be supplied through a separate path without sharing the polarity protection diode connected to the transceiver. As a rule of thumb, the slew rate of the supply voltage on pin VBAT should be limited to less than 10 V/μs for rising edge and less than 1 V/μs for falling edge.

The internal soft clamp on pin VBAT can be turned off to minimize quiescent current while V_{BAT} is between 28 V and 40 V. External circuitry may need to be added to ensure that V_{BAT} does not exceed 40 V.

2.1.3 Capacitors

An external ceramic (i.e. low-ESR) buffer capacitor (C_{BUF}) should be placed close to each supply pin to compensate for supply line inductance. When multiple supply pins are connected to the same power rail, they may share a common capacitor. The nominal capacitance on the VCC pin should be at least 1 μF.

Ceramic capacitors connected to the car battery without current-limiting circuitry should have fail-safe properties (e.g. so-called 'Open-mode' or 'Soft-termination' capacitors). Alternatively, two conventional ceramic capacitors in series can be used, mounted on the PCB at a 90° angle relative to each other. Both options reduce the risk that bending the PCB could damage the capacitor in a way that causes it to conduct a high DC current. For details, contact the capacitor vendor.

2.1.4 Auxiliary circuitry for debugging

When INH is used for direct on/off control of the voltage regulator supplying the MCU, consider adding optional circuitry to allow the regulator to be enabled continuously, regardless of the state of INH. An example is illustrated in Figure 5. Setting the debug jumper may be useful while a debugger or flash tool is connected to the MCU.

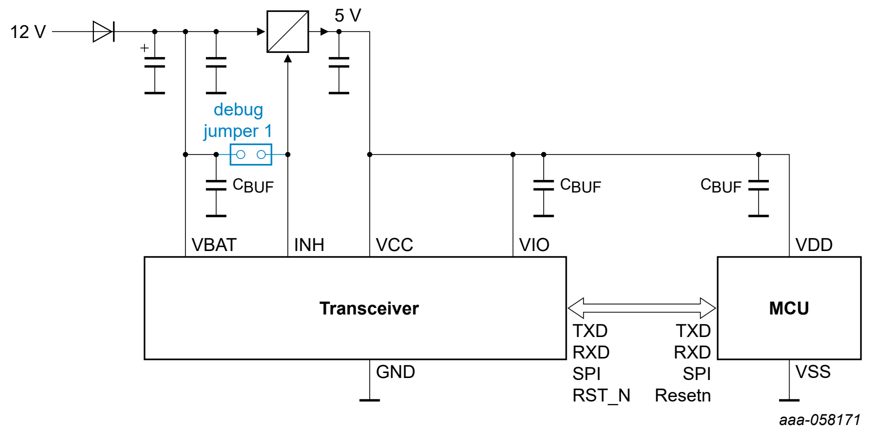


Figure 5. Adding a jumper for optional INH overrule, e.g. during SW development

2.2 MCU/host controller interface

Seven microcontroller port pins are needed to interconnect with the transceiver (4 SPI signals, the CAN TXD/RXD signals and RST_N), of which three (SCK, SDI and SDO) can be shared with other devices.

The V_{DD} supply for the MCU port pins connected to the transceiver must be identical to the transceiver V_{IO} supply.

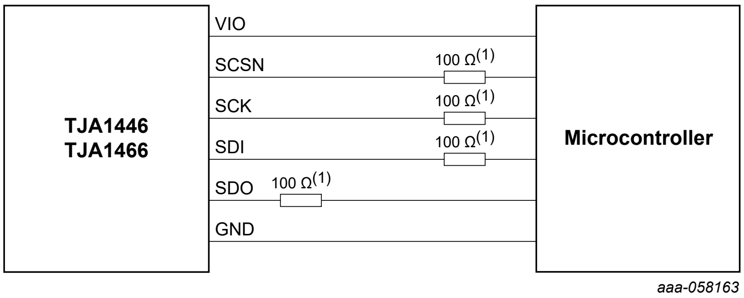
2.2.1 SPI pins SCSN, SCK, SDI, SDO

The SPI interface is the main communication channel between the transceiver and the microcontroller. The microcontroller uses the SPI interface to configure the transceiver and to read back status information. SPI clock speed is up to 4 Mbit/s.

The transceiver is controlled via the 4-wire SPI interface as shown in Figure 8. It consists of four digital pins used for synchronization and data transfer:

- SCSN: SPI chip-select input (active-LOW)
- SCK: SPI clock input
- SDI: SPI data input
- SDO: SPI data output

Pay particular attention to the routing of the clock signal and its ground return path because strong ringing or glitches due to crosstalk from other signals could cause problems. The greater the distance between the host controller and the transceiver, the more likely are the SPI signals to show some ringing during/after each edge. This should be avoided, especially for the SCK signal. Ringing can be reduced by placing series resistors close to the output terminals (see Figure 6). The sum of the resistor value and the source impedance should match the signal impedance on the PCB. A 100 Ω resistor is often appropriate. While higher values would further reduce ringing by slowing the edges, signal speed could be compromised. Note that maximum values are specified for SCK rise and fall times ($t_{r(clk)}$/$t_{f(clk)}$) and a minimum value for the delay time from SCK LOW to SCSN LOW ($t_{d(SCKL-SCSNL)}$).



(1) Optional series resistors to reduce ringing

Figure 6. Typical SPI Interface showing connections between the TJA1446/66 and the microcontroller

When the input function of the microcontroller port pin connected to SDO remains active in a low-power mode, the SDO signal must be pulled HIGH or LOW - using an external resistor or by activating an MCU-internal pull-up or pull-down resistor.

Internal pull-up resistors on pins SDI and SCK are turned on automatically when a HIGH level is applied externally; internal pull-down resistors are turned on when a LOW level is applied. When not driven by an external signal, the pins retain the most recently selected state (HIGH or LOW). To avoid compromising this functionality, external pull-up or pull-down resistors should not be added. While in a low-power mode, the related MCU port pins should remain on or off without pull-up or pull-down currents.

The MCU may share the signals connected to SCK, SDI and SDO with other peripheral devices, but the transceiver needs its own chip-select signal, SCSN (see Figure 7). Daisy-chain connections of SDI and SDO with other devices are not supported.

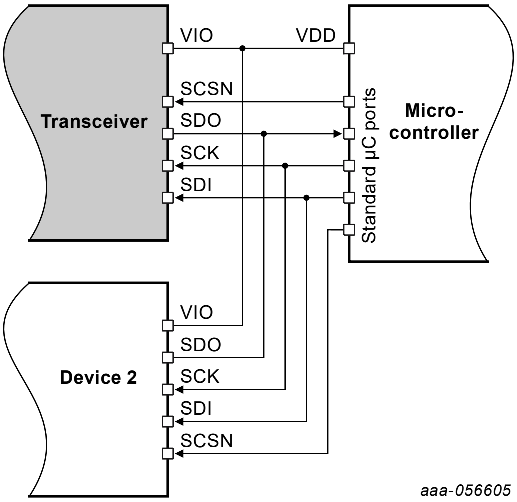


Figure 7. Connecting multiple devices to the same SPI lines

2.2.2 CAN TXD/RXD

The CAN bit stream input (TXD) and output (RXD) pins must be connected to the corresponding MCU port pins. TXD is connected to the MCU port pin with CAN protocol controller bit stream output function 'TXD' (or a similar name). RXD is connected to the MCU port pin with CAN protocol controller bit stream input function 'RXD' (or a similar name).

While series resistors could be added to reduce ringing and emissions on these signals, they could have a negative impact on the loop delay. Refer to the OEM hardware specifications for advice on adding such components.

2.2.2.1 Optional second pair of TXD/RXD pins

When the MCU has more than one CAN protocol controller but the message buffer of a single controller is not big enough for the application, two CAN protocol controllers can be connected to a single transceiver, as illustrated in Figure 8.

- One of the CAN controllers is mapped to the MCU TXD/RXD port pins connected to TXD/RXD on the transceiver
- The other CAN controller is mapped to the MCU TXD/RXD pins connected to GPIO2 (with TXD2 function selected) and GPIO1 (with RXD2 function selected)

The corresponding GPIO1/2 pin configuration is explained in Section 3.5.4.

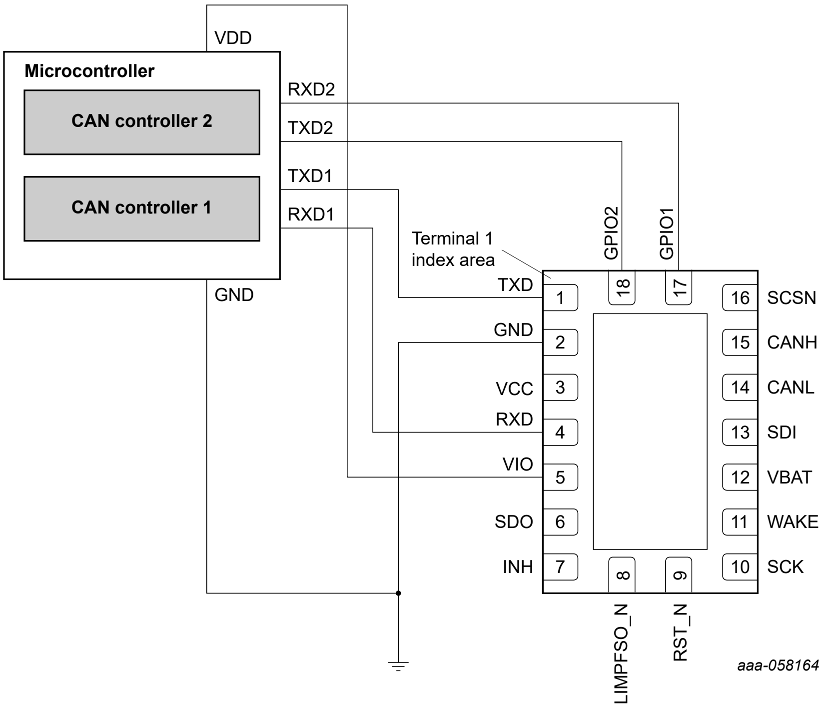


Figure 8. Connecting two CAN controllers of the MCU to the same TJA1446/66 transceiver

2.2.3 GPIO pins

The TJA1446/66 contains two GPIO pins that can be used by the microcontroller as extra SPI-controlled remote digital I/O port pins.

They can be used to help minimize the bottom-line MCU port pin ‘consumption’ by the transceiver. When needed, a signal connected to a GPIO pin may be used to wake up the MCU from a low-power state (see Section 3.5.4). However, GPIO pin functionality is only available when the transceiver is in Normal, Standby, Sleep or ListenOnly mode and V_{IO} is present.

When a GPIO pin is not used, it can be left unconnected thanks to its internal repeater function (automatic pull-up/down resistor).

See also Section 2.2.2.1 on using GPIO pins as a second TXD/RXD signal pair.

2.2.4 RST_N

The bidirectional, active-LOW RST_N pin is used to trigger a system reset. It should be connected to the reset input pin on the connected MCU.

- The device forces pin RST_N LOW for $t_{d(rst)}$ to reset the MCU in response to a transceiver reset event. An internal pull-up allows the signal to return HIGH after the reset event has been processed. After the device has finished driving RST_N LOW, it expects a HIGH level within the reset release time $t_{rel(rst)}$. An external pull-up resistor to VIO may be added, if needed - e.g. to compensate for any capacitance to ground. The external pull-up current must be lower than the specified maximum (18 mA, see the limiting values section in the data sheet), and it should not exceed 10 mA to ensure that the RST_N pin is able to drive a LOW level of less than 25 % V_{IO} (see parameter V_{OL} for this pin). Such a level is certain to be recognized as LOW by the transceiver (max V_{IL}= 30% V_{IO}) but should be confirmed for the MCU (see input specification of the MCU Reset pin).
- In turn, if the MCU or other devices pull RST_N LOW for longer than the reset filter time $t_{fltr(rst)}$, the input function on the RST_N pin recognizes this and triggers a reset event in the transceiver. However, if RST_N is held LOW for longer than the sum of the reset filter, reset delay and reset release times ($t_{fltr(rst)} + t_{d(rst)} + t_{rel(rst)}$), the transceiver will immediately enter Fail-safe mode.
- The device drives RST_N continuously LOW when not in Standby, Normal or ListenOnly mode. Note that RST_N is LOW in Sleep mode.

When an MCU debugger is connected to the MCU during software development, it may also drive the Reset input signal on the MCU. To avoid conflicts with the RST_N input/output function on the transceiver, an optional circuit to disconnect the reset signal may be added, as illustrated in Figure 9. For software development, the 0 Ω bridge R1 would be removed, allowing the reset signal to be temporarily connected or disconnected with debug jumper 2.

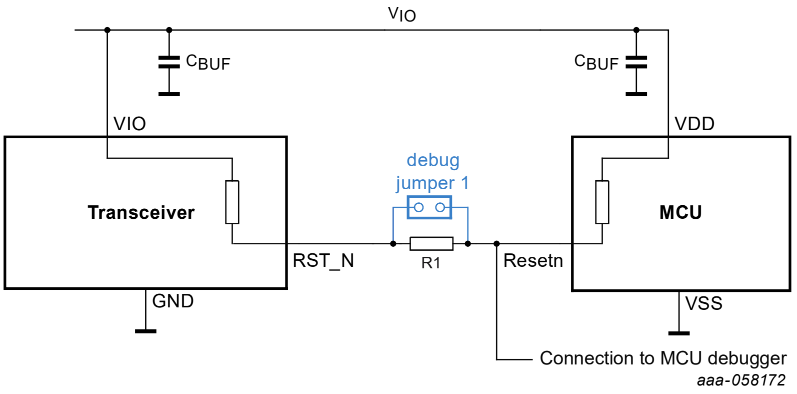


Figure 9. Optional RST_N disconnection from MCU during debugging

An alternative approach is illustrated in Figure 10. When needed for debugging, jumper 2 can be used to isolate the RST_N signal. R1 then acts as an additional pull-up to RST_N and R2 as an additional pull-up for to the MCU/debugger reset signal. The resistor values need to be:

- on the one hand, low enough to ensure RST_N is still able to drive a LOW signal on the MCU's Reset pin when the jumper is not set (consider the voltage divider created by R1 and R2 with the MCU internal pull-up resistor R_{pu}) but
- on the other hand, R1 must be high enough not to overload RST_N (max 10 mA) and R2 high enough not to overload the debugger when these devices drive a LOW level while the jumper is set.

For example, first select R1 = 1 kΩ for V_{IO} = 1.8 V, 2 kΩ for V_{IO} = 3.3 V or 5 V. This limits the current to much less than 10 mA while the jumper is set. The maximum allowed value for R2 can then be calculated from the voltage divider requirements when the jumper is not set:

$V_{OL(RST\_N)max} + (V_{IO} - V_{OL(RST\_N)max}) \times (R1 + R2) / (R1 + R2 + R_{pu}) < V_{IL(MCU)}$

with $V_{IL(MCU)}$ representing the maximum LOW level of the MCU's reset input pin and R_{pu} being its internal pull-up resistor.

$V_{OL(RST\_N)max}$ is 0.4 V when the load current does not exceed 1 mA, which is true for $(R1 + R2 + R_{pu}) >$ VIO / 1 mA when the jumper is not set. Assuming the minimum MCU internal pull-up resistance R_{pu} = 20 kΩ, this requirement is met independently of the selection of R1 and R2.

Selecting R2 = 2 kΩ would work for the debugger when it can drive at least 2.5 mA for a LOW level with V_{IO} = 5 V or 1.7 mA with V_{IO} = 3.3 V, which should be a realistic assumption. For V_{IO} = 1.8 V, we would select R2 = 1 kΩ and assume a 1.8 mA drive strength. Now, we can calculate the left side of the above equation for the individual V_{IO} cases:

V_{IO} = 1.8 V: 0.4 V + 1.4 V x (1 + 1) / (1 + 1 + 20) = 0.53 V = 30 % V_{IO}

V_{IO} = 3.3 V: 0.4 V + 2.9 V x (2 + 2) / (2 + 2 + 20) = 0.9 V = 27 % V_{IO}

V_{IO} = 5 V: 0.4 V + 4.6 V x (2 + 2) / (2 + 2 + 20) = 1.2 V = 24 % V_{IO}

All three cases would fit with a maximum MCU pin LOW input level $V_{IL(MCU)}$ of 30 % V_{IO}.

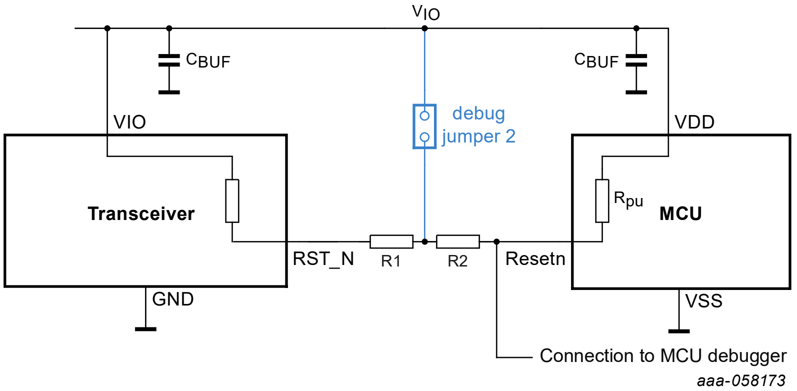


Figure 10. Optional RST_N isolation from MCU during debugging

2.3 CAN bus connection to CANH, CANL

2.3.1 CAN bus termination

In general, the termination circuitry on the CAN bus should be designed according to the car manufacturer's specifications. If this is not applicable, refer to NXP application hints document 'Rules and Recommendations for In-vehicle CAN Networks' [3].

2.3.2 CAN ESD protection

Although the CANH/CANL bus pins are equipped with internal ESD protection, adding external clamping components can be considered, e.g. PESD2CANFD24V-T or PESD2CANFD24L-T.

2.4 WAKE pin interface

In general, on-board circuitry must ensure that the WAKE pin is operated within the boundaries specified in the Limiting values section of the data sheet. The example circuits in this section may need to be adapted to the specific conditions of the application.

2.4.1 WAKE pin connected to the INH pin on another transceiver

An example circuit showing the INH pin on one transceiver being used as a wake-up source for another transceiver is illustrated in Figure 11. With the INH pin on transceiver 1 turned off in Sleep mode, resistor R pulls the WAKE pin on transceiver 2 LOW. When Transceiver 1 wakes up from Sleep mode, the INH output turns on automatically, creating a rising edge on the WAKE input on transceiver 2. The value of resistor R must be high enough to ensure that the INH output is not overloaded and low enough to achieve a LOW level while the internal pull-up on the WAKE pin is active. In this example, transceiver 2 would be a TJA1446 or TJA1466, but transceiver 1 would be a different device.

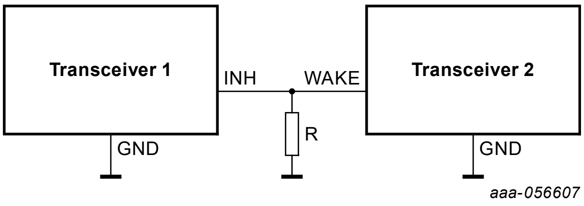


Figure 11. Using transceiver 1 as wake-up trigger for transceiver 2

2.4.2 WAKE pin connected to external switch to ground

In the example circuit in Figure 12, a switch or button with a ground connection serves as the wake source. Resistor R1 determines the WAKE signal level while the contact is open. R2 is needed to protect the WAKE pin against ESD events applied to the switch cable. The minimum value of R2 (3 kΩ) can be derived from the ESD test conditions specified in the Limiting values section of the data sheet. Note that the R2 package must be large enough to prevent arcing over its terminals during an ESD event.

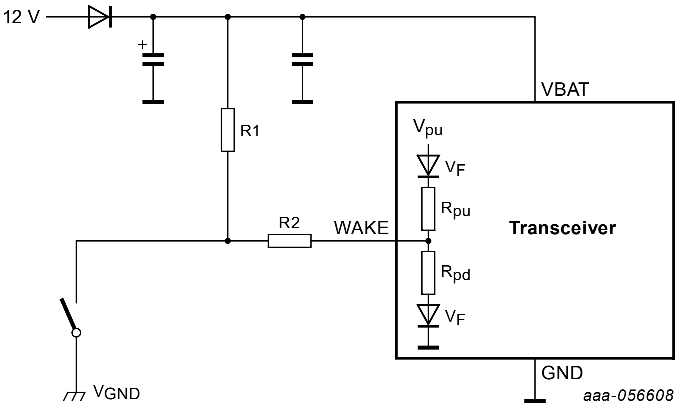


Figure 12. Illustration of circuitry between the WAKE pin and a switch to ground

The value of R1 determines the current running through the closed contact of the switch.

The sum of R1 and R2 must be low enough to maintain a HIGH level on the WAKE pin while it is being pulled down internally via R_{pd}:

$V_{th(wake)} < V_F + (V_{BAT} - V_F) \times R_{pd} / (R_{pd} + R2 + R1)$

$V_{th(wake)}$ x (R_{pd} + R2 + R1) < V_F x (R_{pd} + R2 + R1) + (V_{BAT} - V_F) x R_{pd}

($V_{th(wake)}$ - V_F) x (R_{pd} + R2 + R1) < (V_{BAT} - V_F) x R_{pd}

R_{pd} + R2 + R1 < ((V_{BAT} - V_F) / ($V_{th(wake)}$ - V_F)) x R_{pd}

R1 + R2 < R_{pd} x ((V_{BAT} - V_F) / ($V_{th(wake)}$ - V_F) - 1)

Obviously, the requirement for the sum of R1 and R2 depends on the supply voltage connected to R1 (here V_{BAT}), and this voltage must be higher than the threshold voltage $V_{th(wake)}$ at the WAKE pin. For example, for the circuitry to work correctly when V_{BAT} = 4.25 V or higher and $V_{th(wake)max}$ = 2.6 V, V_F = 0.3 V and $R_{pd(min)}$ = 100 kΩ, the requirement would be:

R1 + R2 < 100 kΩ x ((4.25 - 0.3) / (2.6 - 0.3) - 1) = 100 kΩ x (3.95/2.3 -1) = 71 kΩ

R2 must be low enough to guarantee a LOW level on the WAKE pin while it is being pulled up internally via R_{pu}, considering there may be an offset V_{GND} between switch ground and module ground.

$V_{th(wake)}$ > V_{GND} + R2 / (R2 + R_{pu}) x (V_{pu} - V_F - V_{GND})

R2 / (R2 + R_{pu}) < ($V_{th(wake)}$ - V_{GND}) / (V_{pu} - V_F - V_{GND})

With **V_R = ($V_{th(wake)}$ - V_{GND}) / (V_{pu} - V_F - V_{GND})**:

R2 / (R2 + R_{pu}) < V_R

R2 < R2 x V_R + R_{pu} x V_R

R2 x (1 - V_R) < R_{pu} x V_R

R2 < R_{pu} x V_R / (1 - V_R)

With $V_{th(wake)}$ = 1.8 V, V_{GND} = 1 V, V_{pu} = 5.5 V, V_F = 0.3 V and R_{pu} = 100 kΩ, R2 is calculated as:

R2 < 23.5 kΩ

For example, the above requirements can be met with R2 = 10 kΩ for ESD protection and R1 = 1.2 kΩ for 10 mA contact current at 12 V.

2.4.3 WAKE pin connected to ignition

Figure 13 illustrates an interconnection between the WAKE pin and the ignition line (aka ‘terminal 15’) of the car. R2 ensures that a LOW level is detected when the switch is open. R2 can be calculated as described in Section 2.4.2, with V_{GND} = 0 V. With $V_{th(wake)}$ = 1.8 V, V_{GND} = 0 V, V_{pu} = 5.2 V, V_F = 0.3 V and R_{pu} = 100 kΩ:

R2 < 58 kΩ → select 51 kΩ.

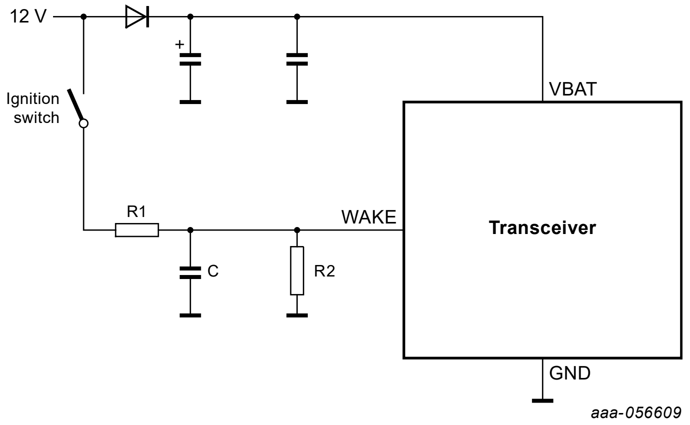


Figure 13. Illustration of circuitry between the WAKE pin and the ignition signal

The combination of R1 and C acts as a low-pass filter to suppress transients on the battery line. The selected capacitance should be large enough to keep the WAKE pin voltage within specified limits while storing the charge of an ESD event. For example, when a 150 pF capacitor with 8 kV discharges into a previously empty 47 nF capacitor, the resulting voltage would be 39.4 V on both capacitors. For an additional safety margin and to compensate for tolerances, a nominal 100 nF capacitor may be selected for C in this example.

When the switch is closed, the value of R1 should be calculated to guarantee a HIGH level on the WAKE pin while it being pulled down internally via R_{pd} and externally via R2.

The formula used in Section 2.4.2 to calculate R1 + R2 can be reused to calculate R1. When using the same parameters for V_{BAT} and $V_{th(wake)}$ (V_{BAT} = 4 V or higher and $V_{th(wake)}$ = 2.6 V) but with R_{pd} = 34 kΩ (internal 100 kΩ resistor R_{pd} in parallel with external 51 kΩ resistor R2) and V_F = 0 V (which simplifies the calculation and creates an additional safety margin), the requirement would be:

R1 < 34 kΩ x (4 / 2.6 - 1) = 18.3 kΩ → select 18 kΩ.

The resulting RC filter time constant would be 18 kΩ x 100 nF = 1.8 ms. When a longer filter time is needed, increase the capacitance, because the resistance should not exceed the calculated value.

2.5 LIMPFSO_N

The LIMPFSO_N pin can be used in one of two ways: as a fail-safe output or a limp-home output signal, configured via bit LIMPFSOC in the Fail-safe output control register. These functions are described in subsections Section 2.5.1 and Section 2.5.2 and summarized in Table 3.

Table 3. LIMPFSO_N usage examples

Usage type	Required input signal property of connected HW	Default status of connected HW at power up (before initialization)	LIMPFSOC initialization (no failure)	Status of connected HW after initialization (no failure)	Status of connected HW with and after entering Fail-safe mode
activation of limp-home HW under failure condition	pull-up[1]; LOW level activates hardware	off	00	off	on
enabling of safety-relevant hardware while system integrity is confirmed	pull-down[2]; HIGH level enables hardware	disabled	10 (or 11)	enabled	disabled

[1] See limiting values section of the data sheet for max voltage (40 V) and max current (2 mA).

[2] See data sheet parameter ΔV_H for the LIMPFSO_N pin: connected HW must recognize a HIGH level when $V_{LIMPFSO\_N} \geq V_{IO} - 0.4$ V (for nominal V_{IO} = 1.8 V), or $V_{IO} - 1$ V (for nominal V_{IO} = 3.3 V or 5 V).

2.5.1 Limp-home application example

A limp-home output signal (LIMPFSO_N forced LOW) activates back-up hardware in the event of a main system failure. It is active-LOW by default. For reverse polarity, a signal inverter would need to be connected.

Since the pin is inactive at power up (hi-Z), it must be pulled HIGH by the hardware it is connected to. When the transceiver enters Fail-safe mode, the LIMPFSO_N pin is automatically driven LOW.

The pin can be pulled to V_{IO} or higher, limited by the maximum ratings (see parameters V_x and $I_{O(LIMPFSO\_N)}$ in the Limiting values section of the data sheet). Internal protection circuitry ensures that a level higher than V_{IO} would not cause an internal cross-current to flow from pin LIMPFSO_N to pin V_{IO} if the LIMPFSOC bits were accidentally set to 10 (or 11).

2.5.2 Fail-safe output application example

The fail-safe output signal keeps connected fail-silent hardware deactivated until proper system operation has been confirmed. It also deactivates it automatically in response to a system failure. The fail-silent hardware is disabled by default (LIMPFSO_N LOW). A HIGH level on LIMPFSO_N enables the fail-safe hardware. For reverse polarity, a signal inverter would need to be connected.

Since the pin is inactive at power up (hi-Z), it must be pulled LOW by the hardware it is connected to. Once the application software has started up and all self-tests have been completed successfully, the connected hardware can be enabled by setting the LIMPFSOC bits to 10 (or 11). This allows the device to drive LIMPFSO_N HIGH (V_{IO}). When the transceiver enters Fail-safe mode, the LIMPFSO_N pin drives the signal LOW, disabling that hardware again.

When LIMPFSOC = 10 or 01, the pin drives a V_{IO}-based HIGH level as specified by data sheet parameter ΔV_H (HIGH-level voltage drop). The higher max value for variants B/C (compared with variant A) represents an additional internal voltage drop caused by the internal protection circuitry mentioned in Section 2.5.1. Note that the observed output signal may vary within the range $V_{IO} - \Delta V_H$ to V_{IO} when the temperature or V_{BAT} is changing.

3 Application software

This section proposes ways a microcontroller (MCU) can use application software to control the transceiver via the SPI. It assumes that the interconnections between the transceiver and the MCU are available, as discussed in Section 2.2. For aspects related to functional safety, see the related safety manual [4].

3.1 SPI status check

SPI communication issues can be detected by comparing the first two return bytes of an SPI transfer with the corresponding bytes sent to the transceiver. When a mismatch is found, the SPI transfer should be regarded as void. This check should always be performed when attempting to read data from the device registers to detect invalid received data (see also Section 3.4).

3.2 Addressing multiple registers at once via SPI

The transceiver accepts SPI messages with up to four bytes of data for read and/or write access. In this way, up to four registers with incremental addresses can be accessed with a single SPI message. The address carried by the SPI frame points to the register with the first (lowest) address (see example in Section 3.5.4, Table 5 describing writing to addresses 0x042 and 0x043). The register map is optimized to use this feature effectively, with functionalities such as PN configuration, status information or configuration bits grouped accordingly. Refer to the data sheet for further details on the SPI protocol and register map.

3.3 Parity bit

The parity bit, PAR, is calculated in the user application. The first 16 SPI bits must contain an even number of '1' bits - so if the first 15 bits contain an odd number of 1's, the parity bit (bit 16) must be set to 1 (otherwise it is set to 0).

3.4 Read-back of written data

Bit failures on the SDI signal occurring during transmission of one or more data bytes of an SPI frame will not be detected by the device. To be on the safe side, writing to registers should consist of:

- an initial SPI frame writing to a register(s)

- a second SPI frame reading the register contents (same address but with read-only bit set)
- a comparison between transmitted (1st frame) and read data (2nd frame)

When a match is confirmed and the SPI status check (see Section 3.1) is ok, the write attempt can be regarded as successful. Otherwise, the write and check should be repeated. An escape mechanism should be implemented to prevent it being stuck in an endless loop.

Checking for a match between read and written data does not apply to Interrupt status registers, to the System reset register, to the Watchdog answer register or to read-only bits in registers. When an attempt to set the WDD and/or the WDOFF bit to '1' in the Watchdog configuration register fails, this does not necessarily mean that the SPI transfer has failed. These bits can be set to '1' only when the device is in an appropriate state, as described in the data sheet.

Note that the SPI supports full-duplex communication, but an SPI frame writing new data to a register returns the data the register had before the new data arrived.

3.5 Device initialization

3.5.1 Power supply configuration

When pin VBAT is supplied with the same 5 V voltage as pin VCC, or with any other regulated voltage < 5.5 V, bit VBATVCC in the system configuration register must be set to 1 and V_{CC} must remain powered in low-power modes.

When V_{CC} is turned off in Sleep mode, VBATVCC must be cleared to 0 and V_{BAT} must be powered with 12 V (see Figure 3 and Figure 4) or with a regulated voltage > 5.5 V. See Table 4 for an overview of the available options.

Table 4. VBATVCC settings in Sleep mode

V_{CC} in Sleep mode	$V_{BAT} = V_{CC}$[1]	V_{BAT} = 12 V (or regulated voltage > 5.5 V)[1]
V_{CC} on	VBATVCC = 1	VBATVCC = 0
V_{CC} off	not allowed	VBATVCC = 0

[1] V_{BAT} must be powered in Sleep mode.

When an external clamping circuit is used on V_{BAT} (see Section 2.1.2), bit BCCTRL in the system configuration register may be set to 1 (internal clamp off) to reduce the internal quiescent current while V_{BAT} is above 28 V. Otherwise, BCCTRL must be cleared to 0 (internal clamp enabled).

The other bits in the system configuration register, RXDINTC (see Section 3.5.5) and SLEEPDIS (see Section 3.5.7), should be configured as required by the application.

3.5.2 CAN transceiver configuration

The default value of 0x00 for the CAN configuration register should be sufficient for sending and receiving CAN bus messages. Bit CWC may need to be adjusted for wake-up pattern optimization per OEM requirements.

GPIO configuration for optional TXD2/RXD2 is discussed in Section 3.5.4.

3.5.3 Wake-up source configuration

Local (pin WAKE) and remote (CAN) wake-up can be enabled/disabled via interrupt enable bits WPRE/WPFE and CWE in the System interrupt enable register. This can be done during initialization or, at the latest, before the ECU enters a low-power mode. Note that these bits may have been set automatically by the device during earlier failure handling (VIO undervoltage or MCU reaction timeout).

When the transceiver switches off power to the MCU in Sleep mode via the INH pin (see Figure 3 and Figure 4), consider keeping ‘regular’ wake-up sources (CAN and WAKE pin) disabled until just before issuing a Sleep command. This ensures that any accidental Sleep command (e.g. due to noisy SPI) would only trigger an SPI fail interrupt (if enabled) and not an unintended transition to Sleep mode.

When partial networking (PN) wake-up is employed, it must be configured via the PN ID, PN ID mask, PN frame control and PN data rate and filter configuration registers. When the data length code (DLC) and data field are included in the wake-up frame (PNDM = 1), the DLC and the PN data mask registers need to be initialized as well. PN configuration is completed by writing CPNC = 1 and PNCOK = 1 to the PN CAN configuration register. With the same SPI command, the desired behavior for CAN FD frames or CAN XL frames should be selected via bits PNECC and CXLDE (if applicable to the device variant). A detailed explanation of the PN settings is provided in the appendix, Section 4.1. SPI commands for an example PN configuration with transition to Sleep mode are described in the appendix, Section 4.2.

Bit WFC in the wake-up pulse configuration register can be used to select one of two filter times (short or long) for the WAKE pin.

3.5.4 GPIO pin configuration

When GPIO pins are used, their functionality needs to be initialized via bits GPIOxC and GPIOxFS in the GPIOx configuration registers (x = 1, 2). The digital input function is always available, independent of the function selected via GPIOxFS. For example, select GPIOxFS = 0x02 to use the pin as a general-purpose, bi-directional remote I/O port (see also Section 2.2.3).

For pins with an output function other than RXD2, the polarity needs to be defined via bits GPPx in the GPIO polarity configuration register. These bits may also be used to initialize the default level on GPIO pins used as digital outputs (see also Section 3.6.3).

When a GPIOx pin is to be used as a wake-up interrupt source, it must be configured with GPIOxFS = 0x13, 0x14 or 0x15 (wake-up detection input with rising, falling or dual-edge sensitivity) and with GPIOxE = 1 (interrupt enabled). The configuration combination GPIOxFS = 0x01 (‘digital input only’) with GPIOxE = 1 will not configure the pin for wake-up detection.

Using GPIO1/2 as a second pair of TXD/RXD pins to connect with a second CAN controller is discussed in Section 2.2.2.1. The construction of a single SPI frame to configure the GPIO pins for this purpose is illustrated in Table 5.

Table 5. Initialization of GPIO1/2 as RXD2/TXD2, using a single SPI frame

SPI header					**GPIO1 config register (address 0x042)**			**GPIO2 config register (address 0x043)**		
ADDRESS		RO	PLS	PAR	DATA0			DATA1		
address of GPIO1 config reg		not read-only	2 data bytes	parity	GPIO1C	GPIO1FS		GPIO2C	GPIO2FS	
					output: push-pull	RXD2 (and RXD)		input pull-up	TXD2 (and TXD)	
0x42		0	01	1	000	0x06		001	0x05	
0x04	0x02	0	01	1	000	0	0110	001	0	0101
Byte 1	**Byte 2**				**Byte 3**			**Byte 4**		
0x04	**0x23**				**0x06**			**0x25**		

3.5.5 Configuring interrupts

Transient events on internal or external signals may be interpreted as interrupts when related interrupts have been enabled. Some of these interrupts can be used as wake-up sources (see Section 3.5.3).

When an interrupt is generated by the transceiver in Standby or Sleep mode, it is signaled to the MCU via a LOW level on pin RXD while V_{IO} is available. It is possible to select which interrupts are signaled on RXD via the RXDINTC bit in the system configuration register. When RXDINTC = 0 (default value), only wake-up and power-on interrupts are signaled on RXD. When RXDINTC = 1, any enabled interrupt will be signaled on RXD and will wake the MCU from its low-power mode (applicable when the MCU remains powered, see Section 3.7.2).

Transceiver interrupts may already be pending after an MCU reset, even before they have been enabled during the initialization process. For example, the non-maskable PO interrupt is always generated during power on. An MCU reset due to wake-up from Sleep mode would be accompanied by a pending wake-up interrupt of the transceiver. See also Section 3.6.2.

Note that the device may already be in Normal mode if it was powered up with a steadily dominant CAN bus. See also Section 4.3.1.

3.5.6 Watchdog configuration and initialization

There is no need to initialize the watchdog fail counter WDFC. After any reset, it starts automatically with value 2, which means that the next invalid watchdog trigger will cause the MCU to be reset. To prevent the next watchdog timer overflow generating a reset (due to a missing watchdog trigger), write a value less than 2 to the the watchdog fail counter.

During configuration, select the desired watchdog period (WDP) via the Watchdog configuration register before the device enters Normal (or ListenOnly) mode.

The watchdog can be disabled in Standby mode by setting WDOFF = 1. All pending interrupts, e.g. the PO interrupt, must be cleared before disabling the watchdog. Note that the watchdog runs in Normal mode independently of WDOFF. WDOFF is cleared automatically by any interrupt or watchdog service (i.e. by writing to bits WDA in the Watchdog answer register).

The 'Start-to-Normal' SNM boot sequence (see Section 4.3) puts the device into Software Development mode (bit SDM = 1; watchdog disabled). However, any watchdog service (valid or invalid watchdog trigger) would clear SDM automatically. Watchdog debugging can be enabled while SDM = 1 by setting bit WDD = 1 before the first write access to the watchdog answer (WDA) register. The watchdog will remain off while WDD = 1; an incorrect serving of the watchdog will not trigger the reset process. Note that the device will ignore any attempt to set WDD = 1 in the absence of a 'Start-to-Normal' startup.

3.5.7 Initialization of fail-safe behavior

After each system reset, the fail-safe counter FSCC must be initialized to 0 to prevent the next fail-safe-relevant reset event (see Table 6) causing the device to enter Fail-safe mode.

Table 6. Fail-safe relevance of reset events

Reset event	Fail-safe relevant
Power on	no
Wake-up from Sleep mode	no
SPI system reset	no
RST_N pulled LOW externally	yes
Reset with RST_N clamped HIGH externally	yes

Table 6. Fail-safe relevance of reset events*...continued*

Reset event	Fail-safe relevant
V_{IO} undervoltage/overvoltage	yes
Watchdog failure while WDD = 0 and WDFC = 2 or 3	yes

When FSCC is initialized to 1, the next fail-safe-relevant reset event will cause the device to enter Fail-safe mode. Initialization to 2 or 3 may have the same effect but should be avoided.

When not initialized, the value of FSCC depends on the device operating history. FSCC may still have its power-on value 0, or it may have been incremented to 1 by a previous event.

When the LIMPFSO_N pin is used, it needs to be initialized according to its purpose (see Table 3). Before doing so, all available system self-tests should have been run successfully. When a self-test fails, the LIMPFSOC bits may be set to 01 to, respectively, activate the limp-home hardware or disable the fail-silent hardware.

If SLEEPDIS = 0 in the System configuration register (the default value), the device will enter Sleep mode after entering Fail-safe mode. If this transition is not wanted, SLEEPDIS should be set to 1.

The success or failure of a previous attempt to set the WDD bit can be checked by reading the Watchdog configuration register (see Section 3.5.6). If WDD = 1, the device started up in software development mode and it may be useful to disable Sleep mode by setting SLEEPDIS = 1. See also section Section 4.3.

Note that it will still be possible to enter Sleep mode by clearing bit SLEEPDIS before issuing a Sleep command (see Section 3.7.1).

3.5.8 Watchdog synchronization

Confirm that the device is still in Standby mode and generate a valid watchdog trigger immediately before setting the device to Normal mode. This trigger marks the start of the watchdog period to which the MCU's software timing for watchdog service should be synchronized. Note that such synchronization is easier to perform in Standby mode than in Normal mode. The watchdog is in Timeout mode in Standby mode, which means that there is no risk of a 'too early' watchdog trigger.

This step may be skipped when the device is in Software Development mode (SDM = 1), see Section 3.6.1 and Section 4.3.3.

3.5.9 Transition to Normal mode

The CAN transceiver is only enabled for full operation after the device has entered Normal mode. Provided V_{CC} is present, this will happen $t_{t(moch)}$ after issuing the Normal mode command (write 0x0F to the Mode control register).

3.6 Normal operation

3.6.1 Watchdog service

Consider servicing the watchdog only when bit SDM = 0 (watchdog active). The watchdog is disabled when the device powers up with the bus dominant ('Start-to-Normal'; SDM = 1). See also Section 3.5.7 and Section 4.3.

When the watchdog period needs to be reduced, a valid watchdog trigger should be generated before changing WDP. This re-starts the watchdog timer. Set the device to Standby mode before changing WDP to avoid 'too early' trigger errors (see also Section 3.7).

Note that clearing WDFC to 0 has a similar effect to a valid watchdog trigger - it prevents the watchdog generating resets. When this is repeated periodically at an interval of less than two watchdog periods, the absense of watchdog triggers will not generate resets.

3.6.2 Interrupt handling

While the device is in Normal mode, enabled interrupts are still generated but they are not signaled on pin RXD. The MCU may check periodically for pending interrupts by reading the interrupt status registers. This can be done most efficiently with a single 6-byte SPI read access to address 0x060 (the system interrupt status register). If any of the returned data bytes is not 0x00, there is a pending interrupt.

Once processed, single or multiple interrupts can be cleared, individually or all at once, by writing 1 to the associated bits in the interrupt status registers.

3.6.3 Using GPIO pins as remote digital I/O port pins

The output level on a GPIO pin configured as a 'digital output' (GPIOxFS = 0x02) is controlled via the GPPx bits in the GPIO polarity configuration register. Since this register covers both GPIO pins, changing the output level of one pin means that the existing polarity configuration of the other pin needs to be repeated.

The HIGH/LOW status of a GPIO output or input signal can be sampled by reading the GPIO status register. When a GPIO pin was configured as a wake-up input with enabled interrupt (see Section 3.5.4), the occurrence of edges that have passed the input filter with the selected polarity will be visible in the GPIO interrupt status register.

3.7 Transition to low-power mode

If not yet done, the required wake sources must be enabled before the ECU enters a low-power mode (see Section 3.5.3), and all pending interrupts should be processed and cleared (see Section 3.6.2). Note that the transceiver will not enter Sleep mode unless at least one of the main wake-up sources (CAN bus, WAKE pin) is enabled, all wake-up interrupts are cleared and SLEEPDIS = 0. Entering Standby mode is always possible, even without any wake source being enabled.

Before leaving transceiver Normal mode, consider waiting until ongoing CAN bus message transmission or reception has been completed.

3.7.1 Sleep mode (MCU not powered in low-power mode)

If SLEEPDIS was set to 1 during initialization (Section 3.5.1, Section 3.5.7), it needs to be cleared to 0 before initiating a transition to Sleep mode.

After transmitting the SPI Sleep mode command (write 0x01 to the Mode control register), wait long enough for the transceiver to process this request and to drive RST_N LOW. During this time, the device can be checked for coincidental wake-up or for other reasons that may cause the Sleep mode command to be canceled. Allow $t_{t(moch)}$ after issuing the SPI sleep command for the transceiver to enter Sleep mode.

See Appendix Section 4.2 for an example SPI command sequence for PN configuration with transition to Sleep mode.

3.7.2 Standby mode (MCU remains powered in low-power mode)

When the MCU remains powered in low-power mode, the RXD signal is used to wake the MCU from its low-power mode (‘MCU stopped’). In transceiver Standby mode (write 0x06 to the Mode control register), RXD is LOW continuously while interrupts are pending (as selected via bit RXDINTC, see also Section 3.5.5).

When the related MCU pin interrupt is edge-sensitive, the readiness of the transceiver to generate a wake-up edge on RXD must be confirmed before stopping the MCU: the RXD signal must be HIGH. If it is LOW, there are pending interrupts that need to be cleared (see Section 3.6.2) before the MCU is stopped.

Even if bit WDOFF in the watchdog configuration register was set successfully earlier, e.g. during device initialization, this should now be repeated because WDOFF may have been cleared in the meantime, e.g. by interrupts.

Setting WDOFF will only stop the watchdog if all interrupts have been cleared. When writing to this register, a long enough watchdog period should be selected for the upcoming wake-up event, which will automatically restart the watchdog with that period. Consider the time that the MCU will need between wake-up and first watchdog service.

3.8 Wake-up

After the MCU wakes up from low-power mode (Section 3.7.2), or after an MCU reset caused by a wake-up from Sleep mode (Section 3.7.1), a full re-initialization of the transceiver (Section 3.5) may not be necessary but is recommended to be on the safe side. In any case, a watchdog (re-)initialization/synchronization (Section 3.5.7) and a transition to Normal mode (Section 3.5.9) will need to be executed before normal operation can be resumed.

4 Appendix

4.1 Partial networking configuration

Since the proper configuration of the partial networking registers is critical for successful wake-up from low-power mode, the integrity of any write access to these registers should be checked as described in Section 3.1 and Section 3.4.

4.1.1 Concept of selective wake-up

Partial networking is the concept of splitting the network into subnetworks that can be woken-up separately by dedicated wake-up frames (WUFs). Such subnetworks can contain any number of nodes - even a single node or all the nodes on the network. A node may belong to more than one subnetwork. The network owner needs to define how this selective wake-up of the subnetworks by WUFs is handled.

A WUF is a standard CAN frame according to ISO11898-1 and therefore consists of the CAN identifier (ID, Standard or Extended Frame Format), the data length code (DLC) and the data field of a CAN frame. Three options are available for defining which of these elements is to be used to control the wake-up of subnetworks:

- Only the ID
- ID and DLC with DLC = 0
- ID, DLC with DLC > 0 and data field

Note that a WUF frame with CAN FD or CAN XL frame format is not supported, even when PNDM = 0.

4.1.2 ID and ID mask

The CAN frame identifier (ID) that will be accepted as a valid WUF ID is defined in the partial networking ID registers.

As illustrated in Figure 14, an 11-bit ID can be loaded into ID registers 3 and 2 after shifting the ID to the left by two bit positions, which is equivalent to multiplying it by 4. A 29-bit identifier can be loaded directly into ID registers 3 to 0 (see Figure 15).

For 11-bit IDs, the values stored in ID registers 1 and 0 are not used and are 'don’t care'.

If only one CAN ID is used for wake-up, then all partial networking ID mask registers should be set to 0x00 (default value). As specified by ISO11898-2, multiple WUF IDs can be configured by defining individual ID bits as 'don’t care', which is represented by an ‘x’ in the WUF ID examples in Figure 14 and Figure 15. A '1' needs to be set at the corresponding bit positions in the ID mask. The ID mask can also be calculated as follows:

1. Determine the highest ID by setting all 'don’t care' bits to ‘1’
2. Determine the lowest ID by setting all 'don’t care' bits to ‘0’
3. The difference, highest ID minus lowest ID, represents the ID mask value

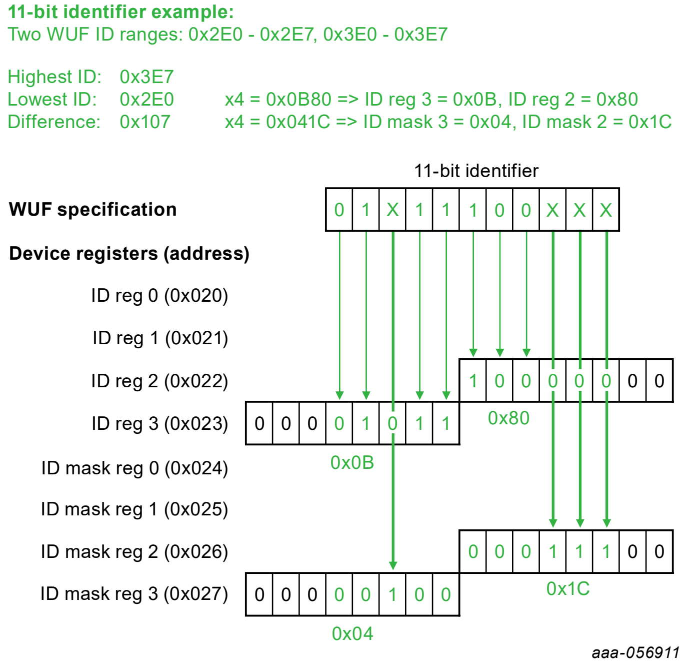


Figure 14. 11-bit ID configuration

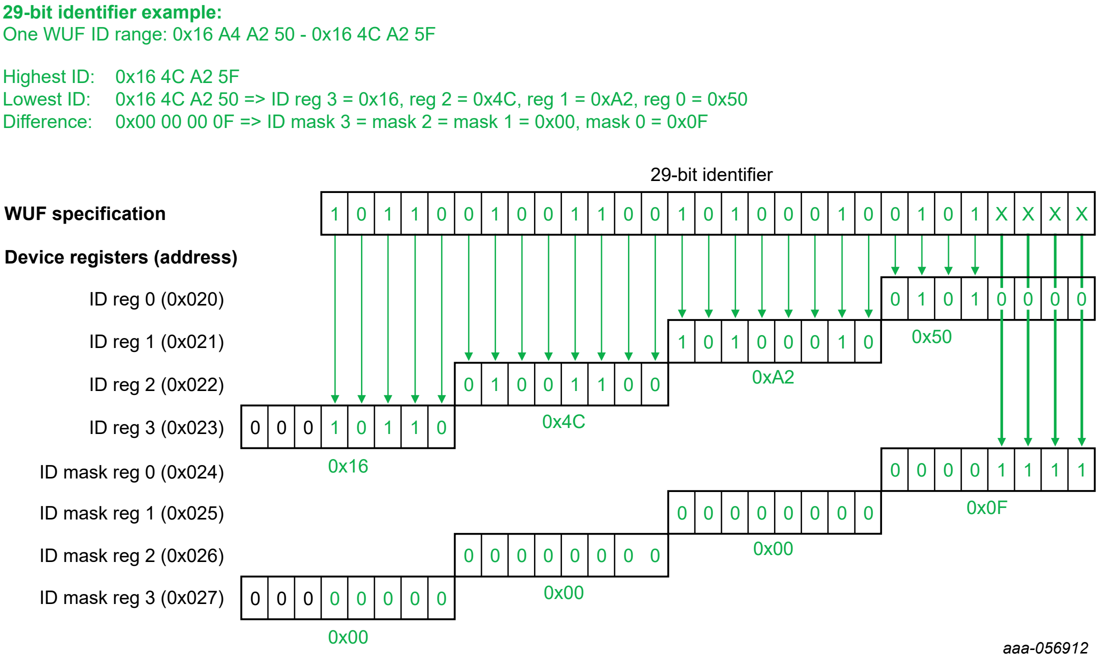


Figure 15. 29-bit ID configuration

4.1.3 DLC and data mask

If a wake-up has already been triggered when the received identifier was found to match the configuration, regardless of the DLC and data field contents (Figure 16), the appropriate contents for the frame control register is 0x00 for 11-bit WUF, or 0x80 for 29-bit WUF. Further configuration of data length code (DLC) or data mask is not needed in this case.

When the data field of the WUF is to be included for wake-up selection, each ‘1’ bit in the data field is supposed to address a group of network nodes. A WUF may address multiple groups by setting multiple bits in the data field to ‘1’. In turn, a PN transceiver may be assigned to several groups by setting the corresponding bits in the data mask registers to ‘1’. Then a PN transceiver only wakes up when:

- the ID of the WUF matches with the configuration as explained in Section 4.1.2
- and the WUF DLC matches the DLC in the frame control register
- and the WUF has a ‘1’ in one or more data field bit positions for which the transceiver has set the corresponding bits in the data mask registers to ‘1’.

The appropriate configuration of the frame control and data mask registers for an example with WUF DLC = 3 is illustrated in Figure 16.

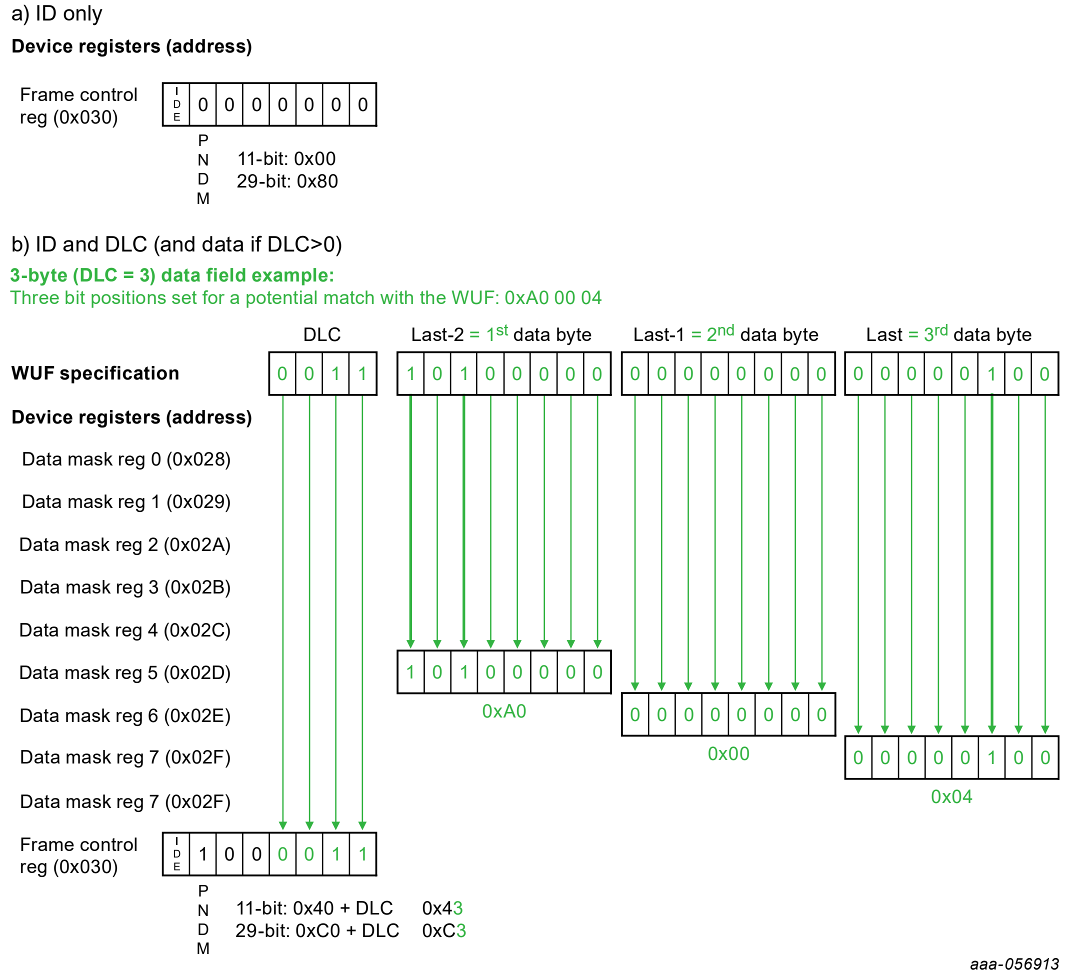


Figure 16. PN configuration with and without DLC and data field

4.1.4 Data rate

To decode the incoming classic CAN frame correctly, its bit rate must be defined via the CDR bits in the partial networking data rate and filter configuration register (address 0x031). In the example shown in Figure 17, the selected data rate is 500 kbit/s.

4.1.5 Optional CAN FD/CAN XL and FAST mode tolerance

When one of the other CAN frame formats, CAN FD or CAN XL, is expected to appear on the bus, the ‘CAN FD passive’ feature must be enabled by setting PNECC = 1 (in the partial networking and CAN configuration register). Note that the TJA1466 is the recommended product for CAN XL tolerance.

The PN decoder is not able to read the data phase of a CAN FD or CAN XL frame. When the PN passive function has recognized the FD or XL format of a CAN frame, it skips the rest of that frame by waiting for the bus to become idle (continuously recessive bus state for between 6 and 10 arbitration data rate bit times).

The FD passive function features a number of digital filter characteristics supporting the idle detection mechanism, including the two bitfilter options specified in ISO11898-2. Such a filter should reject ‘noise’, which is defined as dominant pulses shorter than would be expected in a CAN message (including CAN FD or CAN XL, if applicable). For example, the expected nominal minimum pulse length is 500 ns for 2 Mbit/s, 200 ns for 5 Mbit/s and 125 ns for 8 Mbit/s. The maximum value of the selected filter time $t_{fltr(bit)dom}$ must be lower than these pulse lengths, considering device tolerances and effects of bus physics. The bit filter requirements should ideally be defined by the system owner.

The ISO11898 filter options are defined as percentages of the arbitration bit time, which is the reciprocal of the chosen arbitration bit rate defined via the CDR. These filters should be the first choice for CAN FD speeds up to 5 Mbit/s. Example: when CDR = 100 (arbitration bit rate = 500 kbit/s), ISO bit filter 2 ignores pulses up to 175 ns, making it suitable for a data phase bit rate up to 5 Mbit/s.

The filter options are set via the idle detection filter select bits (IDFS in the partial networking data rate and filter configuration register at address 0x031). In addition to the ISO filter options, the TJA1446/66 provides a number of filter options with settings specified as absolute values independent of the CDR settings (bit filter 3, for example, ignores pulses up to 93 ns, which makes it suitable for communication up to 8 Mbit/s).

The properties of the two ISO filter options (with absolute filter times calculated for an arbitration data rate of 500 kbit/s), along with bit filter 3, are summarized in Table 7. Pulses longer than the max bit filter time value are never rejected. Pulses shorter than the min bit filter time value are always rejected. Pulses with lengths between these values may, or may not, be rejected.

Table 7. IDFS examples

	ISO bit filter 1 (IDFS = 0x1)	ISO bit filter 2 (IDFS = 0x2)	Bit filter 3 (IDFS = 0x3)
Min bit filter time	5 % (100 ns[1])	2.5 % (50 ns[1])	18 ns
Max bit filter time	17.5 % (350 ns[1])	8.75 % (175 ns[1])	93 ns
Max suitable data phase bit rate	2 Mbit/s[1]	5 Mbit/s[1]	8 Mbit/s[2]

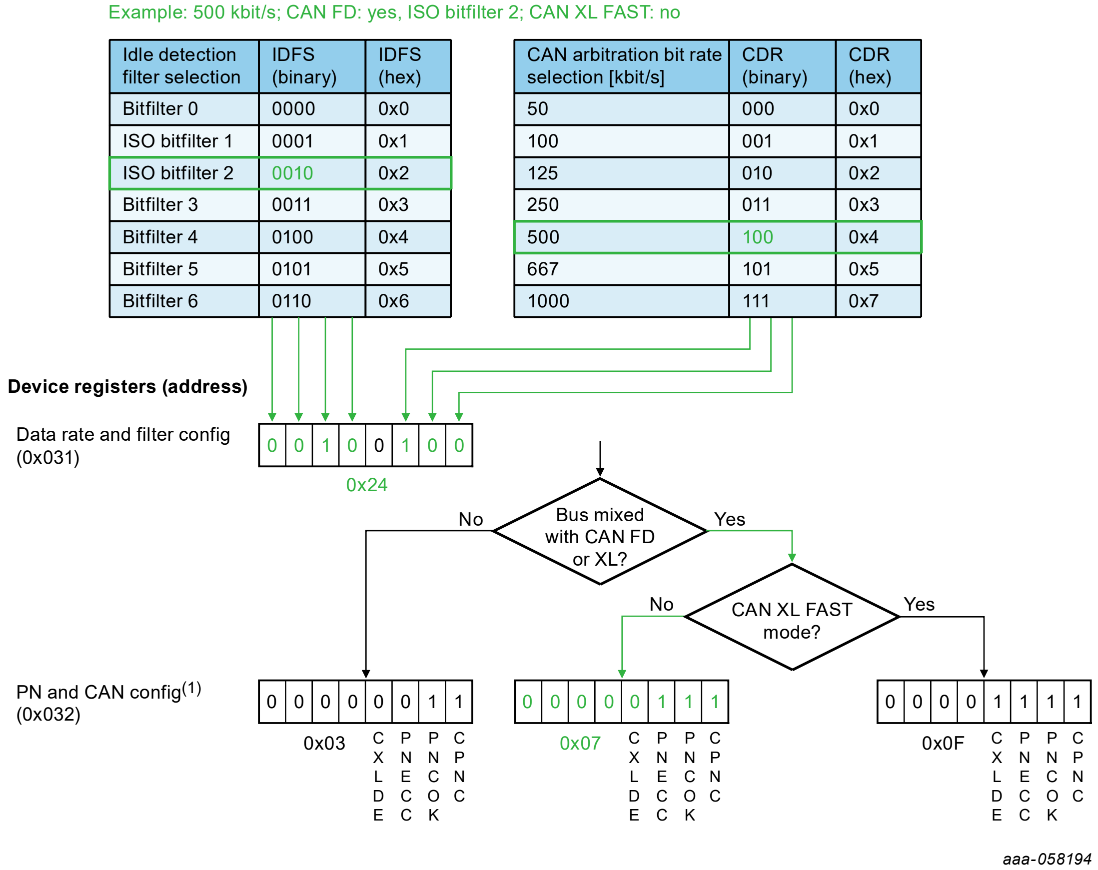
[1] This number is only valid for an arbitration data rate of 500 kbit/s (CDR = 100).

[2] Only applicable to the CAN SIC device.

With PNECC set to 1, a TJA1466 device tolerates not only CAN FD frames but also CAN XL frames sent in SIC mode. Only when CAN XL frames are sent using the FAST mode level scheme must bit CXLDE also be set to 1. As this function consumes additional current, it is recommended to disable it (CXLDE = 0) when not needed.

The appropriate register settings for a given data rate with or without CAN FD/CAN XL FAST mode tolerance are illustrated in Figure 17. The partial networking and CAN configuration register includes the PNCOK bit. Before setting this bit to 1, all other PN registers should have been initialized. After setting PNCOK = 1 and

CPNC = 1 (in the same register), the device is initialized to use the current contents of the PN registers for wake-up by WUF. However, the CWE bit in the system interrupt enable register must also be set to 1 for general CAN bus wake-up capability.



Example: 500 kbit/s; CAN FD: yes, ISO bitfilter 2; CAN XL FAST: no

Idle detection filter selection	IDFS (binary)	IDFS (hex)
Bitfilter 0	0000	0x0
ISO bitfilter 1	0001	0x1
ISO bitfilter 2	0010	0x2
Bitfilter 3	0011	0x3
Bitfilter 4	0100	0x4
Bitfilter 5	0101	0x5
Bitfilter 6	0110	0x6

CAN arbitration bit rate selection [kbit/s]	CDR (binary)	CDR (hex)
50	000	0x0
100	001	0x1
125	010	0x2
250	011	0x3
500	100	0x4
667	101	0x5
1000	111	0x7

(1) Here, the PN and CAN configuration register contents include PNCOK = 1 and CPNC = 1, which means this register should be the last PN configuration register written to.

Figure 17. PN configuration register settings for data rate and CAN FD / XL filter

4.2 Example SPI sequence for PN configuration and transition to Sleep mode

Table 8. Example SPI sequence for PN configuration and transition to Sleep mode
It is assumed that the device is Normal, Standby or ListenOnly mode, when starting the SPI sequence.

Action	Register name	Address	Content	Single-register SPI code	Multi-register SPI code
Enable CAN as wake source (CWE = 1)	System interrupt enable register	0x010	0x40	0x01 01 40	0x01 01 40
Select 11-bit format plus DLC = 3	Partial networking frame control register	0x030	0x43	0x03 00 43	0x03 03 43 24
Set data rate = 500 kbit/s and ISO filter 2	Partial networking data rate and filter configuration register	0x031	0x24	0x03 11 24	
Set WUF ID	Partial networking ID register 0	0x020	0x00	0x02 01 00	0x02 07 00 00 80 0B

Table 8. Example SPI sequence for PN configuration and transition to Sleep mode*...continued*

It is assumed that the device is Normal, Standby or ListenOnly mode, when starting the SPI sequence.

Action	Register name	Address	Content	Single-register SPI code	Multi-register SPI code
	Partial networking ID register 1	0x021	0x00	0x02 10 00	
	Partial networking ID register 2	0x022	0x80	0x02 20 80	
	Partial networking ID register 3	0x023	0x0B	0x02 31 0B	
Set WUF ID mask	Partial networking ID mask register 0	0x024	0x00	0x02 40 00	0x02 46 00 00 1C 04
	Partial networking ID mask register 1	0x025	0x00	0x02 51 00	
	Partial networking ID mask register 2	0x026	0x1C	0x02 61 1C	
	Partial networking ID mask register 3	0x027	0x04	0x02 70 04	
Set data mask 0-3	Partial networking data mask register 0	0x028	0x00	0x02 80 00	0x02 86 00 00 00 00
	Partial networking data mask register 1	0x029	0x00	0x02 91 00	
	Partial networking data mask register 2	0x02A	0x00	0x02 A1 00	
	Partial networking data mask register 3	0x02B	0x00	0x02 B0 00	
Set data mask 4-7	Partial networking data mask register 4	0x02C	0x00	0x02 C1 00	0x02 C7 00 A0 00 04
	Partial networking data mask register 5	0x02D	0xA0	0x02 D0 A0	
	Partial networking data mask register 6	0x02E	0x00	0x02 E0 00	
	Partial networking data mask register 7	0x02F	0x04	0x02 F1 04	
Finalize PN configuration with CAN FD passive, without CAN XL FAST	Partial networking and CAN configuration register	0x032	0x07	0x03 21 07	0x03 21 07
Clear all interrupts	System interrupt status register	0x060	0xFF	0x06 00 FF	0x06 06 FF FF FF FF
	CAN interrupt status register	0x061	0xFF	0x06 11 FF	
	Partial networking interrupt status register	0x062	0xFF	0x06 21 FF	
	GPIO interrupt status register	0x063	0xFF	0x06 30 FF	
Select Sleep mode	Mode control register	0x000	0x01	0x00 00 01	0x00 00 01

Table 8. Example SPI sequence for PN configuration and transition to Sleep mode*...continued*

It is assumed that the device is Normal, Standby or ListenOnly mode, when starting the SPI sequence.

Action	Register name	Address	Content	Single-register SPI code	Multi-register SPI code
Confirm Sleep mode (see Section 3.7.1)	Mode status register	0x070	0x00	0x07 08 00	0x07 08 00

4.3 Software development, MCU flash memory programming

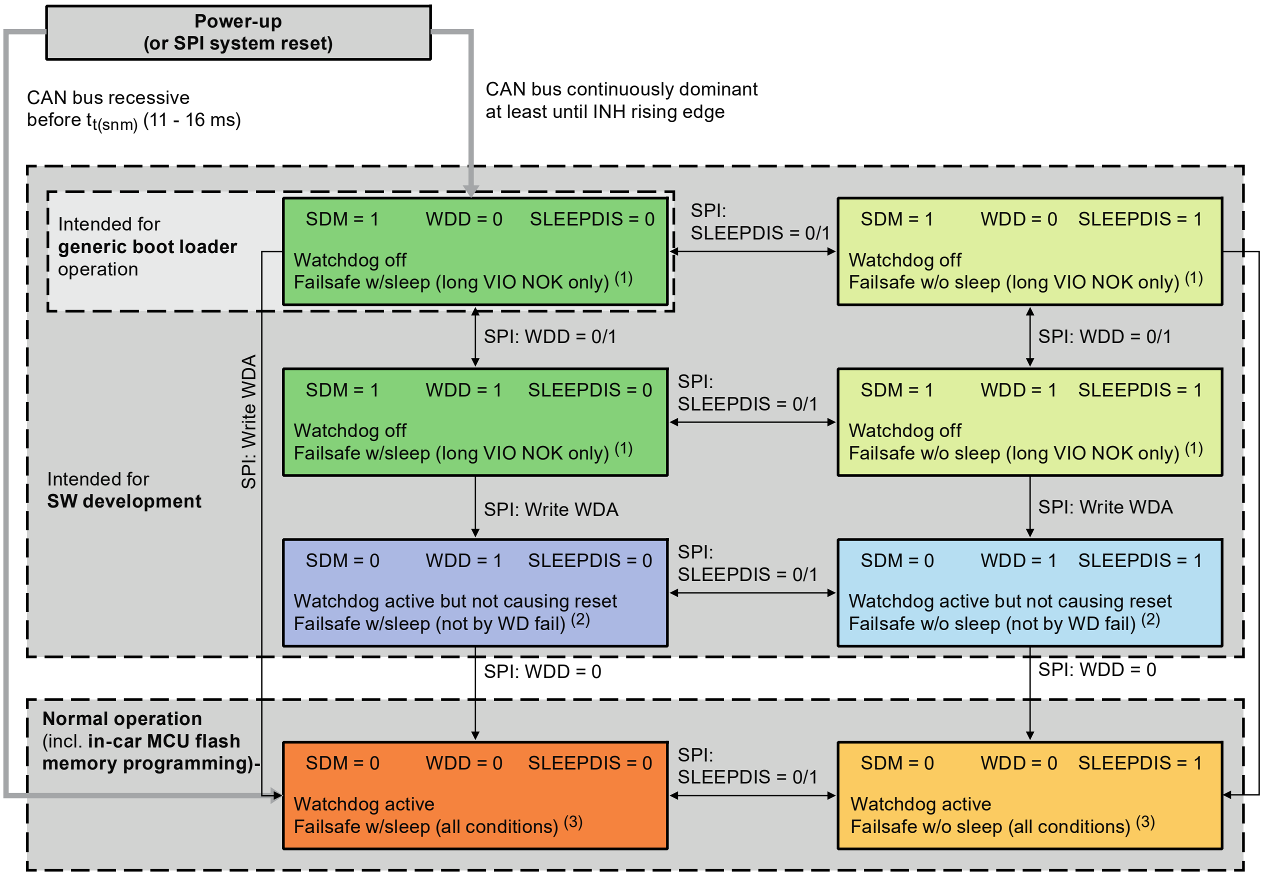
Figure 18 and Figure 19 provide an overview of the device modes discussed in the section:

- Software development mode (SDM, active when system status bit SDM = 1) ensures that the watchdog is off and Fail-safe mode is almost always disabled, see Figure 18.
- Start to Normal Mode (SNM, active when status bit SNMS = 1) puts the transceiver into Normal mode with CAN active, see Figure 19. Note that a LOW level on TXD would delay initial CAN activation until TXD goes HIGH. Also, CAN is not active during a V_{CC} undervoltage.

Both modes are activated automatically if the CAN bus switches to a dominant state ($V_{CANH} – V_{CANL} > 1.1$ V) before the main state machine FSM_MAIN enters Check_SNM mode, with the dominant state maintained for at least $t_{t(snm)}$. This can be achieved, for example, by connecting CANL to module GND and CANH to V_{BAT} or to an auxiliary power supply > 1.1 V before V_{BAT} powers up. CANH and CANL can be released as soon as the device has turned on INH. Note that this causes the device start-up time, from VBAT ramp-up to INH rising edge, to be lengthened by $t_{t(snm)}$.

The maximum voltage that may be applied to CANH is determined by the max voltage rating of the pin and by the max current or power rating of the bus termination resistors.

Forcing an SPI system reset by writing to the system reset register would mean that SDM/SNM mode would have to be renewed – if still required – by keeping the CAN bus dominant during device restart. Be aware that SPI system reset is not just a reset, but it also turns off several device pins (incl. INH) temporarily.

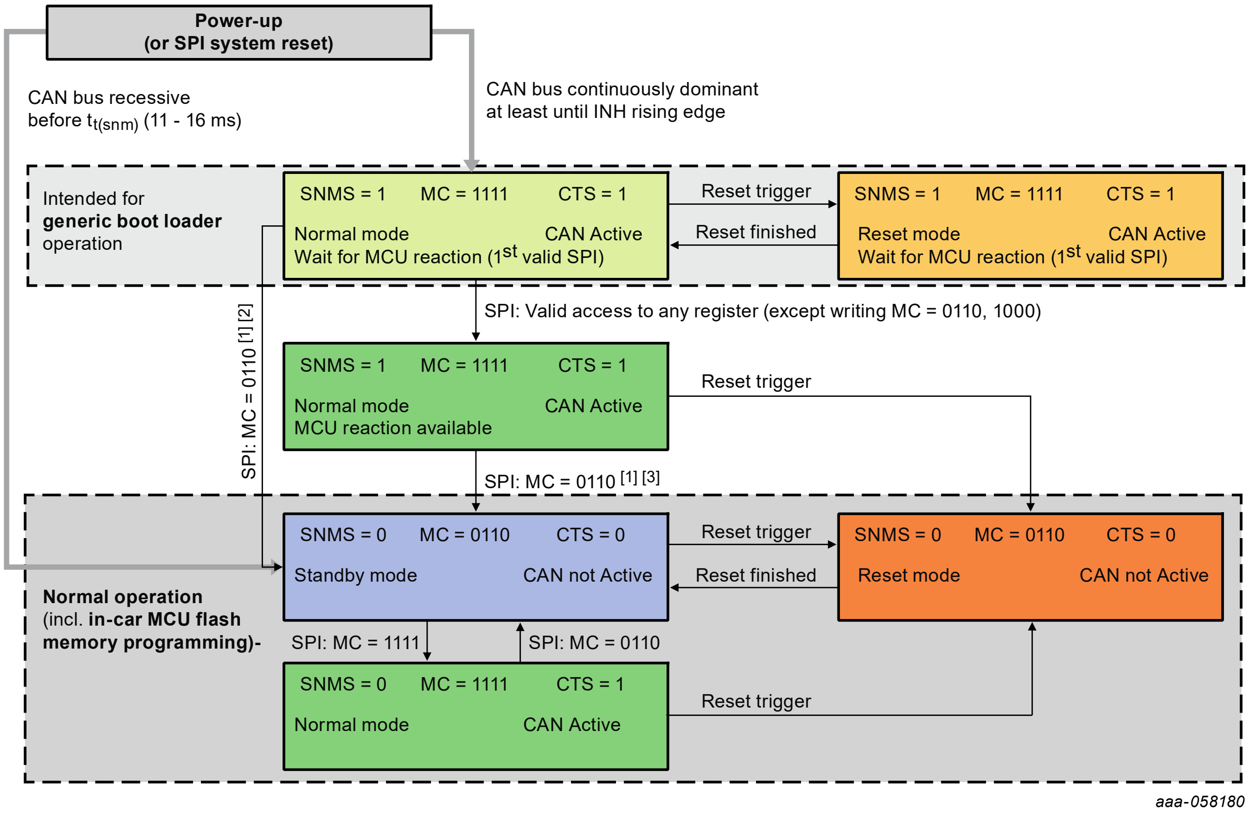


(1) Fail-safe mode only due to V_{IO} long (typ > 0.2 ms) overvoltage or long (typ > 125 ms) undervoltage (represented by the reset time out time $t_{to(rst)}$)

(2) Fail-safe mode only due to (1) or long (typ > 4 ms) RST_N LOW or FSCC > 1 by short VIO uv/ov or by short RST_N LOW

(3) Fail safe mode due to (2) or FSCC > 1 by WDFC = 3

Figure 18. Watchdog related modes available for generic boot loader usage or software development



(1) MC = 1000 (ListenOnly) would also clear SNMS

(2) MC = 0001 (Sleep) would be invalid since no wake sources enabled yet => no change

(3) MC = 0001 (Sleep) would clear SNMS only when a wake source has been enabled and all interrupts have already been.

Figure 19. CAN bus-related modes available for generic boot loader usage

4.3.1 Using a generic bootloader

A generic MCU bootloader would not be able to control the transceiver via SPI. This is not an issue when the device boots up with the bus dominant, as described above. The transceiver will be ready for the bootloader without the need for any SPI communication. Indeed, the absence of SPI accesses is ideal in this situation. When the bootloader has finished its task and the application program starts up, the transceiver will automatically cancel Software Development mode with the first watchdog service (writing any value to the WDA bits in the watchdog answer register), as illustrated in Figure 18. However, the device would then still be in Normal mode, and would remain in Normal mode until a reset is generated or the mode is changed via SPI (MC bits), see Figure 19. Note that a reset would not terminate Normal mode if it occurred before a valid SPI access.

4.3.2 Software development

4.3.2.1 Using development tools that drive the MCU reset signal

While an MCU debug or flash tool is connected to the PCB, it may drive the MCU reset signal. The RST_N pin signal may then need to be temporarily isolated from the MCU reset signal, see Section 2.2.4, Figure 9 and Figure 10.

In an application where the INH pin controls the voltage regulator(s) directly (i.e. INH off means regulator off), `debug jumper 1' (Section 2.1.4) may need to be set to avoid losing power to the MCU due to the device entering Fail-safe, then Sleep mode.

4.3.2.2 Disabling the watchdog during debugging

When the transceiver starts up in Software Development mode as described above, application software can be debugged without regular watchdog service if it is set up in one of the following two ways:

- To keep the device in Software Development mode, the software should avoid servicing the watchdog while SDM = 1 (see Section 3.5.8 and Section 3.6.1)
- Instead of keeping the watchdog disabled, it can be activated without the ability to generate resets. This is achieved by initializing WDD = 1 (Section 3.5.6) before the first write access to the watchdog answer (WDA) register. Regular watchdog service can then be executed, but a missing watchdog service will not generate a reset. However, since SDM will be cleared, pulling RST_N LOW (e.g. with a reset button on the board) or a V_{IO} under/overvoltage event would cause the device to enter Fail-safe mode. If not disabled by setting SLEEPDIS = 1 (Section 3.5.7), the device would then enter Sleep mode, driving RST_N LOW until the next wake-up event.

4.3.3 In-car MCU flash memory programming

When the watchdog cannot be serviced during in-car flash programming, the watchdog period should be set to the longest value (WDP = 7) and WDFC cleared to 0. Immediately before starting the programming process, trigger the watchdog (switch first to Standby mode to set the watchdog to Timeout mode) and clear WDFC. When necessary, enter Normal mode to enable CAN communication via this transceiver. The next watchdog service will be due before the selected period has elapsed three times, at the latest. Calculate using the minimum values of the period for worst-case timing. Each time WDFC is cleared, the due time is postponed by at least two periods.

4.4 Pin failure mode and effects analysis (FMEA) of the TJA1445x/TJA1446x/ TJA1465x/TJA1466x family

Table 9. Failure classification used in pin FMEA tables

A	damage to device; bus may be affected
B	no damage to device; bus communication not possible
C	no damage to device; bus communication possible; corrupted node excluded from communication
D	no damage to device; bus communication possible; reduced functionality of device or system

Table 10. Pin FMEA of TJA1445A and TJA1465A, part 1

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		Class	Mode	Class	Mode	Class	Mode
1	TXD	A	limiting value exceeded	C	TXD clamped recessive; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	TXD clamped recessive
2	GND	C	node is left unpowered and behaves passive to the bus (biasing off)	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	V_{IO} undervoltage detected; device enters Sleep mode

Table 10. Pin FMEA of TJA1445A and TJA1465A, part 1*...continued*

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		Class	Mode	Class	Mode	Class	Mode
3	VCC	A	limiting value exceeded	-	n/a	D	potential damage to µC I/O pin at 1.8 V-3.3 V V_{IO} or V_{CC} undervoltage detected with device behaving passive to the bus (biasing on)
4	RXD	A	limiting value exceeded	C	RXD clamped recessive; bus communication may be disturbed; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	RXD clamped recessive; bus communication may be disturbed
5	VIO	A	limiting value exceeded	D	host interface voltage pulled to higher V_{CC} supply (5 V); potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	-	n/a
6	SDO	A	limiting value exceeded	C	cannot read SPI from device; behavior depends on software; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	cannot read SPI from device; behavior depends on software
7	INH	D	INH-controlled regulators remain on permanently	D	INH-controlled regulators may remain on permanently	C	INH-controlled regulators may remain on or off permanently
8	SCK	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device
9	WAKE	D	local wake-up not possible	D	local wake-up not possible	D	local wake-up not possible
10	VBAT	-	n/a	A	limiting value exceeded	A	limiting value exceeded
11	SDI	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device
12	CANL	B	bus clamped recessive; bus communication not possible	B	bus clamped recessive; bus communication not possible	B	CANL clamped recessive; bus communication might be possible at low V_{IO}, but in principle no bus communication is possible
13	CANH	D	degradation of EMC; bit timing violation possible	D	degradation of EMC; bit timing violation possible	D	degradation of EMC; bit timing violation possible
14	SCSN	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O or the	C	no communication towards device

Table 10. Pin FMEA of TJA1445A and TJA1465A, part 1*...continued*

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		Class	Mode	Class	Mode	Class	Mode
					complete µC at V_{IO} = 1.8 V-3.3 V		

Table 11. Pin FMEA of TJA1445A and TJA1465A, part 2

		Short to GND		Pin open		Short to neighbor	
Pin		Class	Mode	Class	Mode	Class	Mode
1	TXD	C	transmitter disabled (either because it is not able to enter CAN Active mode, or due to a TXD dominant timeout)	C	TXD clamped recessive	C	TXD-GND: transmitter disabled (either because it is not able to enter CAN Active mode, or due to a TXD dominant timeout)
2	GND	-	n/a	C	floating voltages on the supply pin can lead to an undervoltage; device then enters Off mode and behaves passive to the bus	C	GND-VCC: V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)
3	VCC	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	VCC-RXD: RXD clamped recessive; bus communication may be disturbed; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V
4	RXD	C	RXD clamped dominant	C	when the MCU signal is floating, the node may continue to generate error frames until it enters bus-off state	C	RXD-VIO: RXD clamped recessive; bus communication may be disturbed
5	VIO	C	V_{IO} undervoltage detected; device enters Sleep mode	C	V_{IO} undervoltage detected; device enters Sleep mode	C	VIO-SDO: cannot read SPI from device; behavior depends on software
6	SDO	C	cannot read SPI from device; behavior depends on software	C	cannot read SPI from device; behavior depends on software	A	SDO-INH: cannot read SPI from device; potential damage to the µC I/O or the complete µC due to INH output voltage; SDO pin could also be damaged
7	INH	C[1]	INH-controlled regulators remain off permanently	C	INH-controlled regulators remain off permanently	-	n/a
8	SCK	C	no communication towards device	C	no communication towards device	A	SCK-WAKE: potential damage to SCK pin if WAKE pin voltage related to V_{BAT} supply; potential damage to the µC I/O or the complete µC; no

Table 11. Pin FMEA of TJA1445A and TJA1465A, part 2*...continued*

		Short to GND		Pin open		Short to neighbor	
Pin		**Class**	**Mode**	**Class**	**Mode**	**Class**	**Mode**
							communication towards device
9	WAKE	D	local wake-up not possible	D	local wake-up not possible	D	WAKE-VBAT: local wake-up not possible
10	VBAT	C	node left unpowered and behaves passive to the bus (biasing off)	C	node left unpowered and behaves passive to the bus (biasing off)	A	VBAT-SDI: SDI limiting value exceeded; potential damage to the µC I/O or the complete µC
11	SDI	C	no communication towards device	C	no communication towards device	A	SDI-CANL: no communication towards device; damage to SDI pin and potential damage to the µC I/O or the complete µC
12	CANL	D	degradation of EMC; bit timing violation possible	C	bus communication not possible	B	CANL-CANH: bus clamped recessive, bus communication not possible
13	CANH	B	bus clamped recessive; bus communication not possible	C	bus communication not possible	A	CANH-SCSN: no communication towards device; potential damage to SCSN pin and potential damage to the µC I/O or the complete µC
14	SCSN	C	no communication towards device	C	no communication towards device	-	n/a

[1] Exceeding the rated current may reduce device lifetime. See section 'Limiting values' in the data sheet.

Table 12. Pin FMEA of TJA1445B and TJA1465B, part 1

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		**Class**	**Mode**	**Class**	**Mode**	**Class**	**Mode**
1	TXD	A	limiting value exceeded	C	TXD clamped recessive; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	TXD clamped recessive
2	GND	C	node is left unpowered and behaves passive to the bus (biasing off)	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	V_{IO} undervoltage detected; device enters Sleep mode
3	VCC	A	limiting value exceeded	-	n/a	D	potential damage to µC I/O pin at 1.8 V-3.3 V V_{IO} or V_{CC} undervoltage detected with device behaving passive to the bus (biasing on)

Table 12. Pin FMEA of TJA1445B and TJA1465B, part 1*...continued*

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		Class	Mode	Class	Mode	Class	Mode
4	RXD	A	limiting value exceeded	C	RXD clamped recessive; bus communication may be disturbed; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	RXD clamped recessive; bus communication may be disturbed
5	VIO	A	limiting value exceeded	D	host interface voltage pulled to higher V_{CC} supply (5 V); potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	-	n/a
6	SDO	A	limiting value exceeded	C	cannot read SPI from device; behavior depends on software; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	cannot read SPI from device; behavior depends on software
7	INH	D	INH-controlled regulators remain on permanently	D	INH-controlled regulators may remain on permanently	C	INH-controlled regulators may remain on or off permanently
8	GPIO3	A	limiting value exceeded	C	no damage to device; GPIO3 function not usable; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	D	no damage to device; GPIO3 function not usable
9	TXEN_N	A	limiting value exceeded	C[1]	no damage to the device; transmitter cannot be enabled; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C[1]	transmitter cannot be enabled
10	SCK	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device
11	WAKE	D	local wake-up not possible	D	local wake-up not possible	D	local wake-up not possible
12	VBAT	-	n/a	A	limiting value exceeded	A	limiting value exceeded
13	SDI	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device
14	CANL	B	bus clamped recessive; bus communication not possible	B	bus clamped recessive; bus communication not possible	B	CANL clamped recessive; bus communication might be possible at low

Table 12. Pin FMEA of TJA1445B and TJA1465B, part 1*...continued*

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		Class	Mode	Class	Mode	Class	Mode
							V_{IO}, but in principle bus communication is not possible
15	CANH	D	degradation of EMC; bit timing violation possible	D	degradation of EMC; bit timing violation possible	D	degradation of EMC; bit timing violation possible
16	SCSN	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device
17	GPIO1	A	limiting value exceeded	C	no damage to the device; GPIO1 function unusable; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	D	no damage to the device; GPIO2 function unusable
18	GPIO2	A	limiting value exceeded	C	no damage to the device; GPIO2 function unusable; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	D	no damage to the device; GPIO2 function unusable

[1] Exceeding the rated current may reduce device lifetime. See section 'Limiting values' in the data sheet.

Table 13. Pin FMEA of TJA1445B and TJA1465B, part 2

		Short to GND		Pin open		Short to neighbor	
Pin		Class	Mode	Class	Mode	Class	Mode
1	TXD	C	transmitter disabled (either because it is not able to enter CAN Active mode, or due to a TXD dominant timeout)	C	TXD clamped recessive	C	TXD-GND: transmitter disabled (either because it is not able to enter CAN Active mode, or due to a TXD dominant timeout)
2	GND	-	n/a	C	floating voltages on the supply pin can lead to an undervoltage; device then enters Off mode and behaves passive to the bus	C	GND-VCC: V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)
3	VCC	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	VCC-RXD: RXD clamped recessive; bus communication may be disturbed; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V
4	RXD	C	RXD clamped dominant	C	when the MCU signal is floating, the node may continue to generate	C	RXD-VIO: RXD clamped recessive; bus communication may be disturbed

Table 13. Pin FMEA of TJA1445B and TJA1465B, part 2*...continued*

		Short to GND		Pin open		Short to neighbor	
Pin		Class	Mode	Class	Mode	Class	Mode
					error frames until it enters bus-off state		
5	VIO	C	V_{IO} undervoltage detected; device enters Sleep mode	C	V_{IO} undervoltage detected; device enters Sleep mode	C	VIO-SDO: cannot read SPI from device; behavior depends on software
6	SDO	C	cannot read SPI from device; behavior depends on software	C	cannot read SPI from device; behavior depends on software	A	SDO-INH: cannot read SPI from device; potential damage to the µC I/O or the complete µC due to INH output voltage; SDO pin could also be damaged
7	INH	C[1]	INH-controlled regulators remain off permanently	C	INH-controlled regulators remain off permanently	A	INH-GPIO3: potential deactivation of ECU regulators by GPIO3 signal on INH pin; potential damage to GPIO3 pin or to the µC I/O or the complete µC due to INH output voltage
8	GPIO3	D	no damage to device; GPIO3 function unusable	D	no damage to device; GPIO3 function unusable	C	GPIO3-TXEN_N: no damage to device; transmitter could be disabled and GPIO3 function unusable
9	TXEN_N	D	transmitter cannot be disabled externally	C	transmitter cannot be disabled externally	C	TXEN_N-SCK: SCK causes transmiter to be continuously enabled and disabled; no communication towards device.
10	SCK	C	no communication towards device	C	no communication towards device	A	SCK-WAKE: potential damage to SCK pin if WAKE pin voltage related to V_{BAT} supply; potential damage to the µC I/O or the complete µC; no communication towards device
11	WAKE	D	local wake-up not possible	D	local wake-up not possible	D	WAKE-VBAT: local wake-up not possible
12	VBAT	C	node left unpowered and behaves passive to the bus (biasing off)	C	node left unpowered and behaves passive to the bus (biasing off)	A	VBAT-SDI: SDI limiting value exceeded; potential damage to the µC I/O or the complete µC
13	SDI	C	no communication towards device	C	no communication towards device	A	SDI-CANL: no communication towards device; damage to SDI pin and potential damage

Table 13. Pin FMEA of TJA1445B and TJA1465B, part 2*...continued*

		Short to GND		Pin open		Short to neighbor	
Pin		Class	Mode	Class	Mode	Class	Mode
							to the µC I/O or the complete µC
14	CANL	D	degradation of EMC; bit timing violation possible	C	bus communication not possible	B	CANL-CANH: bus clamped recessive, bus communication not possible
15	CANH	B	bus clamped recessive; bus communication not possible	C	bus communication not possible	A	CANH-SCSN: no communication towards device; potential damage to SCSN pin and potential damage to the µC I/O or the complete µC
16	SCSN	C	no communication towards device	C	no communication towards device	C	SCSN-GPIO1: no SPI communication possible; GPIO1 function unusable
17	GPIO1	D	no damage to device; GPIO1 function unusable	D	no damage to device; GPIO1 function unusable	D	GPIO1 - GPIO2: no damage to device; GPIO1 and GPIO2 functions unusable.
18	GPIO2	D	no damage to device; GPIO2 function unusable	D	no damage to device; GPIO2 function unusable	C	GPIO2-TXD: no damage to device; communication towards TXD may not be possible.

[1] Exceeding the rated current may reduce device lifetime. See section 'Limiting values' in the data sheet.

Table 14. Pin FMEA of TJA1446x and TJA1466x, part 1

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		Class	Mode	Class	Mode	Class	Mode
1	TXD	A	limiting value exceeded	C	TXD clamped recessive; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	TXD clamped recessive
2	GND	C	node is left unpowered and behaves passive to the bus (biasing off)	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	V_{IO} undervoltage detected; device enters Sleep mode and pulls RST_N LOW (safe state)
3	VCC	A	limiting value exceeded	-	n/a	D	potential damage to µC I/O pin at 1.8 V-3.3 V V_{IO} or V_{CC} undervoltage detected with device behaving passive to the bus (biasing on)
4	RXD	A	limiting value exceeded	C	RXD clamped recessive; bus communication may be disturbed; potential damage to the µC I/O pin	C	RXD clamped recessive; bus communication may be disturbed

Table 14. Pin FMEA of TJA1446x and TJA1466x, part 1*...continued*

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		Class	Mode	Class	Mode	Class	Mode
					or to the complete µC at V_{IO} = 1.8 V-3.3 V		
5	VIO	A	limiting value exceeded	C	host interface voltage pulled to higher V_{CC} supply (5 V); potential damage to the µC I/O pin or to the complete µC at V_{IO} = 1.8 V-3.3 V	-	n/a
6	SDO	A	limiting value exceeded	C	cannot read SPI from device; behavior depends on software; potential damage to the µC I/O pin or the complete µC at V_{IO} = 1.8 V-3.3 V	C	cannot read SPI from device; behavior depends on software
7	INH	D	INH-controlled regulators remain on permanently	D	INH-controlled regulators may remain on permanently	C	INH-controlled regulators may remain on or off permanently
8	LIMPFSO_N	D[1]	no damage to device; LIMPFSO_N functionality not usable in the application	D[1]	no damage to device; LIMPFSO_N functionality not usable in the application	D[1]	no damage to device; LIMPFSO_N functionality not usable in the application
9	RST_N	A	limiting value exceeded	C[1]	no damage to the device; system reset not possible; ECU might not start correctly; WD failures cannot reset the controller and, consequently, a SW problem will not be detected; potential damage to the µC I/O pin or the complete µC at V_{IO} = 1.8 V-3.3 V	D[1]	system reset not possible; ECU might not start correctly; WD failures cannot reset the controller and, consequently, a SW problem will not be detected
10	SCK	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O pin or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device
11	WAKE	D	local wake-up not possible	D	local wake-up not possible	D	local wake-up not possible
12	VBAT	-	n/a	A	limiting value exceeded	A	limiting value exceeded
13	SDI	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O pin or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device

Table 14. Pin FMEA of TJA1446x and TJA1466x, part 1*...continued*

		Short to V_{BAT} (12 V to 40 V)		Short to V_{CC} (5 V)		Short to V_{IO} (1.8 V/3.3 V/5.0 V)	
Pin		**Class**	**Mode**	**Class**	**Mode**	**Class**	**Mode**
14	CANL	B	bus clamped recessive; bus communication not possible	B	bus clamped recessive; bus communication not possible	B	CANL clamped recessive; bus communication might be possible at low V_{IO}, but in principle bus communication is not possible
15	CANH	D	degradation of EMC; bit timing violation possible	D	degradation of EMC; bit timing violation possible	D	degradation of EMC; bit timing violation possible
16	SCSN	A	limiting value exceeded	C	no communication towards device; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	C	no communication towards device
17	GPIO1	A	limiting value exceeded	C	no damage to the device; GPIO1 function unusable; potential damage to the µC I/O pin or the complete µC at V_{IO} = 1.8 V-3.3 V	D	no damage to the device; GPIO2 function unusable
18	GPIO2	A	limiting value exceeded	C	no damage to the device; GPIO2 function unusable; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V	D	no damage to the device; GPIO2 function unusable
					no damage to the device; GPIO2 function unusable; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V		

[1] Exceeding the rated current may reduce device lifetime. See section 'Limiting values' in the data sheet.

Table 15. Pin FMEA of TJA1446x and TJA1466x, part 2

		Short to GND		Pin open		Short to neighbor	
Pin		**Class**	**Mode**	**Class**	**Mode**	**Class**	**Mode**
1	TXD	C	transmitter disabled (either because it is not able to enter CAN Active mode, or due to a TXD dominant timeout)	C	TXD clamped recessive	C	TXD-GND: transmitter disabled (either because it is not able to enter CAN Active mode, or due to a TXD dominant timeout)
2	GND	-	n/a	C	floating voltages on the supply pin can lead to an undervoltage; device then enters Off mode	C	GND-VCC: V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)

Table 15. Pin FMEA of TJA1446x and TJA1466x, part 2*...continued*

		Short to GND		Pin open		Short to neighbor	
Pin		**Class**	**Mode**	**Class**	**Mode**	**Class**	**Mode**
					and behaves passive to the bus		
3	VCC	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	V_{CC} undervoltage detected; device behaves passive to the bus (biasing on)	C	VCC-RXD: RXD clamped recessive; bus communication may be disturbed; potential damage to the µC I/O or the complete µC at V_{IO} = 1.8 V-3.3 V
4	RXD	C	RXD clamped dominant	C	when the MCU signal is floating, the node may continue to generate error frames until it enters bus-off state	C	RXD-VIO: RXD clamped recessive; bus communication may be disturbed
5	VIO	C	V_{IO} undervoltage detected; device enters Sleep mode and pulls RST_N LOW (safe state)	C	V_{IO} undervoltage detected; device enters Sleep mode and pulls RST_N LOW (safe state)	C	VIO-SDO: cannot read SPI from device; behavior depends on software
6	SDO	C	cannot read SPI from device; behavior depends on software	C	cannot read SPI from device; behavior depends on software	A	SDO-INH: cannot read SPI from device; potential damage to the µC I/O or the complete µC due to INH output voltage; SDO pin could also be damaged
7	INH	C[1]	INH-controlled regulators remain off permanently	C	INH-controlled regulators remain off permanently	C	INH-LIMPFSO_N: potential deactivation of ECU regulators by LIMPFSO_N signal on INH pin; potential damage to LIMPFSO_N pin or to the µC I/O or the complete µC due to INH output voltage
8	LIMPFSO_N	D	no damage to device; LIMPFSO_N functionality not usable in the application	D	no damage to device; LIMPFSO_N functionality not usable in the application	A	LIMPFSO_N-RST_N: [1] LIMP application: depending on load conditions, potential damage to the RST_N pin and to the µC I/O or the complete µC
						D	[2] FSO application: proper system reset not possible.
9	RST_N	C	permanent system reset	D	system reset not possible; ECU might not start correctly; WD failures cannot reset the controller and, consequently, a SW	C	RST_N-SCK: continuous system resets

Table 15. Pin FMEA of TJA1446x and TJA1466x, part 2*...continued*

		Short to GND		Pin open		Short to neighbor	
Pin		Class	Mode	Class	Mode	Class	Mode
					problem will not be detected		
10	SCK	C	no communication towards device	C	no communication towards device	A	SCK-WAKE: potential damage to SCK pin if WAKE pin voltage related to V_{BAT} supply; potential damage to the µC I/O or the complete µC; no communication towards device
11	WAKE	D	local wake-up not possible	D	local wake-up not possible	D	WAKE-VBAT: local wake-up not possible
12	VBAT	C	node left unpowered and behaves passive to the bus (biasing off)	C	node left unpowered and behaves passive to the bus (biasing off)	A	VBAT-SDI: SDI limiting value exceeded; potential damage to the µC I/O or the complete µC
13	SDI	C	no communication towards device	C	no communication towards device	A	SDI-CANL: no communication towards device; damage to SDI pin and potential damage to the µC I/O or the complete µC
14	CANL	D	degradation of EMC; bit timing violation possible	C	bus communication not possible	B	CANL-CANH: bus clamped recessive, bus communication not possible
15	CANH	B	bus clamped recessive; bus communication not possible	C	bus communication not possible	A	CANH-SCSN: no communication towards device; potential damage to SCSN pin and potential damage to the µC I/O or the complete µC
16	SCSN	C	no communication towards device	C	no communication towards device	C	SCSN-GPIO1: no SPI communication possible; GPIO1 function unusable
17	GPIO1	D	no damage to device; GPIO1 function unusable	D	no damage to device; GPIO1 function unusable	D	GPIO1 - GPIO2: no damage to device; GPIO1 and GPIO2 functions unusable.
18	GPIO2	D	no damage to device; GPIO2 function unusable	D	no damage to device; GPIO2 function unusable	C	GPIO2-TXD: no damage to device; communication towards TXD may not be possible.

[1] Exceeding the rated current may reduce device lifetime. See section 'Limiting values' in the data sheet.

5 References

[1] **TJA1446 data sheet** — High-speed CAN transceiver with partial networking and advanced system monitoring

[2] **TJA1466 data sheet** — CAN SIC transceiver with partial networking and advanced system monitoring

[3] **TR1135 application hints** — Rules and recommendations for in-vehicle CAN networks

[4] **UM12193** — TJA14x6 safety manual

6 Revision history

Table 16. Revision history

Document ID	Release date	Description
AN14452 v.1.0	18 November 2024	• Initial version

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