AN14505

EV Traction Inverter Reference Design Gen 3 System application note

Rev. 1.0 — 7 February 2025 **Application note**

Document information

Information	Content
Keywords	Traction Inverter Reference Design, Dynamic Gate Strength, Software, System FuSa, Efficiency, S32K39 MCU, FS26 SBC, GD3162 HV Gate Driver
Abstract	The purpose of this system application note is to provide introduction information related to system anatomy, performance, and offering for the EV Traction Inverter Reference Design Gen3. Further document such User Manual, SW AN, Device Datasheet , FuSa Documents complement this application note.

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1 Introduction

The purpose of this system application note is to provide detailed information about the EV Traction Inverter Reference Design Gen 3. This document describes the detailed functions of the application and system, and forms a clear and comprehensive document for our customers.

Some system KPIs are reported to illustrate concrete achievable performance in a dedicated test setup environment. This document should ease system understanding for our customers from a device, hardware, software, and collateral point of view.

Further documentation related to the device, subsystem, and safety are available in Section 6.

A dedicated user manual is also available to assemble and enable the reference design with and without our recommended third-party vendor.

2 System overview

2.1 General description

Compared to the previous reference design (https://www.nxp.com/design/design-center/development-boards-and-designs/ev-power-inverter-control-reference-platform-gen-2:EV-INVERTERHDBT), this new NXP traction inverter control reference targets the upcoming trend of 800 V silicon carbide (SiC)-based inverter applications by applying the latest generation of NXP high-performance electrification devices.

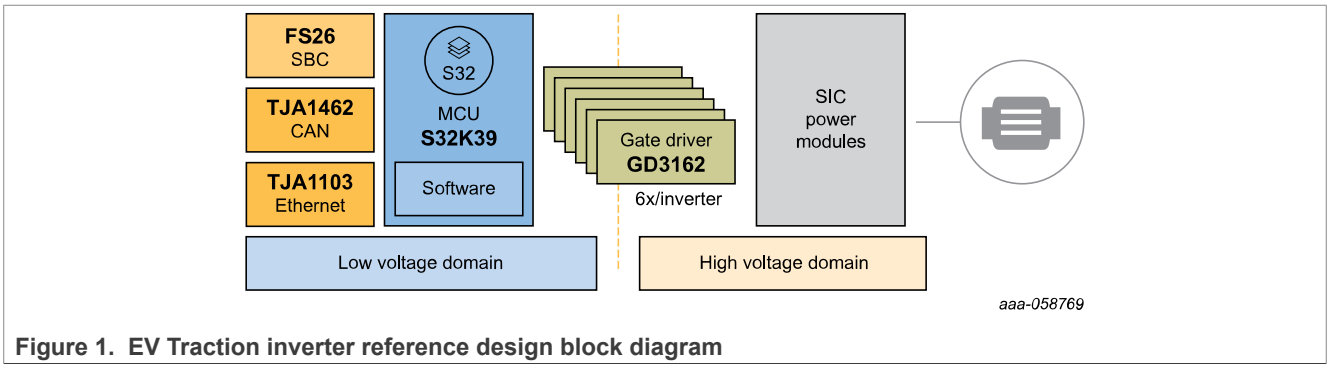

Figure 1. EV Traction inverter reference design block diagram

This reference design and its extensive set of collaterals ease customers in their own design to address key challenges for EV traction inverter system as shown in Figure 2.

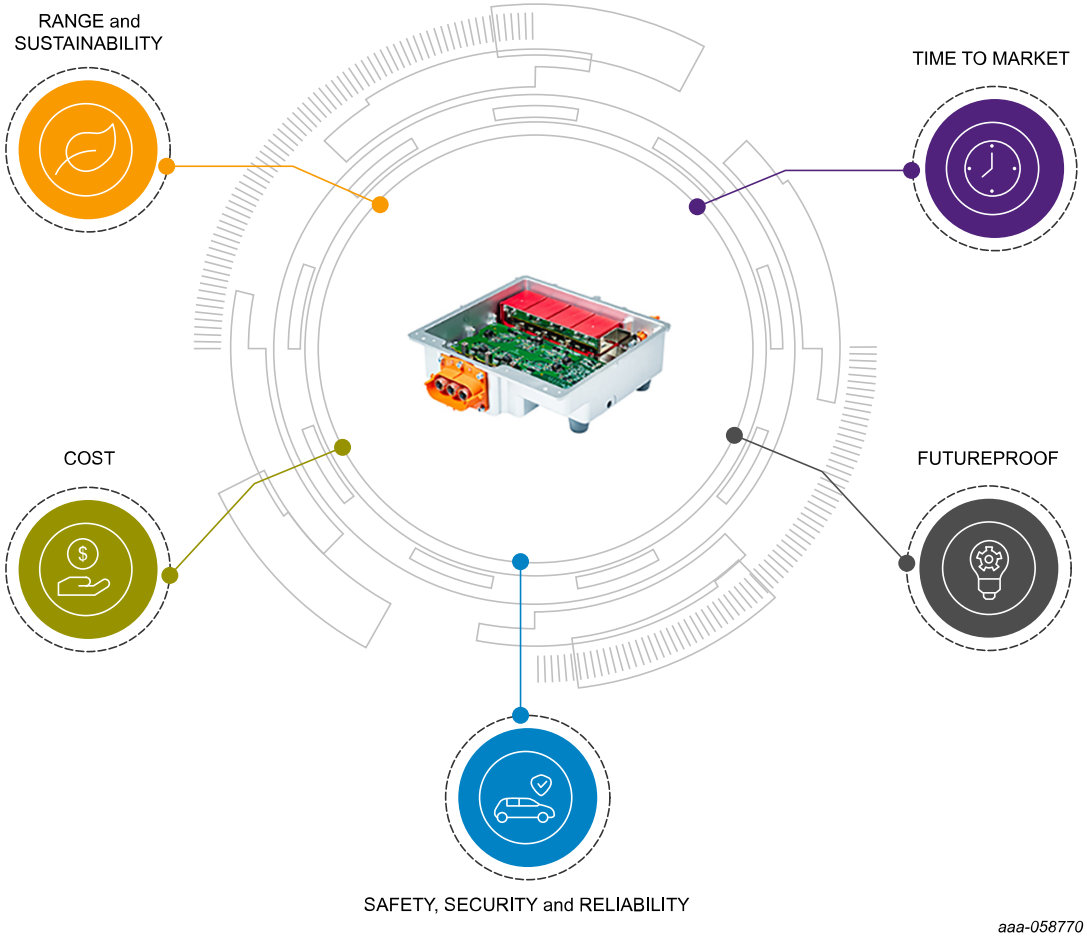

Figure 2. EV traction inverter key challenges

2.2 Block diagram

The following list contains different NXP devices and their uses:

DCDC

- S32K39 MCU for controlling speed and torque of eMotor through PWM switching and I/V and position sensing
- FS26 SBC for system supply and FuSa [6]
- GD3162 Gate driver [1] devices for performing LV to HV switching and protection of power devices[1] (not provided in the reference design offer)
- TJA146X CAN to communicate with a vehicle control unit (VCU) [7]
- TJA1103 Ethernet phy as an alternative to communicate with the VCU [8]. The Ethernet phy is accessible via a dedicated connector.

1 Not provided in the reference design offer- 3rd party to be involved.

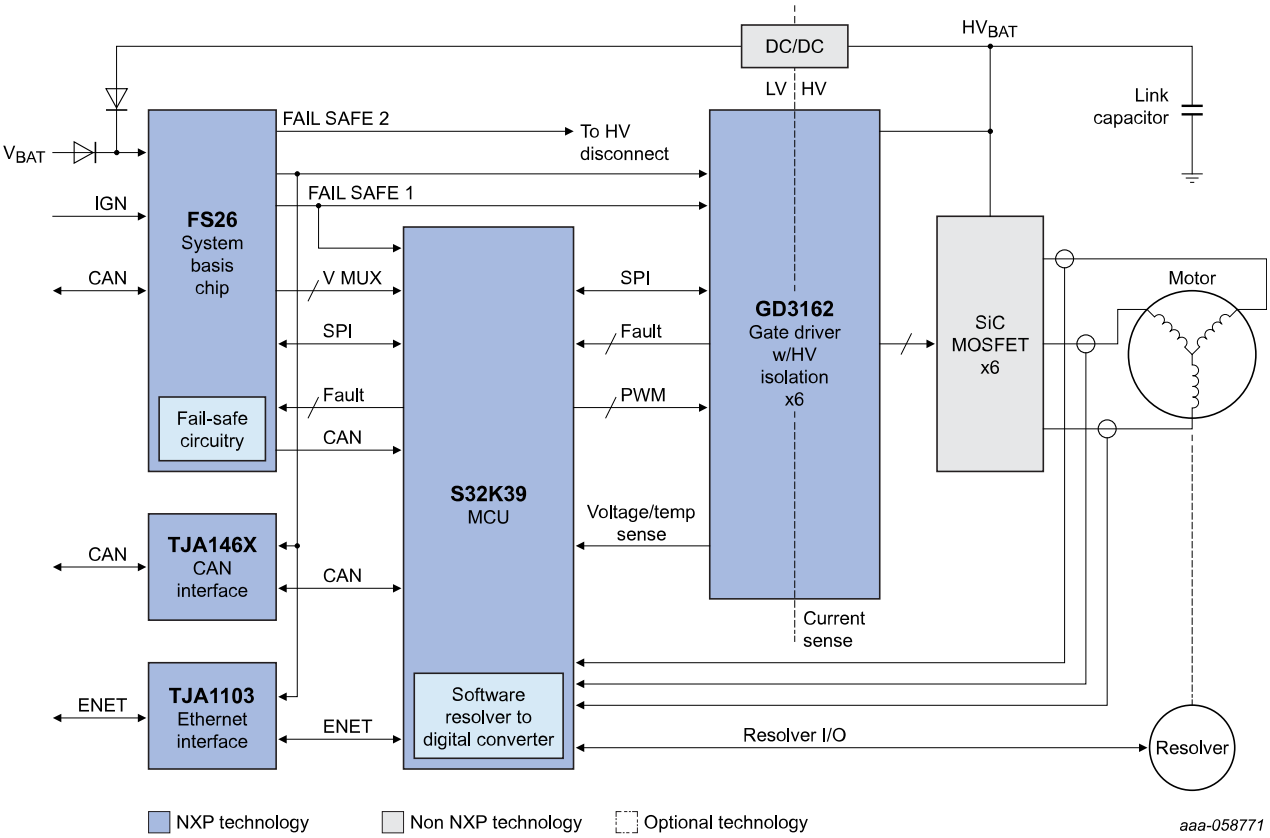

Figure 3. EV Traction inverter reference design block diagram (HV/LV DCDC not implemented)

2.3 YM Wolfspeed SiC power module

Wolfspeed's YM3 six-pack power module family comprises an industry standard footprint specifically engineered to make the integration of SiC into passenger, commercial, and agricultural vehicle traction applications straightforward and dependable. The YM3 module incorporates an optimized DC busbar design that achieves best-in-class package inductance and provides significantly reduced switching energy and lower voltage overshoots than similar modules in this form factor. Additionally, this power module is encapsulated with a hard epoxy, which enhances its robustness and allows for lower operational and storage temperatures. Furthermore, the YM3 incorporates a sintered die attach, high reliability welded power terminal connections, and a copper clip top-side connection to the die, which work together to greatly enhance the package's reliability and robustness. In addition to these advanced packaging technologies, this power module utilizes a direct-cooled pin-fin baseplate resulting in reduced thermal resistance and press-fit electrical pins enabling simpler module assembly into traction inverter systems. Wolfspeed's YM3 power module is available in various voltage and current rating up to 1200 V / 690 A and is qualified to the automotive power module standard, AQG-324.

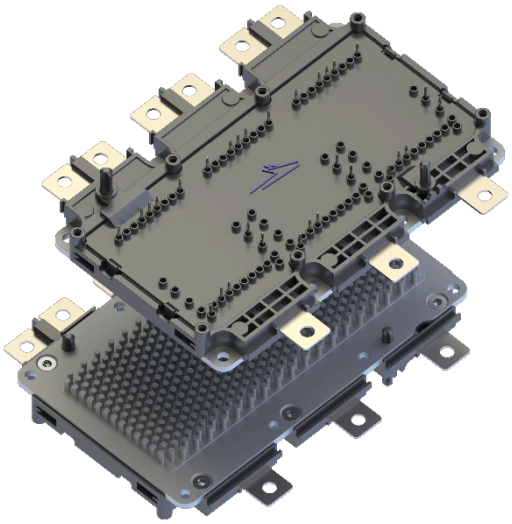

Figure 4. YM3 module

2.4 Reference design system benefits

2.4.1 Accelerate time to market

This reference design aims to accelerate, derisk and streamline/simplify customer design by providing system solution collaterals, such as optimized hardware (MCU control board and gate driver control board), complete software offer (production system RTD and application demo SW), and extensive documentation, such as systemwide application note, SW application note, and system functional safety documentation.

2.4.2 Extending vehicle range

Tested according to the WLTP standard, this solution offers valuable performance indicators that developers can use for comparison and reference. Higher efficiency is achievable using NXP optimized GD3162 for SiC and S32K39 MCU capability with low latency control loop.

GD3162 dynamic gate strength function allows more than 1 % efficiency gain in certain areas of the efficiency map.

2.4.3 Designing with safety

The extensive safety documentation includes an ASIL D in-context safety application that uses the extensive NXP know-how and all safety capabilities provided by the HW and SW components. All guidelines are not implemented on the reference design itself, as the main focus is the performance.

2.4.4 Reducing costs

Thanks to systemwide features integration, such as DC Link discharge, several analog optimizations, and an extensive SW offering that include an ASIL D and production-intent software resolver, our portfolio allows cost saving at system level.

2.4.5 Ease predictive system maintenance

The need to ensure performance across the lifetime of a product is becoming more critical. This product endurance could be achieved thanks to the NXP gate driver. This gate driver supports power device health

monitoring (Vgs_th and RdsON monitoring) [5] and the MCU core that can be used to run a simulation model for analysis.

2.4.6 Addressing future trends

Anticipating future trends, such as dual inverter use, a 6-phase motor, and zonal architecture is critical. These trends can be handled by the S32K39 MCU internal 2x motor control coprocessor and CoolFlux DSP, which run independently from the MCU core. Also, TSN Ethernet for network communication is supported by this MCU.

2.5 Reference design validation

With our partner Wolfpseed, NXP used their HIL inverter laboratory to validate the reference design performance. Due to the programmable motor emulation features, the proper operation of the inverter was verified over the complete functional range of torque and speed, in 1st and 4th quadrants, for various motor models. The motor algorithms were tuned for each model, and both electrical and thermal performance were measured.

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Figure 5. HIL Testing @ Wolfspeed Lab

Advanced features of the inverter, such as dynamic gate strength, were also validated using a power analyzer. The analysis showed significant system efficiency improvement over the complete operating range, while in various coolant temperatures.

Finally, maximum speed and torque tests were performed, to highlight the capabilities of the reference platform.

2.6 Key reference design performance

Table 1. System platform indicators summary

Parameter	Specifications
Motor	3-phase PMSM[1]
Peak power	> 300 kW
Top speed	>12,000 RPM
Rated torque	600 nm
DC link battery	800 V
Peak current	525 amps
Peak efficiency	>99.3 %

Table 1. System platform indicators summary*...continued*

Parameter	Specifications
Power density	50.4 kW/L
Efficiency gain due to dynamic gate strength	~1 %
Semiconductor material	SiC
Number of phases	3
Switching frequency	40 kHz[2]
VDS breakdown voltage	1200 V
VGS threshold voltage	1.8 V to 3.6 V
Low RDSon	2.1 mΩ
VDC capacitor capacity	240 µF
VDC capacitor max voltage	1200 V

[1] HIL testing based on Vepco Linear Motor
[2] Reference SW uses 10 kHz. But the system is capable of over 40 kHz

Performance values mentioned in Table 1 are not production guaranteed. There are many parameters that affect performance, such as the type of power module used, type of motor used, etc.

2.7 Dynamic gate strength

2.7.1 Algorithm example

The GD3162 offers an adjustable dynamic gate strength drive via two methods:

- Programmable interface over SPI
- Using dedicated control pins (GSENH/L) on the low-voltage side

The function and associated implementation recommendations are described in the GD3162 data sheet [1] and Dynamic Gate Strength application note [4]. In this section, an example of an implementation algorithm is described.

Adapt this example to your own system requirements, such as DC link voltage, type of power module, and temperature variation. The most critical parameter is the selection of turn ON and OFF gate resistor for each gate strength selection. Depending on the power module and WLTP profile, these resistors can be optimized to reduce switching losses at specific operating points, while preventing excessive Vds overvoltages.

Gate strength change is based on instantaneous phase setpoint current compared to a threshold Current_th (400A in Figure 6). For a given DC link voltage, a high gate strength setup is used until this threshold, and the switch to a low gate strength setup when crossing this threshold. This gate strength control is therefore separate per phase. This allows fast switching in low current areas (where voltage overshoot is low and WLTP time is significant), while switching slower at high currents, to protect the power module.

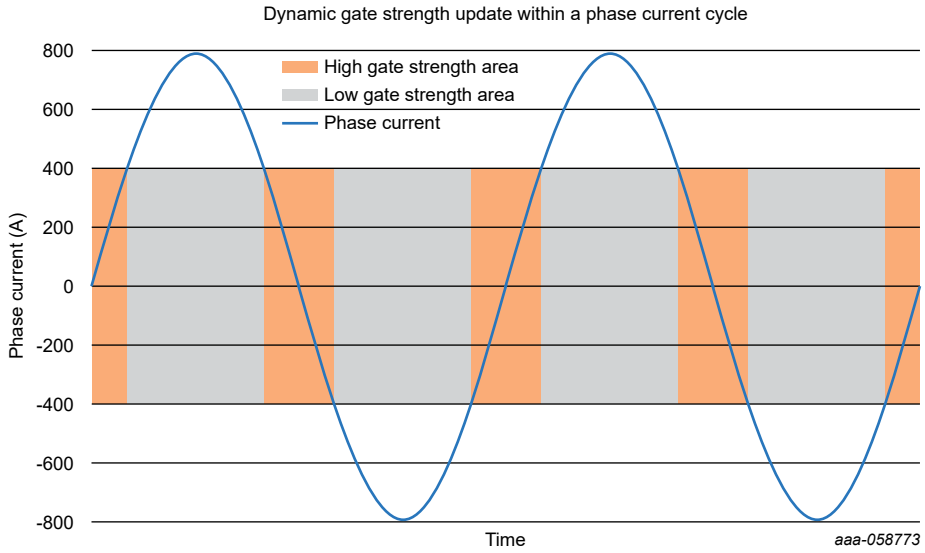


Figure 6. Gate strength strategy by phase for a given DC Link Voltage and temperature

Further optimize the strategy by defining different thresholds based on DC link voltage measurement compared to a threshold DC_Link_th. In this example, only two gate strength selections are used. The GD3162 offers two separate strengths that can be used to accurately adapt the gate drive profile, based on operating conditions.

Table 2 illustrates for a given temperature an example with three different thresholds (400A, 500A, 600A).

Table 2. Gate strength strategy by phase for a given temperature at different DC Link Voltage

DC link voltage (V)	Phase current (A)							
	100	200	300	400	500	600	700	800
950	High	High	High	High	Low	Low	Low	Low
925	High	High	High	High	Low	Low	Low	Low
900	High	High	High	High	Low	Low	Low	Low
875	High	High	High	High	Low	Low	Low	Low
850	High	High	High	High	High	Low	Low	Low
825	High	High	High	High	High	Low	Low	Low
800	High	High	High	High	High	Low	Low	Low
775	High	High	High	High	High	Low	Low	Low
750	High	High	High	High	High	Low	Low	Low
725	High	High	High	High	High	High	Low	Low
700	High	High	High	High	High	High	Low	Low
675	High	High	High	High	High	High	Low	Low
650	High	High	High	High	High	High	Low	Low

The strategy could also consider the module temperature, which influences the authorized overshoot on the power module Vds, if such data is provided by the module manufacturer.

To avoid some high frequency toggling of the gate strength control, reference signals used for the current, DC link voltage, and temperature measure should be exempt of noise. Some dedicated hardware or software strategy should be considered.

2.7.2 SW example

The following fragment of code is responsible for selection and implementation of dynamic gate strength functionality. Gate strength can be controlled manually by using the FreeMASTER tool or it can be automatically adjusted by execution of the following lines:

Dynamic gate strength is changed based on tunable thresholds from Udc bus and currents. By default, the value for gate strength is Slow. It can be changed dynamically based on the following description:

Note: *The Slow name corresponds to the Low gate strength setup and the Fast name to the High set up.*

The following is example code for dynamic gate strength strategy implementation.

```
//phase U
if (MLIB_Abs_FLT(M2.iAbcFbck.fltArg1)>=GS_limits.current_th)
{
if (M2.GD3162.U.high.SlewRate == SR_FAST)
{
M2.GD3162.U.high.SlewRate = SR_SLOW;
GS_limits.update = 0x1;
}
if 2(M2.GD3162.U.low.SlewRate == SR_FAST)
{
M2.GD3162.U.low.SlewRate = SR_SLOW;
GS_limits.update = 0x1;
}
}
else
{
if (M2.GD3162.U.high.SlewRate == SR_SLOW)
{
M2.GD3162.U.high.SlewRate = SR_FAST;
GS_limits.update = 0x1;
}
if (M2.GD3162.U.low.SlewRate == SR_SLOW)
{
M2.GD3162.U.low.SlewRate = SR_FAST;
GS_limits.update = 0x1;
}
}
//phase V
if (MLIB_Abs_FLT(M2.iAbcFbck.fltArg2)>=GS_limits.current_th)
{
if (M2.GD3162.V.high.SlewRate ==SR_FAST)
{
M2.GD3162.V.high.SlewRate = SR_SLOW;
GS_limits.update = 0x1;
}
if (M2.GD3162.V.low.SlewRate == SR_FAST)
{
M2.GD3162.V.low.SlewRate = SR_SLOW;
GS_limits.update = 0x1;
}
}
else
{
if (M2.GD3162.V.high.SlewRate == SR_SLOW)
{
M2.GD3162.V.high.SlewRate = SR_FAST;
GS_limits.update = 0x1;
```

```
}
if (M2.GD3162.V.low.SlewRate == SR_SLOW)
{
M2.GD3162.V.low.SlewRate = SR_FAST;
GS_limits.update = 0x1;
}
}
//phase W
if (MLIB_Abs_FLT(M2.iAbcFbck.fltArg3)>=GS_limits.current_th)
{
if (M2.GD3162.W.high.SlewRate ==SR_FAST)
{
M2.GD3162.W.high.SlewRate = SR_SLOW;
GS_limits.update = 0x1;
}
if (M2.GD3162.W.low.SlewRate == SR_FAST)
{
M2.GD3162.W.low.SlewRate = SR_SLOW;
GS_limits.update = 0x1;
}
}
else
{
if (M2.GD3162.W.high.SlewRate == SR_SLOW)
{
M2.GD3162.W.high.SlewRate = SR_FAST;
GS_limits.update = 0x1;
}
if (M2.GD3162.W.low.SlewRate == SR_SLOW)
{
M2.GD3162.W.low.SlewRate = SR_FAST;
GS_limits.update = 0x1;
}
}
}
if (GS_limits.dynamic == 0x0)
{
//update the slewrate
if ((M2.GD3162.U.high.SlewRate != SR_SLOW)||
(M2.GD3162.U.low.SlewRate != SR_SLOW)||
(M2.GD3162.V.high.SlewRate != SR_SLOW)||
(M2.GD3162.V.low.SlewRate != SR_SLOW)||
(M2.GD3162.W.high.SlewRate != SR_SLOW)||
(M2.GD3162.W.low.SlewRate != SR_SLOW))
{
M2.GD3162.U.high.SlewRate = SR_SLOW;
M2.GD3162.U.low.SlewRate = SR_SLOW;
M2.GD3162.V.high.SlewRate = SR_SLOW;
M2.GD3162.V.low.SlewRate = SR_SLOW;
M2.GD3162.W.high.SlewRate = SR_SLOW;
M2.GD3162.W.low.SlewRate = SR_SLOW;
GS_limits.update = 0x1;
}
}
```

2.7.3 Performance example

Figure 7 illustrates the EV traction inverter Gen3 reference design module at ambient temperature in the low-speed section.

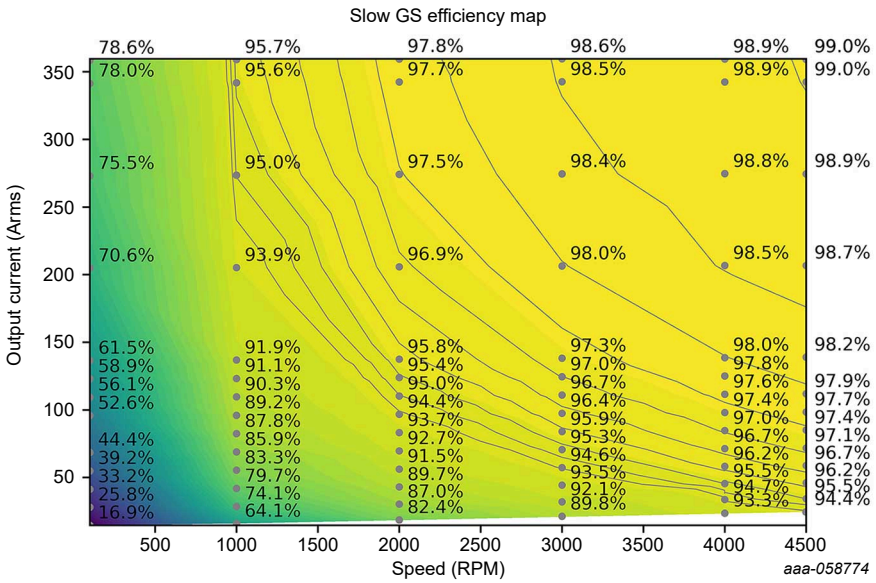


Figure 7. Efficiency map in Slow Gate Strength condition

A second set of measurements with the same HW setup has been created with a gate strength change based on Current_th = 200 A. Below this threshold, the high gate strength setup was applied, when above this threshold the same gate strength that is on Table 2 was applied (slow/low GS).

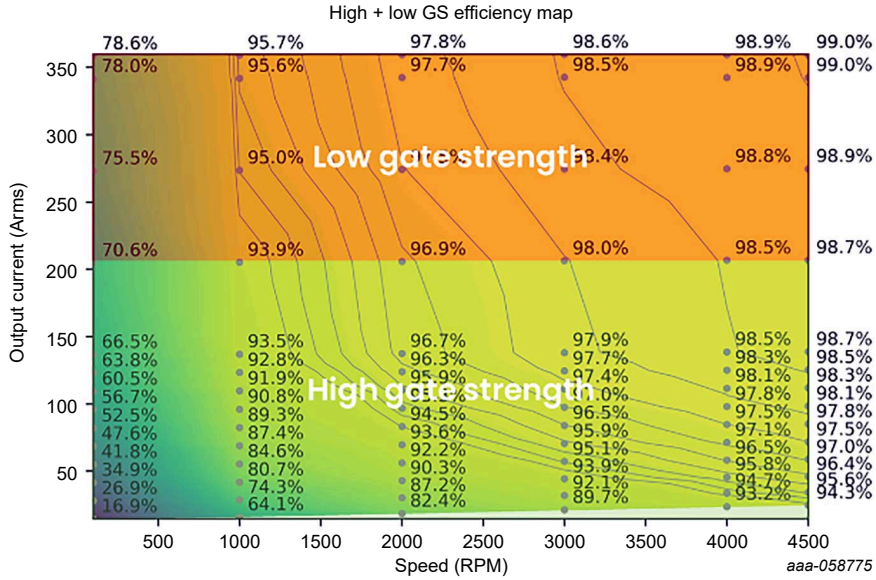


Figure 8. Efficiency map with Dynamic Gate Strength strategy

Figure 9 is a delta between the two previous efficiency maps to illustrate the improvement due to the dynamic gate strength strategy. We could observe a benefit of ~1 % of the efficiency. As explained in the previous section, the strategy could be further optimized.

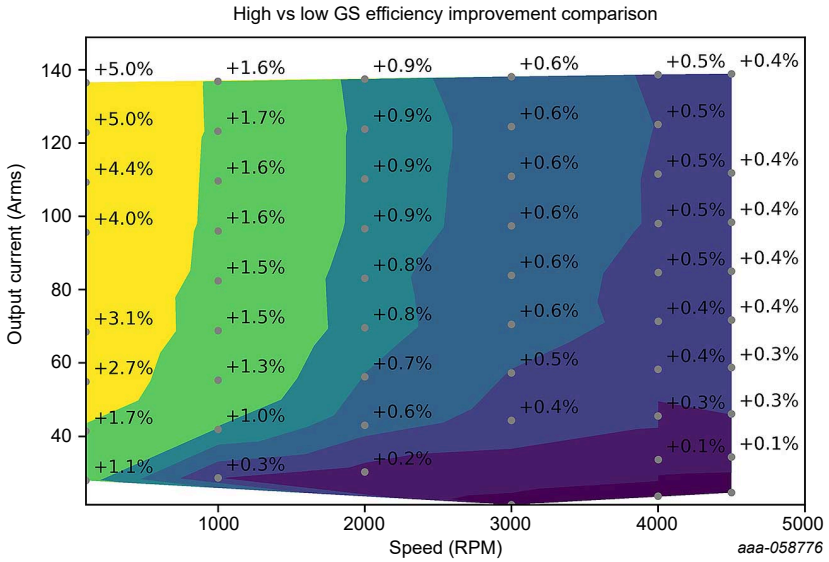


Figure 9. Efficiency map comparison between both strategies

2.8 ASIL D SW resolver

The system implements a software interface to the resolver. The resolver software is executed on a dedicated timer core (eTPU) so that the main cores can be focused on higher-level tasks. Using a software-based resolver external hardware interface between the motor resolver and MCU ADCs is not needed because the processing is done in software within the MCU using eTPU.

In addition, there is an RDC checker function that is executed on the lockstep core. The RDC checker is designed to enhance the safety and reliability of motor control. It is engineered to interface seamlessly with the SW resolver executing on the eTPU, which provides critical information regarding motor shaft position and rotation. The signal from the SW resolver is fed into the RDC checker as input data to check for faults and errors.

If the input data are found to be incorrect, or they are out of the configured thresholds. The RDC checker promptly triggers a fault to prevent potential failures. This proactive approach ensures that any discrepancies in motor shaft position and rotation are identified and addressed, thereby contributing to the overall safety of the system reaching up to ASIL D.

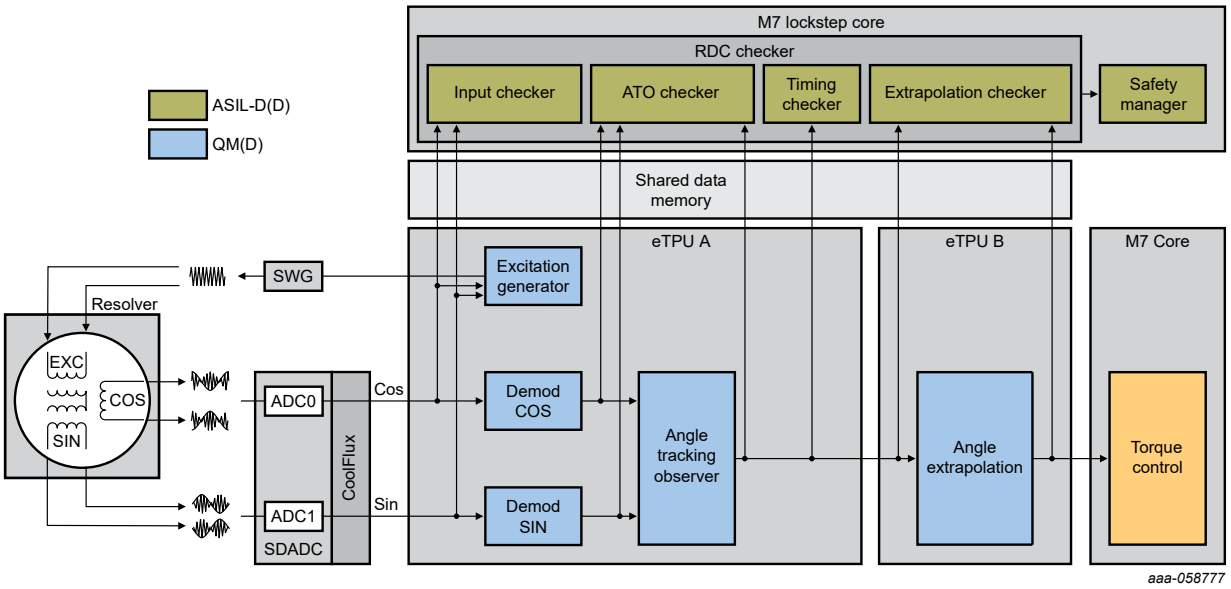


Figure 10. SW resolver block diagram

2.9 DC Link Discharge

Safe handling of the high-voltage DC link capacitor in an automotive inverter is critical. This capacitor usually requires external discharge circuitry. The GD3162 Advanced IGBT/SiC Driver offers several functionalities to help with this process, while minimizing external component cost. Moreover, this driver includes unique power-device monitoring capabilities to provide system designers information about the aging of the semiconductor.

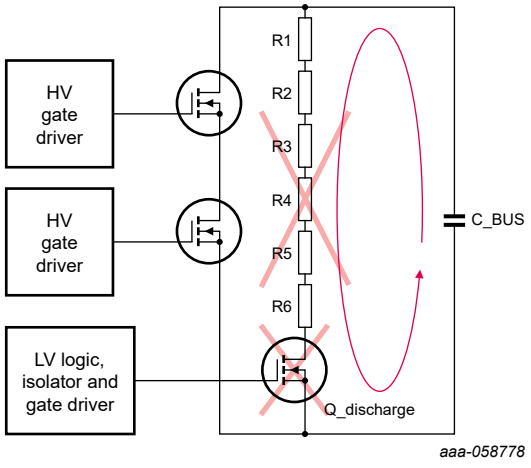


Figure 11. Illustration of components saving with GD3162

A dedicated application note[2] guides you through design aspects related to the DC link discharge of the GD3162 and Vth measurement functionalities. This provides the end user with the knowledge to use and get the most out of the GD3162 application.

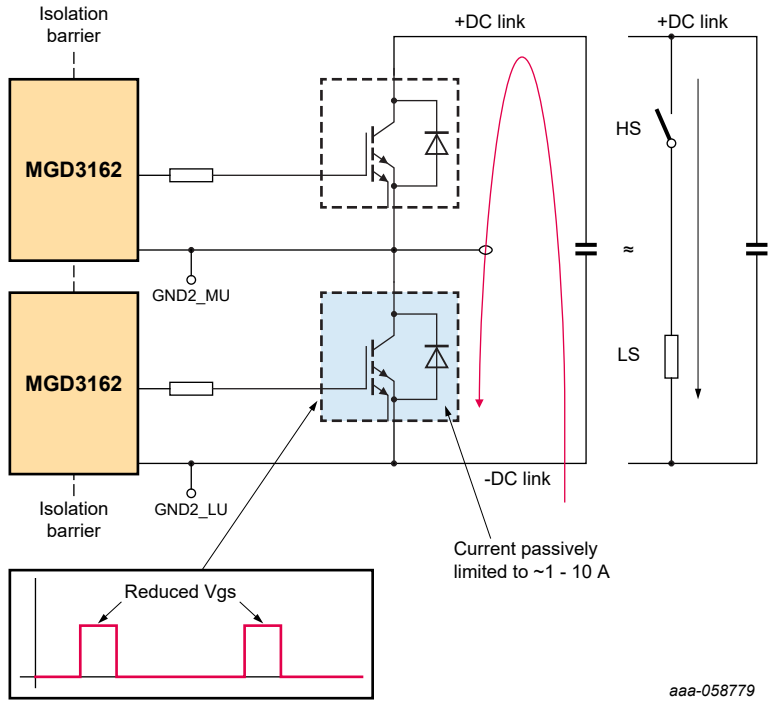


Figure 12. Illustration of DC Link discharge principle with GD3162

This application note provides some guidelines in terms of implementation, including some safety recommendations.

Some software sequences are available either for the Vth measurement, required at initialization and to run the DC link Discharge. Refer to the dedicated application note for further details [3].

The following code is the SW sequence example for Vth measurement.

```
        SPI Write MODE2 (0x01) with CONFIG_EN = 1
        SPI Write DISCHG (0x17) with TL = 1
        SPI Write MODE2 (0x01) with CONFIG_EN = 0
       ...
        Wait 5.82 ms and/or
        If SPI Read DISCHG (0x17) MC = 1 then Threshold-level mode is complete.
        Then
        SPI Read REQADC (0x13) with AMUX_SEL = 0x0F. Returns the TLVA value.
        SPI Write DISCHG (0x17) with TL = 0 and MC = 0. Exits the Threshold-
level mode
```

The following code is the SW sequence example to run DC link discharge.

```
        SPI Write MODE2 (0x01) with CONFIG_EN = 1
        SPI Write DISCHG (0x17) with TL = 1, BM = 1 and
        TLV = 0b1111 for auto mode or
        TLV = "selected value" to skip Threshold-level mode.
        SPI Write MODE2 (0x01) with CONFIG_EN = 0
        Start 5.82 ms timer from rising edge of CSB
       ...
        At timer expiration set opposite PWM HIGH (+3 ms margin)
       ...
```

```
        SPI Read DISCHG (0x17): If MC =1 then discharge is complete.
       ...
        SPI Write DISCHG (0x17) with TL = 0, BM = 0 and MC = 0 to exit this
mode.
```

3 Reference design offering

3.1 Package overview

EV traction reference design Gen3 is composed of five types of deliverables:

- Optimized hardware deliverables without power modules
- Software deliverables
- Extended system functional safety documentation
- Extended system documentation, such as a system application note [9], user manual, and SW application note [3]
- Partner ecosystem

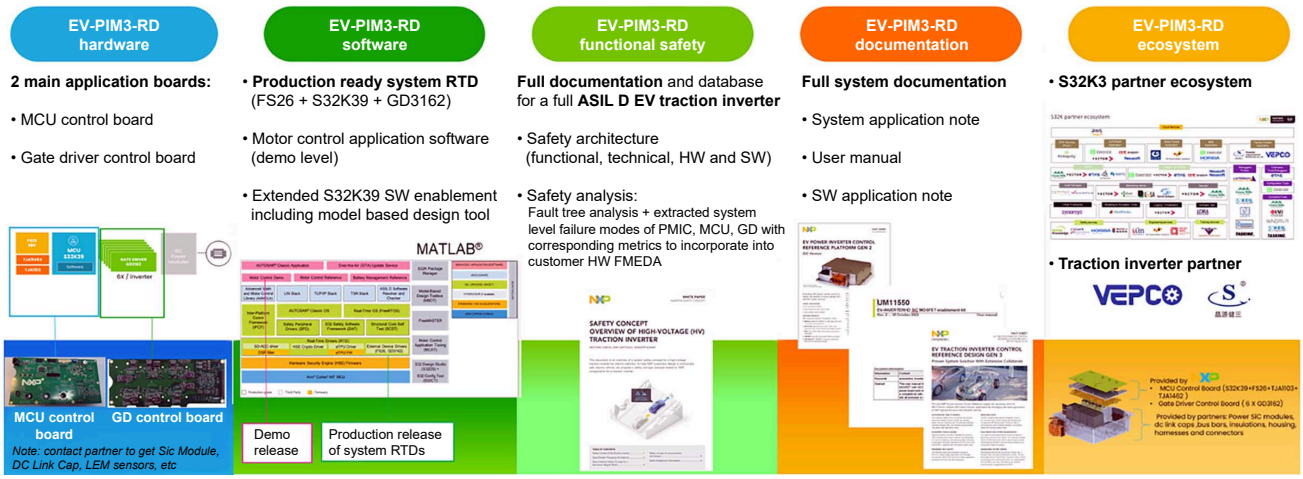


Figure 13. EV traction inverter Gen3 ref design collaterals

Different collaterals are articulated around two different packages, with a main difference around the system functional safety deliverables.

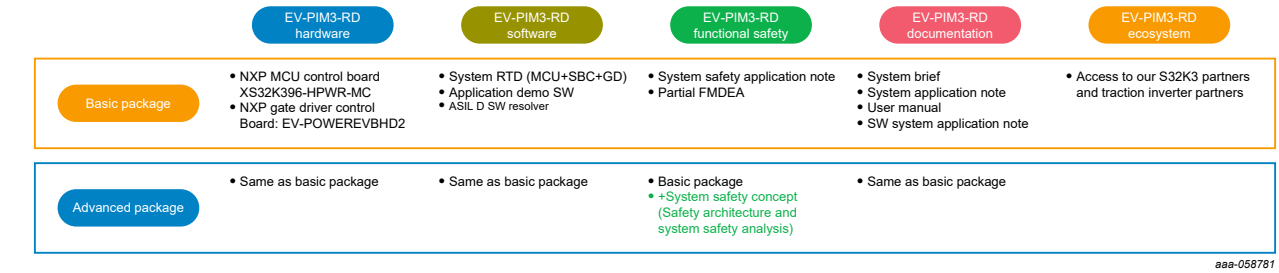


Figure 14. EV traction inverter ref design package offer

3.2 EV traction inverter hardware

3.2.1 Applications boards

Two optimized boards in terms of form and factor, layout, and BOM, according to NXP recommendations, are part of the reference design.

An NXP MCU control board (ref: XS32K396-HPWR-MC) includes the S32K39 MCU with its associated FS26 safety SBC and two options of communications with TJA146X CAN physical layer and TJA1103 Ethernet physical layer.

A second board, NXP gate driver control board (ref: EV-POWEREVBHD2) includes the six GD3162 high-voltage isolated gate drivers. This board is compatible with the newer HybridPACK Power modules such as:

- Infineon - FS05MR12A6MA1B (1200 V, 200 A)
- Infineon - FS03MR12A6MA1B (1200 V, 400 A)
- Starpower - MD816HTC120P6HE (1200 V, 816 A)
- Starpower - MD600HTC120P6HE (1200 V, 600 A)
- Wolfspeed – ECB4R3M12YM3 (1200 V, 440 A)[2]
- Wolfspeed – ECB2R8M12YM3 (1200 V, 560 A)[3]
- Wolfspeed – ECB2R1M12YM3 (1200 V, 690 A)[4]

Note: *Wolfspeed YM3 modules to be launched in Q1-25

All schematics, BOM information, and layout are provided with each board.

Refer to the user manual for the assembly procedure and how to use it.

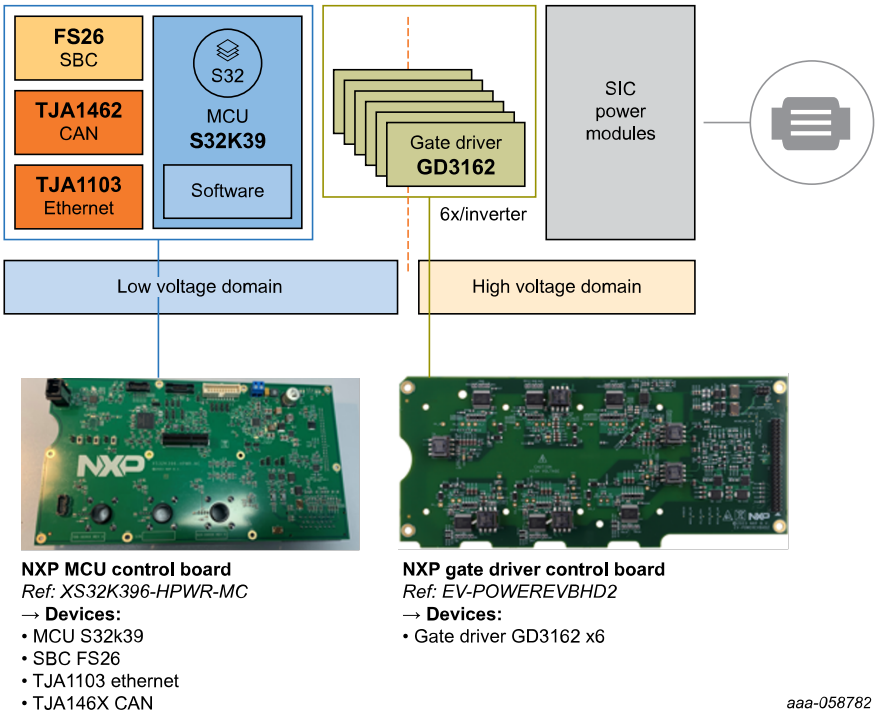


Figure 15. NXP MCU and GD Control Boards

2 Wolfspeed YM3 modules to be launched in Q1-25
3 Wolfspeed YM3 modules to be launched in Q1-25
4 Wolfspeed YM3 modules to be launched in Q1-25

3.2.2 Complete module solution

In collaboration with our partners, such as Vepco, a complete module solution including the following are available for purchase.

- Power Sic modules
- DC link caps
- Busbars
- Insulators
- Cooling housing
- Harnesses
- Connectors

This design provides a quick prototyping and system evaluation.

This is not intended to be a turnkey or production solution.

Contact your sales representative for further information.

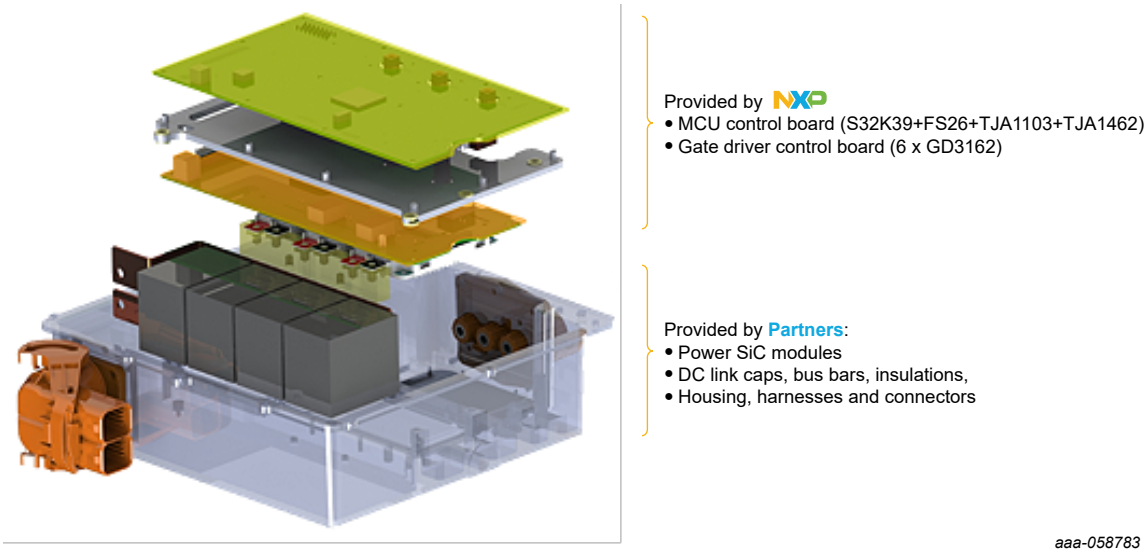


Figure 16. Example of ECU anatomy

3.3 EV traction inverter system software

3.3.1 Introduction

To support EV traction inverter reference design enablement, a production system RTD and a motor control demo SW are part of the system offering.

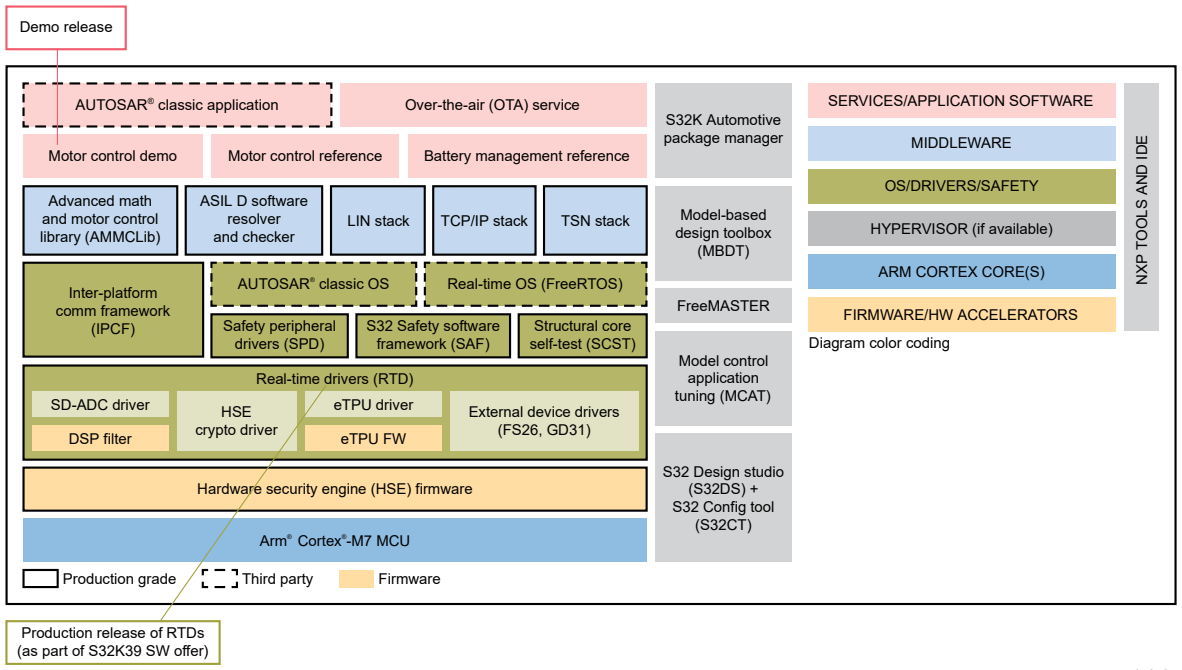


Figure 17. EV traction inverter reference design SW offer

3.3.2 System software real-time drivers

The system uses the S32K3 real-time drivers (RTD) covering the MCU features and the eTPU. The system also uses RTDs for the external SBC/PMIC (FS26) and high-voltage gate driver (GD3162). The RTD drivers are available on the NXP website. RTD is offered at no additional charge and is developed to be safety-compliant up to ASIL D. The RTD package offers a dedicated safety package that includes the RTD safety concept and FMEA reports.

3.3.3 Motor control application SW

On the top of this system RTD, a motor control demo SW based on bare metal and including the previously mentioned system RTD is provided. This demo SW is focused on the performance aspect of the system. Some system functions such as HVIL diagnosis and system active discharge are not implemented in the SW.

Table 3 is a nonexhaustive list of included functions with the associated maturity level for each.

Table 3. Figure x Motor Control SW Application Functions

Maturity Level	Inverter Functions	
Production level	Motor control FOC	Mathematical transformation, Clark, Park: inverse Park, Inverse Clarke
Demo level	Resolver	Resolver offset calibration, resolver analog signal plausibility, resolver analog signal
	Motor control FOC	Maximum torque per ampere (code implementation example), field weakening, regeneration control, SVPWM
	Efficiency optimization	Dynamic gate strength algorithm
	Inverter algorithm	Motor torque estimate (code implementation example)
		Module temp, GD temp
	Application control	Inverter system state manager

Table 3. Figure x Motor Control SW Application Functions...*continued*

Maturity Level	Inverter Functions	
		Thermal threshold monitor
		Discharge (code implementation example)
		Rotor, angle, speed calculator
		Active short circuit
		Freewheeling
	System diagnosis	3 Phases current (overcurrent, sum not zero)
		Over/under voltage
		Over stator Temp
	Input signal processing	Stator current sensor
		DC link voltage sensor
		Resolver analog signal

Note: *Refer to S32K2 SW Business Model Support and Maintenance for Standard and PREMIUM SW option (Custom security firmware, safety SW, etc.).*

3.3.4 S32K39 SW enablement

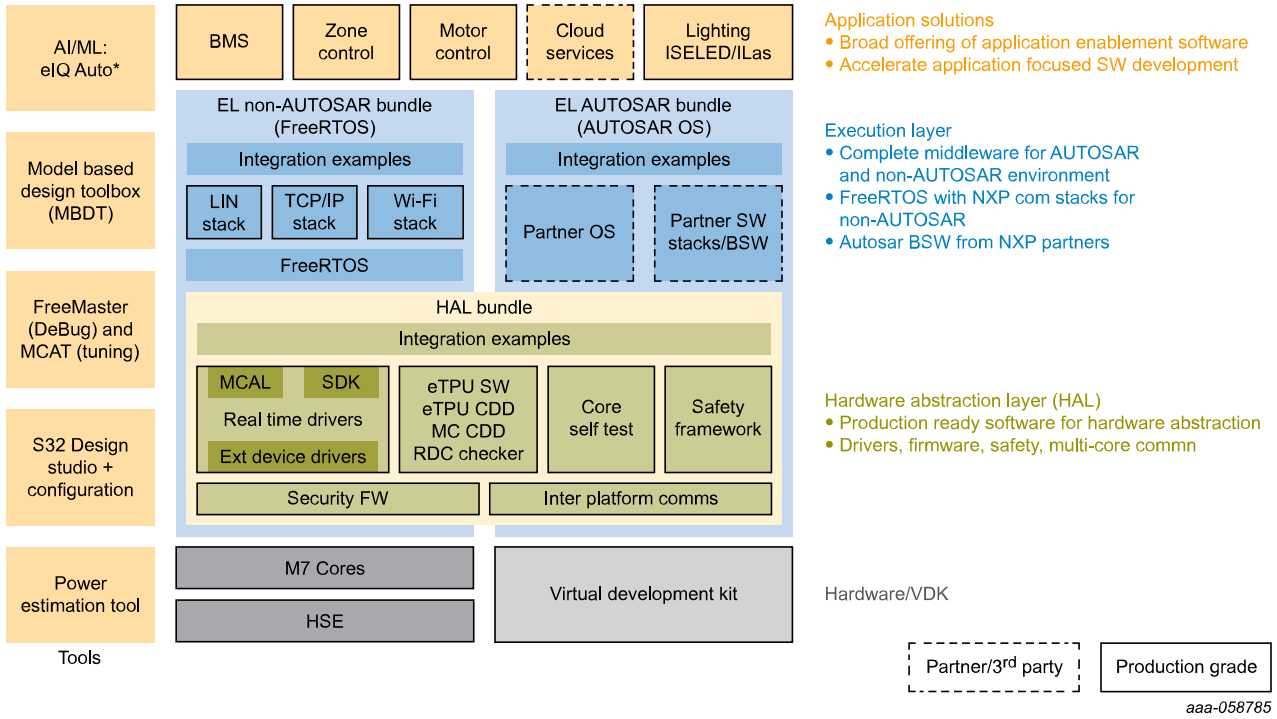
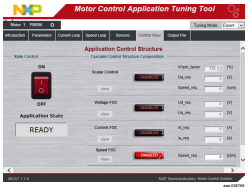
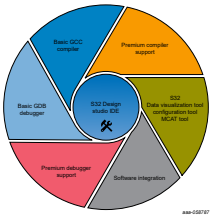
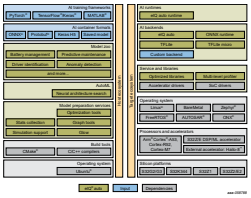


Figure 18. Software overview

Table 4. Tools relevant for inverter motor control

Tools	Design Phase	Description and Link
MATLAB®	Design	S32 Model-Based Design Tool
	Tuning and optimization	Existing MCAT Solution With Motor Control Bare Metal Reference Application
	Development and debug	S32 Design Studio S32 Compilers (eTPU/GCC) S32 Configuration Tools Trust center Secure Debug authentication Framework
	EIQ Auto machine learning (ML) toolkit	Software Development Environment

3.4 System FuSa package

On the top of the ASIL D SW resolver, extended documentation is available at device and system level. This documentation is spread across two different packages: the basic package and the advanced package.

3.4.1 System FuSa package offering

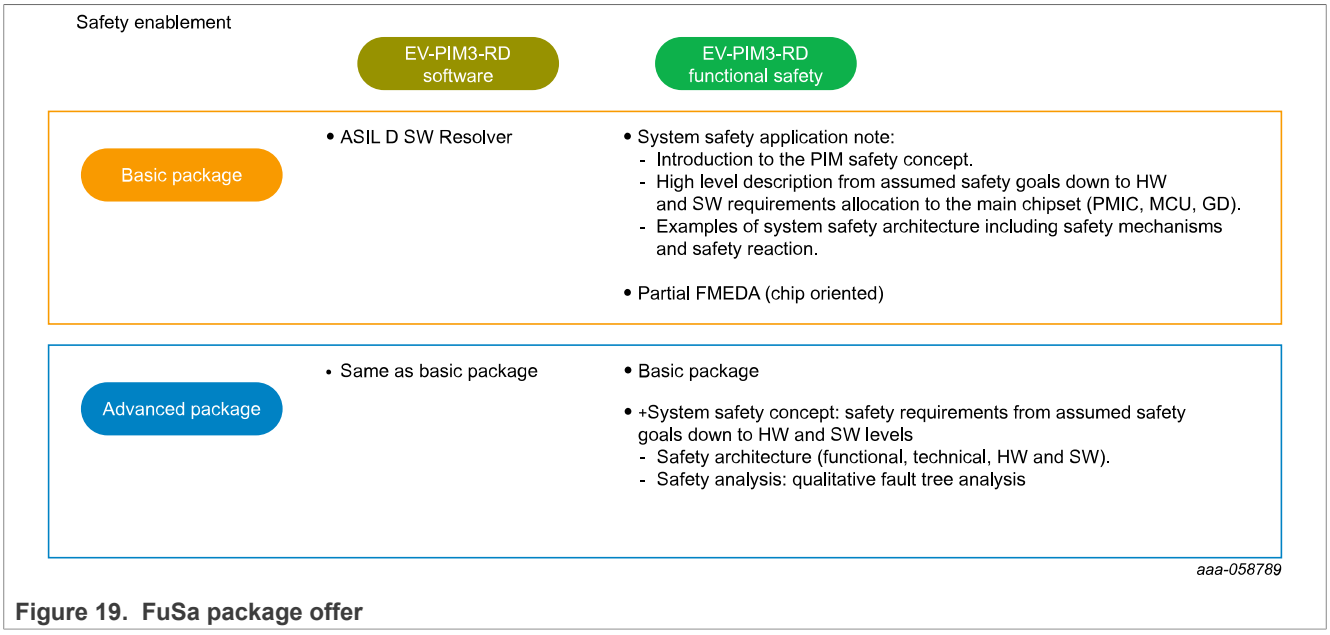


Figure 19. FuSa package offer

3.4.2 System FuSa document

Partial FMEDA (chip oriented) is available for the three main components of the system: S32K39 MCU, FS26 SBC, and GD3162 high-voltage gate driver.

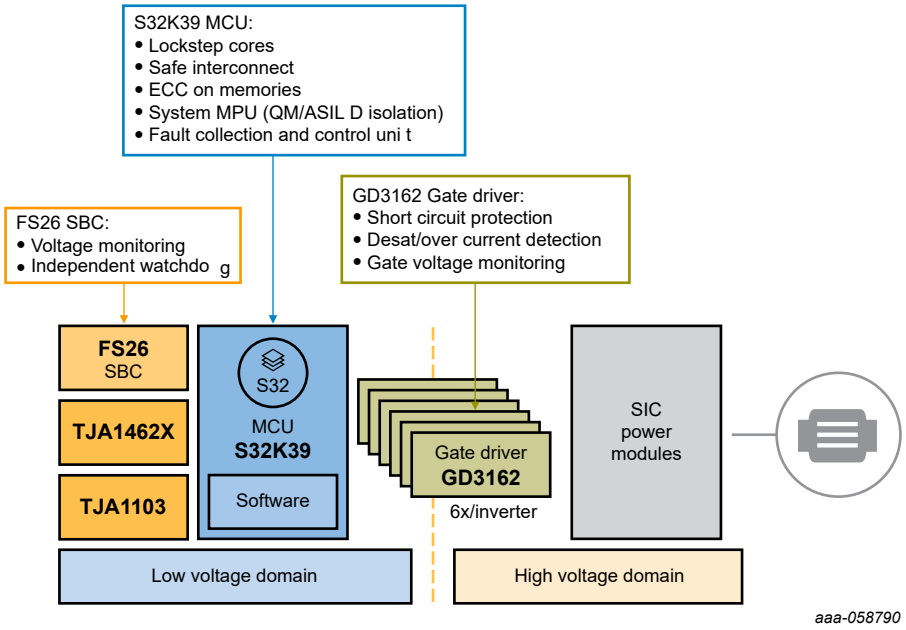


Figure 20. Safety functions overview

In the basic package, the AN14552 application note introduces the EV Traction inverter Safety concept. It consists of a high-level description from assumed safety goals down to HW and SW requirements' allocation to the main chipset (PMIC, MCU, GD). Some examples of system safety architecture including safety mechanisms and safety reaction are also included.

In the advanced package, the safety concept is more complete. The safety architecture (functional, technical, HW, and SW) covers the three assumed safety goals.

A safety analysis completes the package. This analysis includes a qualitative system fault tree analysis and extracted system modes.

3.5 Extensive documentation

On the top of this application note and all System FuSa document, a user manual and a SW application note complete the documentation. Refer to Section 6 for a document list.

4 Devices overview

4.1 Introduction

The purpose of this section is to provide an overview (features and benefits) of the devices used in this system. Further information is available in the dedicated datasheet of each device.

4.2 S32K396 MCU

4.2.1 Key features

- High performance member of the S32K3 family
- Three Arm® Cortex® -M7 cores at 320 MHz (one lockstep and two split-locks)
- CoolFlux DSP® at 160 MHz (digital filters and machine learning)
- Two motor control coprocessors at 320 MHz

4.2.2 Customer benefits

- Designed for safe, EV control applications
  - Motor control (3- or 6-phase motor, Si IGBT/SiC/GaN transistors)
  - Power conversion (DC/DC, OBC)
  - Battery management system (BMS) control
  - Vehicle control unit (VCU) or domain control
- Supports dual motor control loops over 200 kHz
- High-resolution PWM outputs (195 ps resolution)
- Safe, ASIL D software resolver with integrated analog to reduce BOM cost
- Hardware security engine (HSE) for secure boot, security services, secure OTA updates, and key management
- Comprehensive set of software support and tools (library, model-based design, reference software)

4.2.3 Block diagram

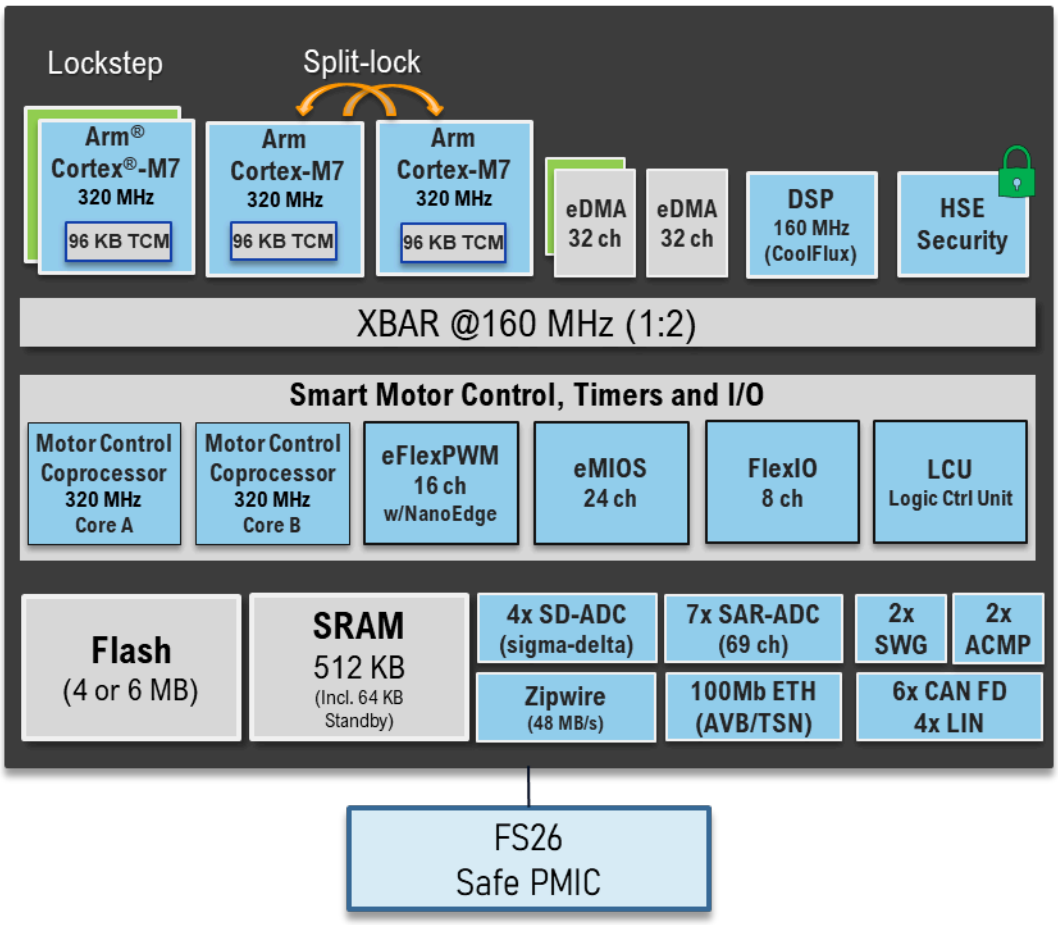


Figure 21. S32K39 block diagram

4.3 FS26 SBC

4.3.1 Key features

- 10 W system power management for 12 V systems (40 V max rating)
- Configurable power management with seven rails (one boost, two DCDCs, two LDOs, and up to two trackers)
- Highly efficient synchronous rectification DCDC with 0.8 A/1.65 A core supply
- Front and back boost to cover LV124 and/or EV use cases (18 V supply)
- High precision voltage reference (30 mA, ±0.75 %)
- 30 µA low quiescent current, in Low Power ON or OFF, with DCDC in PFM
- Third generation safety architecture, fail safe and fail silent robust and proven
- Fit for ASIL B and ASIL D architecture with unique ABIST on demand
- Automotive qualified AEC Q100 Grade 1 extended mission profile for EV

4.3.2 Customer benefits

- Scalable power, safety, and system family concept (pay for what you need)
- Configurable: power all safety MCUs with Icore <1.65 A (40/55 nm)

- Industry proven: designed at main OEMs in ASIL B/D EV and SDV Systems
- Robustness: support enhanced mission profiles for EV systems
- Optimal system integration (long-duration timer, FCCU/SMU monitor, FS0b and FS1b, AMUX)
- Simplify design experience: complete eco system including:
  - HW schematics EMC proven
  - SW drivers AUTOSAR ISO26262
  - Safety documentation, safety application with S32K3 family
  - Thermal/electrical model/FMEDA calculation tools
  - Application note to power S32K3x, TC3x IFX, RH850 RNS

4.3.3 Block diagram

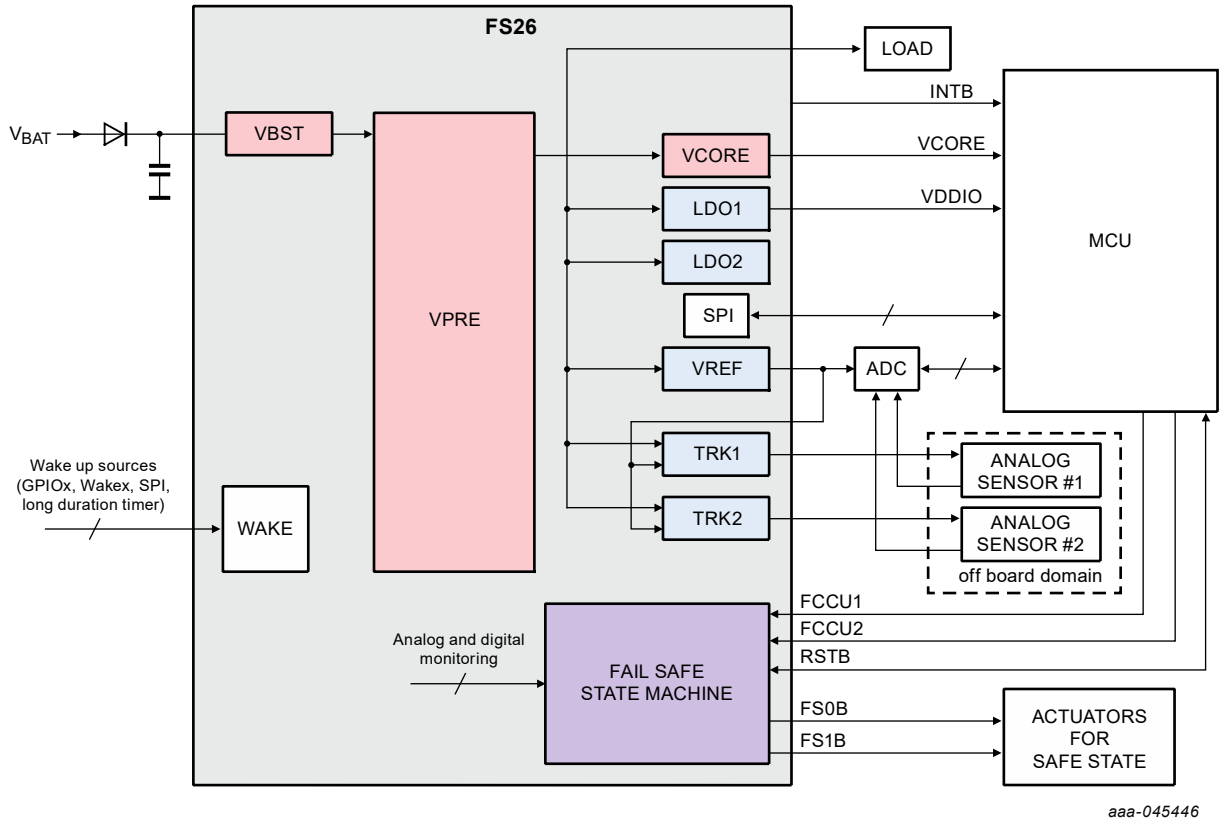


Figure 22. FS26 Block Diagram

4.4 GD3162 HV gate driver

4.4.1 Key features

- Supports IGBT and SiC power switches
- Dynamic gate strength control
- Integrated power switch diagnostics (R_{DSON} and V_T)
- DC Link discharge control
- Integrated LDO
- Segmented drive
- <1 µs SC, OCP, UV, temperature sense, integrated ADC with programmable sampling delay

- ADC with programmable sampling delay
- Real-time reporting
- Integrated features to support ASIL C/D

4.4.2 Customer benefits

- Flexibility and performance
- Higher vehicle range enabled
- Improved efficiency for both 400 V and 800 V systems by reducing switching losses for turn ON and turn OFF
- Inverter + e-Motor system predictive reliability and health monitoring
- System BOM cost and size reduction
- Safety and monitoring
- AEC-Q100, ISO26262 compliant product development with comprehensive suite of safety analysis and documents
- System support: evaluation board/technical support tools customized to support power device/modules footprints from more than eight vendors

4.4.3 Block diagram

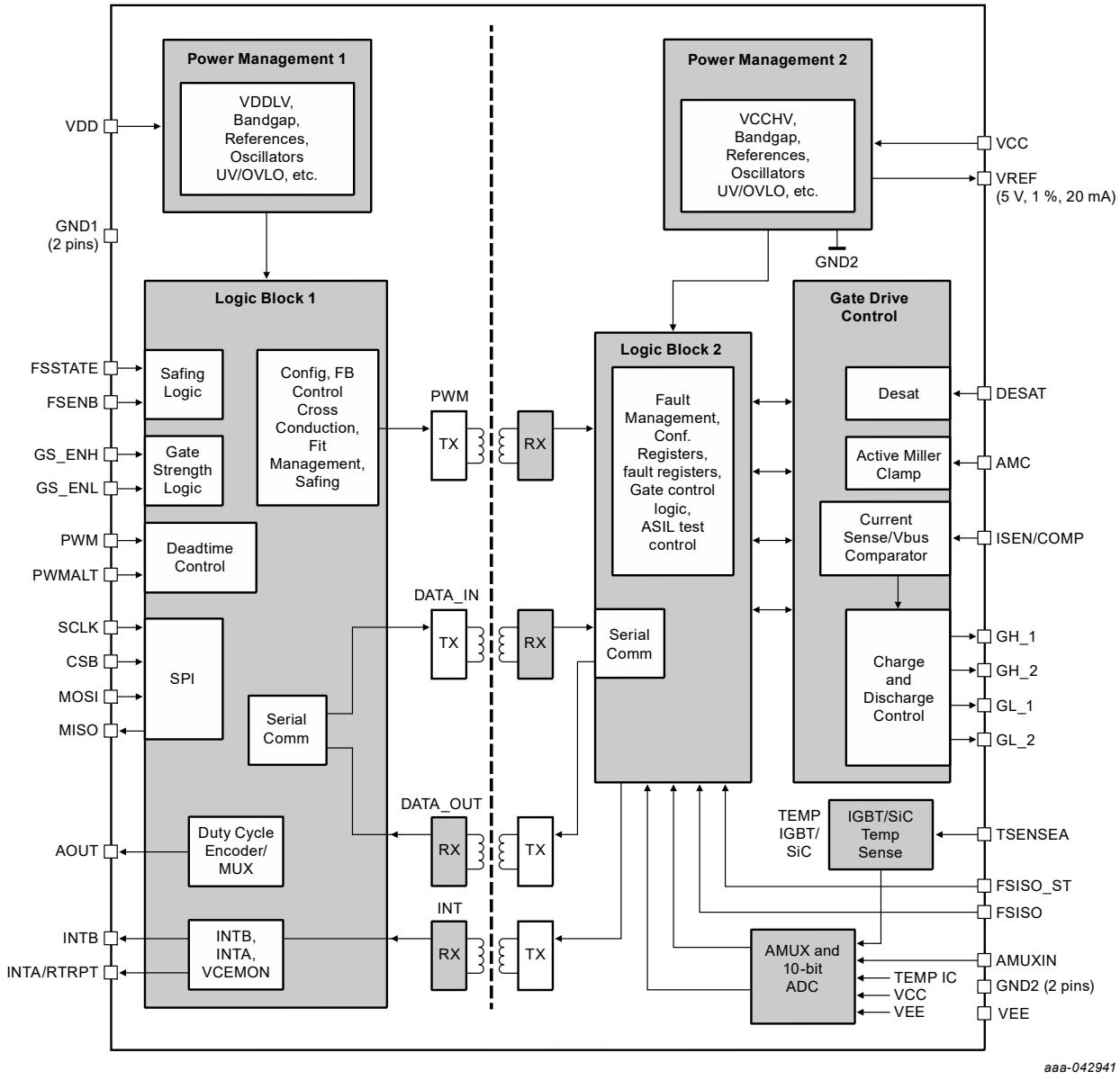


Figure 23. GD3162 Block Diagram

4.5 TJA1462 CAN

4.5.1 Key features

- CAN transceiver with Normal and Standby modes
- Compliant to new ISO 11898-2:2024, parameter set A-C
- VIO pin for interfacing with 3V3 and 5 V supplied MCUs
- Operating voltage: 4.5 V to 5.5 V (± 10 %)
- Automotive AEC Q100 Grade-1 and Grade-0 qualified (up to T_{amb}=150 ºC)
- Wake-up Pattern Filter Time = 0.5 µs to 1.8 µs

- True CAN data rate support up to 8 Mbit/s
- Hardware and software compatible with 8-pin CAN FD standby transceivers
- Available in SO8 and HVSON8 package

4.5.2 Customer benefits

- Implements CAN signal improvement capability as defined in ISO 11898-2:2024 parameter set C to significantly reduce signal ringing effects in a network
- Tighter bit timing symmetry performance allowing more time to reduce signal ringing
- CAN wake-up receiver powered by VIO allowing VCC to be shut down (TJA1462A)

4.5.3 Block diagram

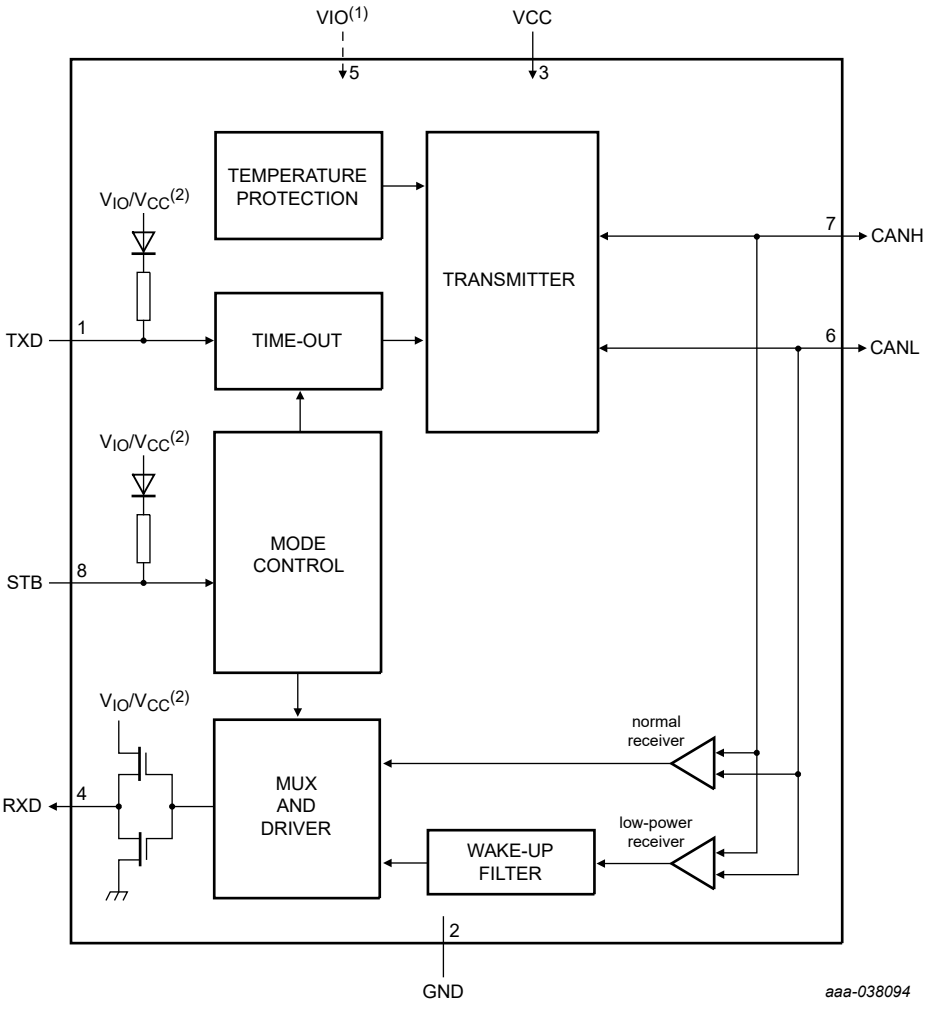


Figure 24. TJA1462 block diagram

4.6 TJA1103 Ethernet phy

4.6.1 Key features

- MII, RMII, RGMII (Variant A), SGMII (Variant B)

- 36-pin, 6 mm x 6 mm HVQFN, wettable flanks
- AEC-Q100 Grade 1
- Tamb = –40 °C to +125 °C (Tj = –40 to +150 °C)
- TJA1103: ~85 mW (typ)
- <0.05 DPPM
- Exceptional BLR (10 kcycles)
- Low emission, even with margin
- Supports TC10 sleep/wake-up forwarding
- Full IOPT round-robin tested (100BASE-T1 and TC-10)

Table 5. TJA1103 test results

EMC, Compliance, and IOP test reports	TJA1103
FTZ (IEC62228-5, IEC62228-5 Strip Line)	Passed
Phoenix (SAE2962-3)	Passed
C&S (OPEN:IOPT, TC-10)	Passed
UNH (Compliance)	Passed

4.6.2 Customer benefits

- Drop-in compatible with the 1000 MB PHYs (TJA1120 and TJA1121) and the 100 MB MACsec enabled variant (TJA1104)
- Supports single supply, therefore, reduction in overall BoM cost
- As shown in Table 5, the device is tested against the latest automotive specs (IEC, SAE, IEEE, OA)

4.6.3 Block diagram

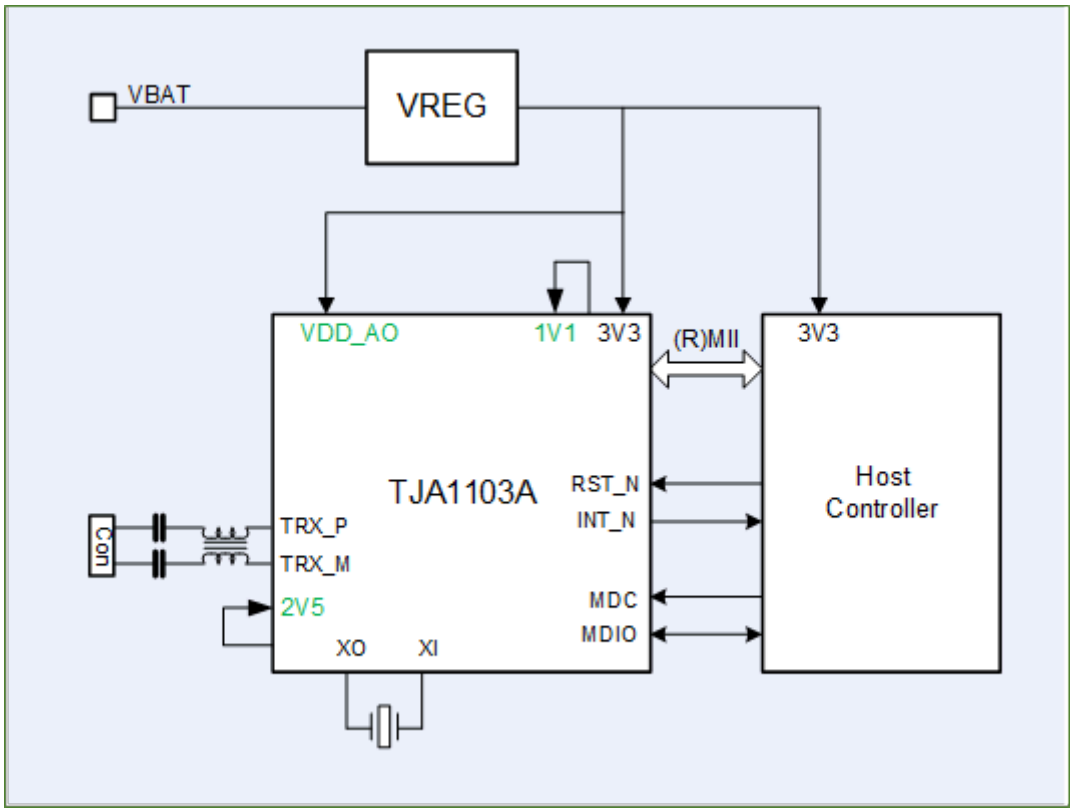


Figure 25. TJA1103 block diagram

5 Acronyms and definitions

Table 6.

Acronyms and terms	Definitions
GS	Gate strength
AN	Application note
MBDT	Model based design toolkit

6 References

[1] GD3162 – Advanced IGBT/SiC gate driver with dynamic gate strength adjust data sheet
[2] AN13710 – GD3162 DC link discharge application note
[3] AN14504 – EV Traction Inverter Reference Design Gen 3 SW application note
[4] AN13673 – Dynamic Gate Strength advantages using the GD3162
[5] AN13978 – Configuring the GD3162 for RDSon Monitoring
[6] FS26 – data sheet
[7] TJA146X – data sheet
[8] TJA1103 – data sheet
[9] AN14552 – System FuSa application note
[10] SM_EVTI_GEN3_FTA – EV traction inverter gen3 reference design FTA export
[11] SM_EVTI_GEN3_SCR – EV traction inverter Gen3 system safety concept requirement specification
[12] SM_EVTI_GEN3_HW – EV traction inverter Gen 3 hardware safety architecture and specification
[13] SM_EVTI_GEN3_SW – EV traction inverter gen 3 reference design: safety software architecture
[14] UM12210 – EV Traction Inverter Gen 3 SiC MOSFET Enablement Kit
[15] AN14552 – Safety concept overview of high-voltage EV traction inverter Gen3 reference design

7 Revision history

Table 7. Revision history

Document ID	Release date	Description
AN14505 v.1.0	07 February 2025	• Initial version

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