Freescale Semiconductor
Application Note

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MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines

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1 Introduction

This application note describes the thermal performance of the MSC8102, MSC8122, and MSC8126 under standard thermal test conditions and when mounted as an array of components and provides guidelines for evaluating board layouts using these devices.

Contents

2 Thermal Resistances

Table 1 shows the thermal performance of the MSC8102, MSC8122, and MSC8126 as determined using the JEDEC standards.

Table 1. Thermal Characteristics for MSC8102, MSC8122, and MSC8126

Rating	Symbol	MSC8102		MSC8122 and MSC8126		Unit
		Natural Convection	200 ft/min (1 m/s) Airflow	Natural Convection	200 ft/min (1 m/s) Airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$ or θ_{JA}	27	20	26	21	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$ or θ_{JA}	15	11	19	15	°C/W
Junction-to-board[4]	$R_{\theta JB}$ or θ_{JB}	4.4		9.0		°C/W
Junction-to-case[5]	$R_{\theta JC}$ or θ_{JC}	0.3		0.9		°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal. The board is the single-layer board specified in JESD51-9.
3. Per JESD51-6 with the board horizontal. Board layer count (either 1 signal or 2 signal and 2 planes) is denoted in the table. Board specification is JESD51-9.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

Using this data, an estimation of the chip-junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values can be obtained from the *Technical Data* sheet for the component executing typical codes. There are two junction-to-ambient thermal resistance values in common usage and specified by the JEDEC JESD51 documents:

- Value measured on a single-layer board (26 or 27°C/W in natural convection)
- Value measured on a board with two planes (15 or 19°C/W in natural convection)

Values with air flow are also listed in **Table 1**. The value that is closer to an individual application depends on the power dissipated by other components on the board. The value measured on a single-layer board is appropriate for a tightly packed printed circuit board. The value measured on a board with the internal planes is usually appropriate for a board with low power dissipation (less than 0.02 W/cm^2 for natural convection) and well-separated components. The ambient temperature is the temperature of the air cooling the component in the immediate vicinity of the component at or below the height of the component. Based on the junction temperature estimate computed using this technique and comparison with the maximum allowed junction temperature, you can determine whether a more detailed thermal analysis should be done. Typically, detailed thermal modeling is done

using Computational Fluid Dynamics (CFD) software that can solve for the air flow, heat transfer to the air, and thermal conduction within the component and board. Commercially available CFD software packages include Flotherm[1], IcePak[2], Maya-ESC[3], and many other products. The component models used for thermal modeling are described in the following sections.

2.1 Two-Resistor Model

The two-resistor model is created using the Junction-to-Case Thermal Resistance ($R_{\theta JC}$) and the Junction-to-Board Thermal Resistance ($R_{\theta JB}$). These two thermal resistances are given in **Table 1**. The technique to create the two-resistor model for use in the CFD code is described by Kromann[4] and is being formulated into a JEDEC guideline. A two-block model is created with additional collapsed blocks to represent the resistances as shown in **Figure 1**.

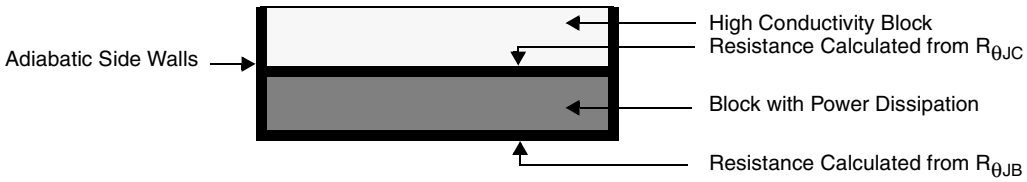
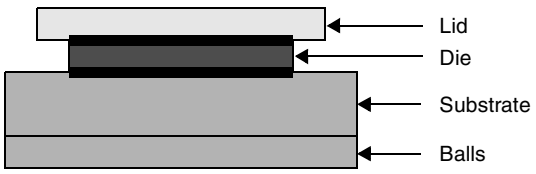


Figure 1. Two-Resistor Model for the Component

The package is placed on the printed circuit board. The two conductive blocks are typically modeled with conductivity of 1000 W/m K. The bottom block, which includes the power dissipation of the component, is modeled as 20 × 20 × 1.66 mm. The top block is modeled as 20 × 20 × 1 mm for a total height of 2.66 mm. A resistive element (collapsed cuboid or plate) is used between the bottom block and the printed circuit board with its resistance calculated from the junction-to-board thermal resistance ($R_{\theta JB}$). A similar resistive element is used between the two blocks calculated from the junction-to-case thermal resistance ($R_{\theta JC}$). The sides of the blocks are made adiabatic. This extremely simple model captures the major heat transfer paths. The heat transfer to the printed circuit board is modeled with the junction-to-board thermal resistance. Heat transfer to the air is modeled with the junction-to-case thermal resistance. This is a low accuracy model best used for initial investigation.

2.2 Recommended Thermal Model for MSC8102, MSC8122, and MSC8126 Devices

The recommended model for the package is illustrated in **Figure 2** with each of the major pieces of the package modeled as a separate block.



Note: Thermal resistances between the substrate and die (underfill and bumps) and between the die and lid (adhesive) are shown as thick black lines.

Figure 2. Recommended Thermal Model for MSC8102, MSC8122, and MSC8126

Table 2. MSC8102, MSC8122, and MSC8126 Recommended Thermal Model Specifications

Layer	MSC8102			MSC8122 and MSC8126			Surface	Comments
	Size (mm)	Conductivity		Size (mm)	Conductivity			
		In Plane	Perpendicular		In Plane	Perpendicular		
Lid	16.5 × 16.5 × 0.5	Copper	Copper	11.5 × 14 × 0.5	Copper	Copper	ε = 0.4	
Lid Adhesive	16.5 × 16.5 × 0.05	1.07	1.07	11.5 × 14 × 0.05	1.07	1.07		Collapsed resistance
Die	13 × 14 × 0.76	Silicon	Silicon	9.7 × 11.8 × 0.76	Silicon	Silicon		Power source
Underfill and bump layer	13 × 14 × 0.05	0.6	2	9.7 × 11.8 × 0.07	0.6	2		Collapsed resistance
Substrate	20 × 20 × 1	16	4	20 × 20 × 1	21.8	1.02	ε = 0.9	
Balls	20 × 20 × 0.4	0.3	10.5	20 × 20 × 0.4	0.03	6.8		

The power can be applied as a source layer at the bottom of the die or as a bulk heat source in the die.

2.3 Component Arrays or “Farms”

To explore the effect of an array of components, a 3 × 3 array of components was measured and modeled, and then the simulations were generalized. For the measurement, a 3 × 3 array of components was placed on a 112 × 127 mm board with two internal planes of 30 µ thickness. This board was designed for a different experiment, so there were no vias under the component and the array was not perfectly centered on the board. The thermal resistance was determined using a package development die built with one layer of metal. The die has one metal trace for a heater and another one for temperature sensing. The temperature sensor was calibrated, the components were heated in the wind tunnel, and the die temperature determined from the sensor. **Table 3** lists the results of the junction-to-ambient thermal resistance measurement for the center component. The center component is the hottest component in natural convection; the trailing (downwind) component is frequently hotter in forced convection.

Table 3. Junction-to-Ambient Thermal Resistance Measurements

Airflow	Center Component Powered	Nine Components Powered
Natural convection	21.6 °C/W	40.4 °C/W
100 ft/min	18.8 °C/W	35.8 °C/W
200 ft/min	17.4 °C/W	31.0 °C/W
400 ft/min	15.6 °C/W	25.7 °C/W

Powering all nine components increases the temperature of the components with the junction-to-ambient thermal resistance (temperature rise) almost doubling.

2.4 Thermal Modeling Verification

To verify the modeling procedures, we simulated this configuration using the thermal model shown in **Figure 2**. The simulation was done with turbulence and radiation. The simulation and measurement agreed within 20 percent. The qualitative agreement was confirmed by comparing the temperature surface plots of the simulation to measurements using an infrared camera after painting the surface black.

The simulation allows us to examine air flow and temperatures around a component which we cannot do with measurements. The results are illustrated in **Figure 3**. Because the upstream component blocks the air flow, the air flows mostly across the top of the component. There is some “recirculation” or reverse flow of the air in the gap between components.

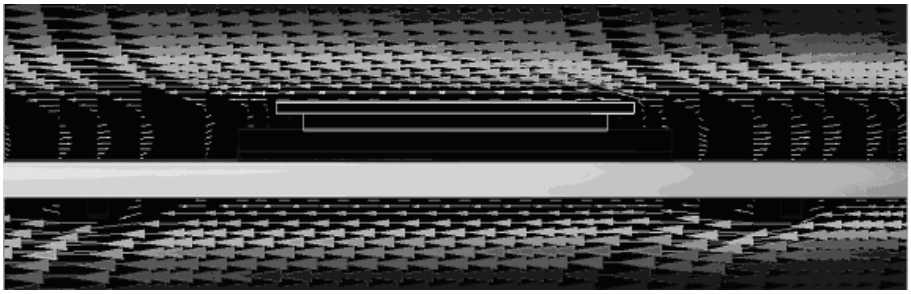


Figure 3. Airflow Across the Center Component

Figure 4 shows the temperature distribution in the center component and the surrounding air. Because of the relatively high conductivity of the materials in the package, there are not large temperature gradients within the package.

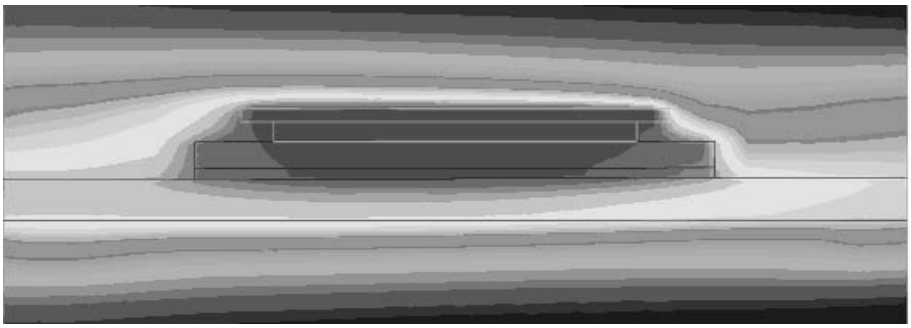


Figure 4. Center Component Temperature Distribution

2.5 Simulation of Arrays of Components.

After validating the thermal model of the component and demonstrating that the modeling yields reasonable accuracy for a array of components, we conducted a series of simulations using various component spacing. The results are shown in **Figure 5**.

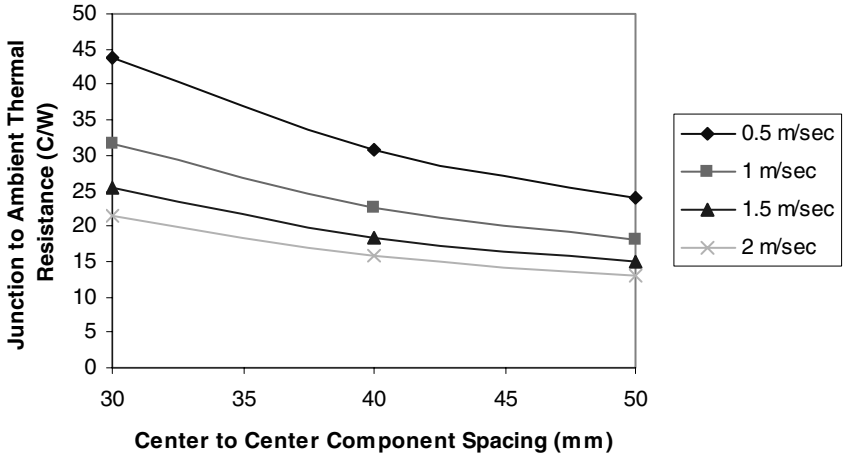


Figure 5. Change in Thermal Performance for Various Component Spacing

The drastic change in effective thermal performance as the components are more tightly grouped is most evident for the low air speeds. At 0.5 m/s, the thermal performance goes from 44 °C/W to 24 °C/W as the component spacing is changed from a center-to-center distance of 30 mm to 50 mm. The effect is less pronounced at higher air speeds. These simulations were for the center component of an array of 3 × 3 components. For the hottest component, the results are similar, as listed in **Table 4**.

Table 4. Junction-to-Ambient Thermal Resistance for the Hottest Component in a 3 x 3 Array

Board Size (mm)	Center-to-Center Spacing (mm)	Air Flow (m/s)			
		0.5	1.0	1.5	2.0
90 × 90	30	47	34	27	23
120 × 120	40	33	24	19	17
150 × 150	50	26	19	16	14

The hottest component temperature is a couple of degrees per watt hotter than the center component. The effect can be amplified by examining a 3 × 6 array of components. **Figure 6** shows the junction-to-ambient thermal resistance for the center column of components. Number 1 is the leading edge; number 6 is the trailing edge. The components are on 40 mm centers. For the 3 × 3 array on 40 mm centers, the hottest component had a junction-to-ambient thermal resistance of 24 °C/W at 1 m/s. For the 3 × 6 array, the hottest component is slightly hotter with a junction-to-ambient thermal resistance of 29 °C/W. The last component is not the hottest; apparently, the last component has less recirculation behind it and allows more cooling from the air flow. The next-to-last component, number 5, was the hottest.

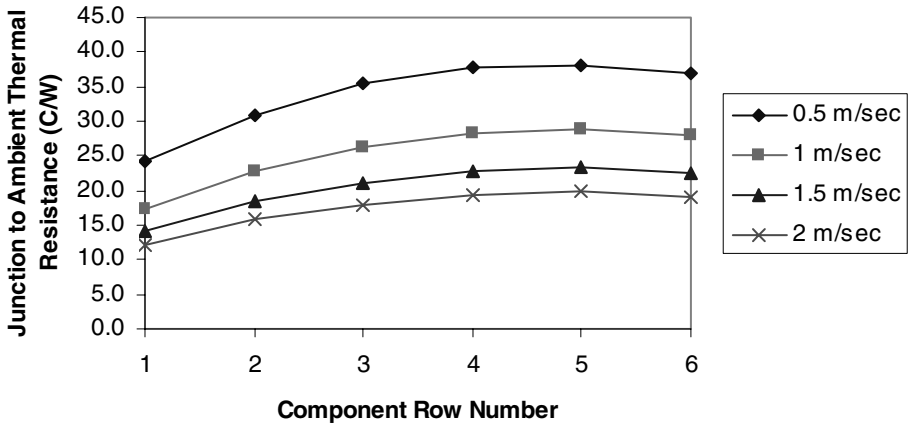


Figure 6. Change in Effective Thermal Resistance by Distance from Board Leading Edge Using a 3 × 6 Array

If the array is depopulated and the overall power dissipation on the board decreases, the effect of the adjacent components is less important. We explored this effect by depopulating the 3 × 3 array by four and using the same board size, as shown in **Figure 7**.

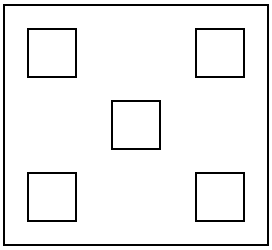


Figure 7. Depopulated 3 x 3 Array with 5 Components

The power dissipation on the board was reduced from 18 W to 10 W on the same 90 × 90 mm board size. At 1 m/s, the junction-to-ambient thermal resistance decreased from 34 °C/W to 19 °C/W as listed in **Table 5**.

Table 5. Center Component Junction-to-Ambient Thermal Resistance Differences Between Using 9 or 5 Components on the Same Size Board

Number of Components	Board Size (mm)	Air Flow (m/s)			
		0.5	1.0	1.5	2.0
9	90 × 90	47 °C/W	34 °C/W	27 °C/W	23 °C/W
5	90 × 90	26 °C/W	19 °C/W	15 °C/W	13 °C/W

3 Conclusion

This application note highlights the change in effective thermal performance that occurs when the number of similar components on the application board is increased. As the number of components or the power dissipation of other components on the printed circuit board increases, the components naturally becomes hotter. System-level thermal analysis is the best technique to address this issue. If the density of components and the ambient temperature are too high, use the typical methods to improve thermal performance and lower component temperatures. If used, attach heat sinks to the printed circuit board using a spring clip mechanism.

4 References

[1] Flotherm *http://www.flotherm.com.*

[2] IcePak Fluent, Inc. *http://www.fluent.com.*

[3] Maya MAYA Heat Transfer Technologies Ltd., *http://www.mayahtt.com.*

[4] G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” *Electronic Packaging and Production*, pp. 53-58, March 1998.

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