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Clock Mode Selection for MSC8126 Mask Set K98M

By Donald Simon and Wes Ray

This application note describes the MSC8126 clock modes for mask set K98M. It also describes a Microsoft® Excel application that assists users in determining the internal/external system clock frequencies generated by the input clock and a 5-bit MODCK value. Mask set K98M supports 27 valid clock modes, as tested using the 0K98M and 1K98M mask sets. The Excel application helps you to reduce design time significantly in two ways:

- Quickly determine whether an input clock frequency and clock mode combination violate frequency limitations.
- Evaluate a wide range of input clock frequencies to determine which combinations meet system requirements.

CONTENTS

1 Mask Set

Each MSC8126 device is labeled with a mask set number (for example mask set 1K98M).

2 Clock Configuration

Figure 1 shows the functional clock block diagram for mask set K98M. The clock contains an internal system phase-lock loop (SPLL), bus division factor (BUSDF), clocks for the timers, universal asynchronous receiver/transmitter (UART), time-division multiplexer (TDM), and direct slave interface (DSI). The SPLL contains a phase-lock loop feedback division factor (PLLFDF), a PLL input clock division factor (PLLRDF), a phase frequency detector (PFD) and voltage control oscillator (VCO), and a PLL output clock division factor (PLLODF). All components in **Figure 1** are clock dividers except for the PFD and VCO.

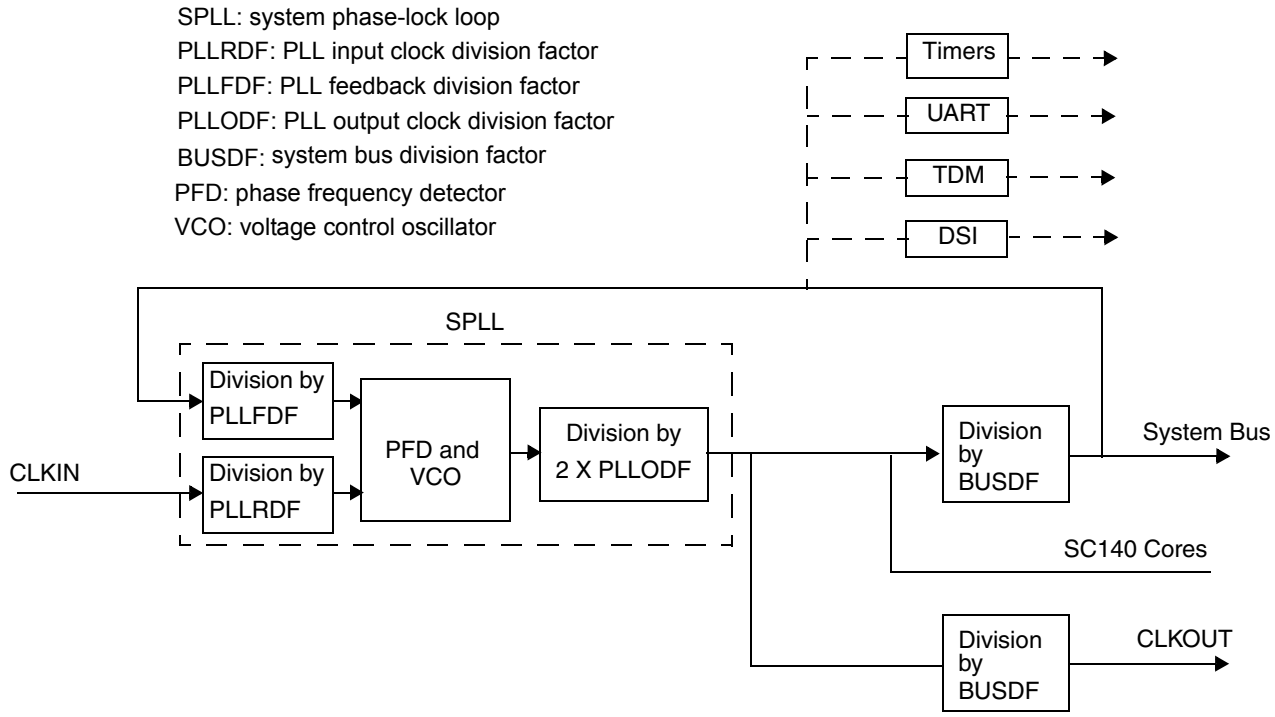


Figure 1. MSC8126 Functional Clock Block Diagram for Mask Set K98M

The timers, UART, TDM, and DSI modules are shown as dotted lines in **Figure 1** because they can use clocks from sources other than the 60x-compatible system bus clock. The timer clock sources are selected by the Timer Configuration Registers, TCFRA and TCFRB. If the system bus clock is the source for the timer, the timer divider is always two. The timers can also be clocked by the GPIO signals, which are clocked separately from the timer interface to the IPBus. The UART baud rate is based on the system bus clock/ (16 × SCIBR[12–0]), where the SCIBR is the SCI Baud-Rate register. The TDM processes the data with the system bus clock. The maximum TDM data bit rate processing is limited to half of the system bus clock. Each TDM has three clock zones:

- The receiver is clocked by RCLKx.
- The transmitter is clocked by TCLKx.
- The interface to the local bus is clocked by the system bus clock.

The DSI has two clearly separated clock zones:

- The DSI interfaces with the external host asynchronously or via a synchronous interface clocked by the HCLKIN signal.
- The DSI interfaces with the internal local bus via the system bus clock.

For details on clocking for the timers, UART, TDM, and DSI, consult the *MSC8126 Reference Manual* (MSC8126RM). **Table 1** shows the maximum frequencies for the SC140 core and system bus for mask set K98M. You must ensure that the system design does not exceed these maximum frequencies.

Table 1. Mask Set K98M Maximum Frequency Limits

	MSC8126		
	300 MHz Device	**400 MHz Device**	**500 MHz Device**
SC140 cores frequency	300 MHz	400 MHz	500
System bus and CLKOUT	100 MHz	133.3 MHz	166.7
DSI clock frequency (HCLKIN)	70 MHz	70 MHz	70 MHz

3 Clock Modes

All MSC8126 devices use a 5-bit MODCK value to configure the clock mode. Refer to the clock mode chart in **Section 7** for valid settings for mask set K98M. The 5-bit MODCK value is determined at reset by sampling the following:

- Two multiplexed system pins (MODCK[1–2])
- MODCK_H field in the Hard Reset Configuration Word (HRCW), corresponding to MODCK[3–5]

The MODCK_H field defines the three most significant bits of the MODCK value. The MODCK[1–2] pins define the two least significant bits. The following example illustrates how the two sets of values define MODCK. The 5-bit values are organized for explanation purposes as one 3-bit and one 2-bit number: xxx-yy, where:

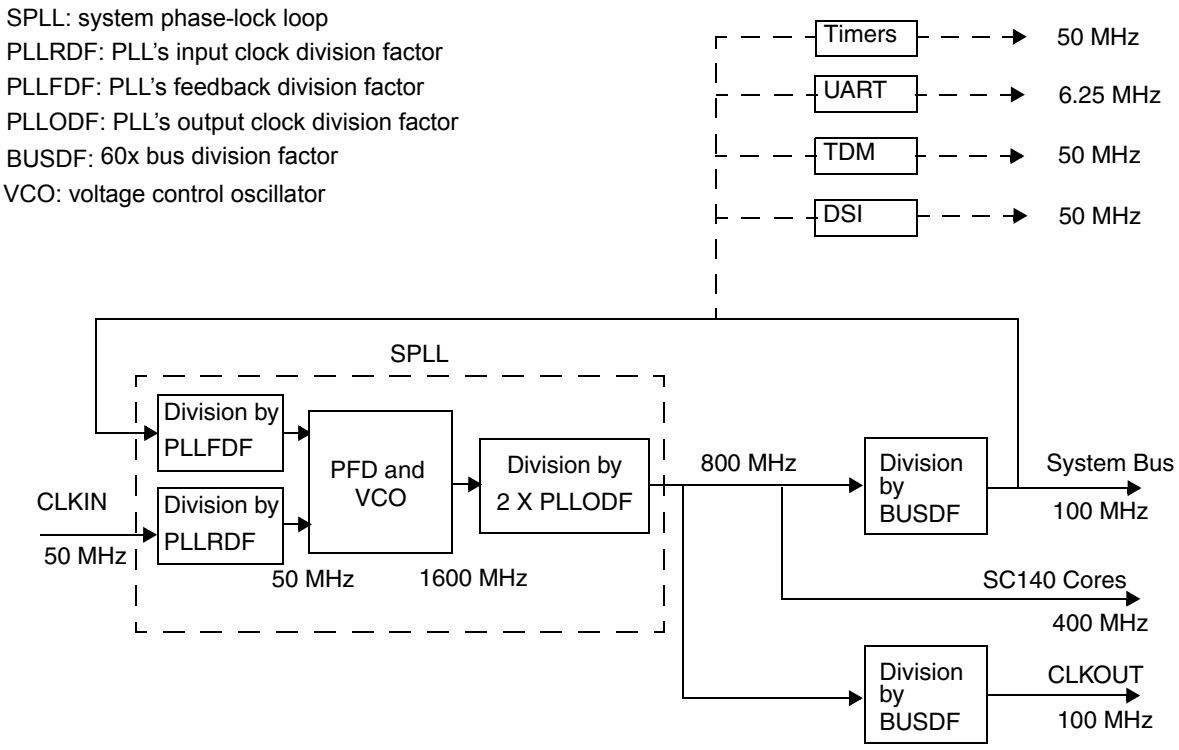
- xxx = MODCK_H. Three clock mode high bits from the HRCW (bits 28–30) (MODCK[3–5]).
- yy = MODCK[1–2]. Two clock mode low bits from external inputs.

Table 2 shows an example of how to derive the MODCK value from the MODCK_H (aka MODCK[3–5]) and MODCK[1–2] values.

Table 2. Clock Mode Example

Input	MODCK Determination Example
HRCW[28–30] = 011	MODCK_H = 011
HD3/MODCK1 pin is pulled up	MODCK1 = 0
HD4/MODCK2 pin is pulled down	MODCK2 = 1

The example in **Table 2** corresponds to a MODCK value of 13: MODCK_H-MODCK[1–2] = 011-01. The clock mode (MODCK) number is the decimal equivalent of the MODCK value read as a binary value: $01101_2 = 13_{10}$ = clock mode 13. **Figure 2** shows an example with clock mode 13 for mask set K98M and the functional clock diagram assuming a 50 MHz input clock (CLKIN).



Clock Mode	MODCK_H-MODCK[1–3]	FDF	RDF	VCO	System Bus/ CLKIN Ratio	Core/Bus Ratio
13	011-01	2	1	32	2x	4x

Figure 2. Mask Set K98M Clocking Example

4 Excel Application

This section explains how to use the Microsoft Excel file listed in **Table 3**.

Table 3. Mask Set K98M Excel File

MSC8126 Mask Set	Excel File Name
0K98M, 1K98M	MSC8126_Mask_Set_K98M.xls

When the Excel file in **Table 3** is opened, a window like that shown in **Figure 3** appears. Select **ENABLE MACROS** to enter the spreadsheet.

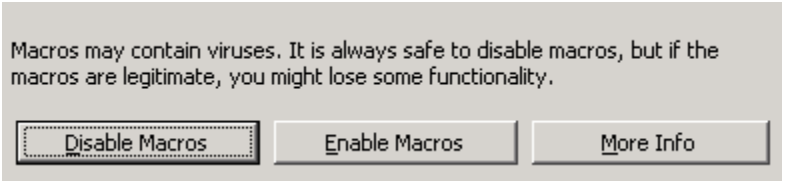


Figure 3. Opening Clock Spreadsheet in Excel

The Excel file contains the following two worksheets:

- *Clock Mode Chart*
- *Clocking Scheme*.

4.1 Mask Set K98M Clock Mode Chart Worksheet

Figure 4 show the *Clock Mode Chart* worksheet, which lists the valid clock modes for the mask set K98M. It requires two entries:

- **CLKIN (MHz)** (cell C5)
- **MAX CORE FREQUENCY (MHz)** (cell E6).

When the desired **CLKIN** frequency in MHz (input clock) and **MAX CORE FREQUENCY** in MHz are entered into cell C5 and E6, respectively, the other cell values in the worksheet update automatically. Only rows colored in yellow are valid. All values in red are invalid. Column R in the spreadsheet indicates whether the **CLKIN**, **MAX CORE FREQUENCY** frequency, and a specific clock mode constitute a valid combination.

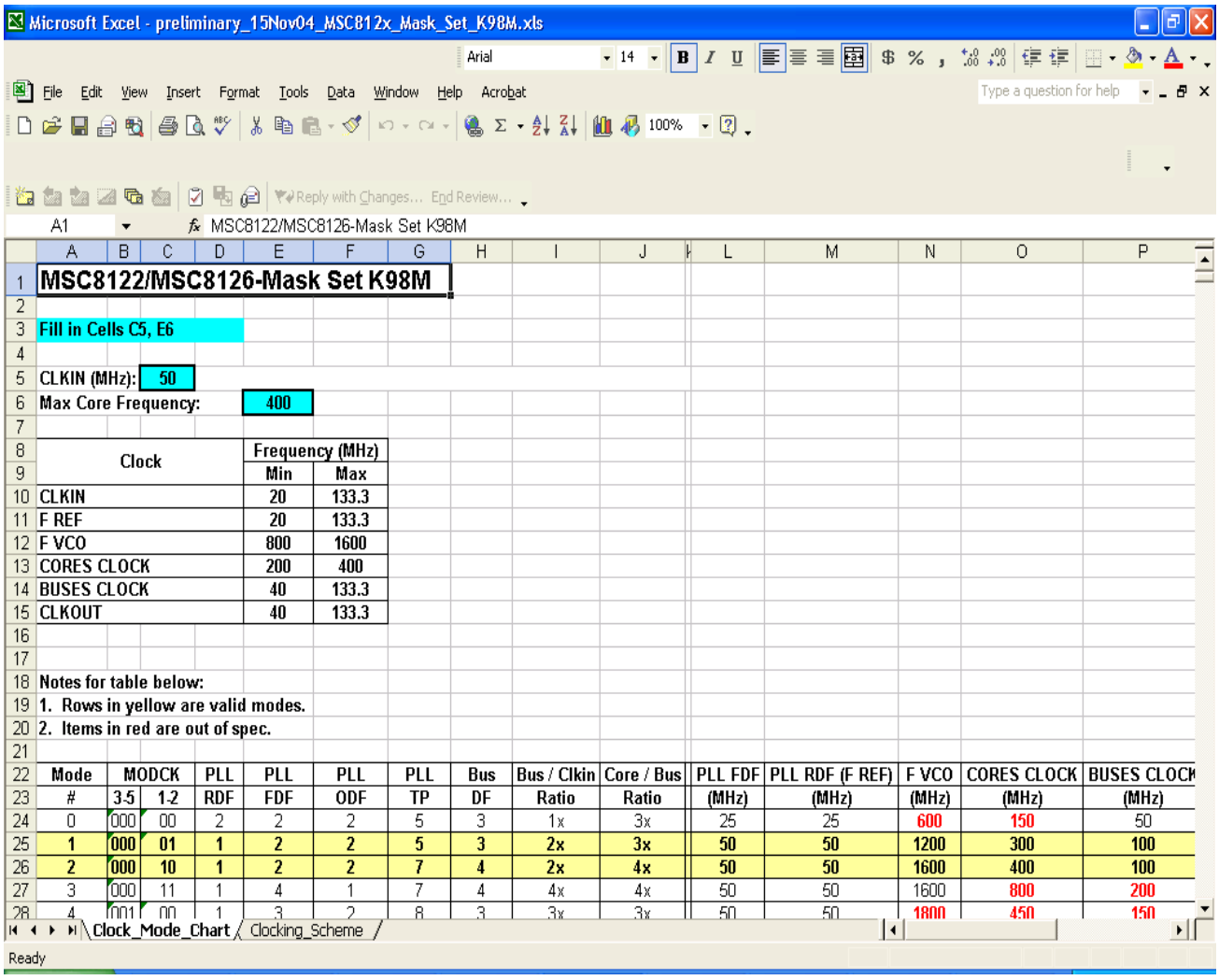


Figure 4. Mask Set K98M Clock Mode Chart

4.2 Mask Set K98M Clocking Scheme Worksheet

Figure 5 displays the mask set K98M *Clocking Scheme* worksheet, which shows the various frequencies, dividers, and multipliers used in the MSC8126 clock module. It requires three entries:

- **CLKIN (MHz):** (cell C5)
- **Clock Mode:** (cell C6)
- **Max Core Freq:** (cell C7)

Figure 5 depicts an example with a clock in (CLKIN) value of 50 MHz (cell C5), a clock mode number of 13 (cell C6), and a max core frequency of 400 MHz (cell C7). Error messages are shown in cell A10. If there are no error messages, cell A10 is left blank. All values changed in the *Clock Mode Chart* worksheet do not change the *Clocking Scheme* worksheet, and *vice versa.*

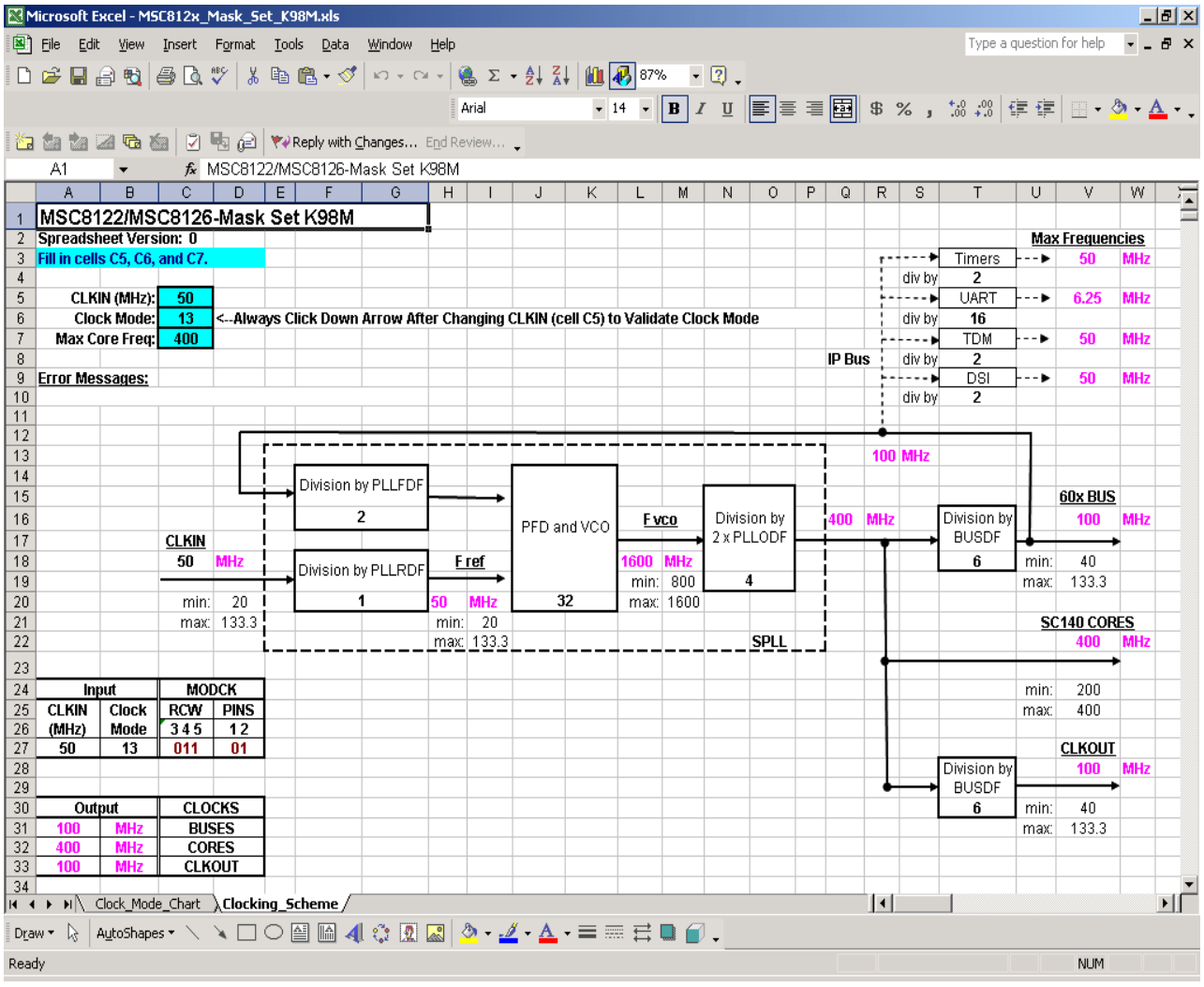


Figure 5. Mask Set K98M Clocking Scheme Worksheet Example

5 Excel Worksheet Quick Guide

Table 4 lists the steps for using the Excel worksheets.

Table 4. Excel Program Procedure

Step	Action	Comments
1	Start the Excel program and open the file that corresponds to the MSC8126 mask set.	Select MSC812x_Mask_Set_K98M.xls
2	Select a worksheet: • Clock Mode Chart • Clocking Scheme	If *Clock Mode Chart* is chosen, perform step 3A. If *Clocking Scheme Chart* is chosen, perform step 3B.
3A	For the *Clock Mode Chart* worksheet: • Enter CLKIN frequency into cell C5. • Enter the maximum rated speed of the MSC8126 into cell E6. • Verify that there are no frequency violations in columns R and S.	Refer to rows A22 through A55. Rows in yellow are valid modes. Items in red are out of spec.
3B	For the *Clocking Scheme* worksheet: • Enter CLKIN frequency into cell C5. • Enter the Clock Mode number into cell C6. • Enter the maximum rated speed of the MSC8126 into cell C7. • Verify that there are no frequency or errata violations (cell A10).	Refer to **Section 7** or the *Clock Mode Chart* worksheet for valid clock modes. Cells A24 through D27 show the input values. Cells A30 through D33 show the output values.

When calculating clock frequencies, be sure to check the data sheet for the maximum/minimum input clock frequencies and the errata for limitations.

6 Errata

There are no known errata in the K98M mask set that impose clock limitations. For a complete list of errata, consult the Freescale web site listed on the back cover of this document.

7 Mask Set K98M Configuration Modes

Table 6 show the clock modes for mask set K98M and their respective bus/CLKIN and core/bus ratios.

Table 5. Clock Configuration Modes

		MSC8126	
Mode	**MODCK[3–5] MODCK[1–2]**	**Bus/CLKIN Ratio**	**Core/Bus Ratio**
0	000-00	1	3
1	000-01	2	3
2	000-10	2	4
3	000-11	4	4
4	001-00	3	3
5	001-01	4	3

Table 5. Clock Configuration Modes (Continued)

		MSC8126	
Mode	**MODCK[3–5] MODCK[1–2]**	**Bus/CLKIN Ratio**	**Core/Bus Ratio**
6	001-10	3	4
7	001-11	1	4
8	010-00	2	4
9	010-01	4	4
10	010-10	2	3
11	010-11	1.5	4
12	011-00	Reserved	
13	011-01	2	4
14	011-10	2	5
15	011-11	1	5
16	100-00	2	5
17	100-01	3	5
18	100-10	2	6
19	100-11	1	6
20	101-00	2	6
21	101-01	1	8
22	101-10	2	8
23	101-11	1	10
24	110-01	Reserved	
25	110-00	Reserved	
26	110-10	Reserved	
27	110-11	Reserved	
28	111-00	1	3
29	111-01	1	4
30	111-10	1	5
31	111-11	1	6

8 References

- MSC8126 *Technical Data.*
- MSC8126RM, *MSC8126 Reference Manual.*
- MSC8126UG, *MSC8126 User's Guide.*

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