Freescale Semiconductor
Application Note

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Layout and Design Guidelines for the MC13883

1 Introduction

This application note describes guidelines for a Printed Circuit Board (PCB) footprint for the QFN40 package used for the MC13883 integrated charger. Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

A general description for QFN packages can be found in AN1902 at the Freescale web site:

http://www.freescale.com

2 Component Copper Layer

Figure 1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the QFN40 package consists of 40 IC contact pads and a centered ground pad.

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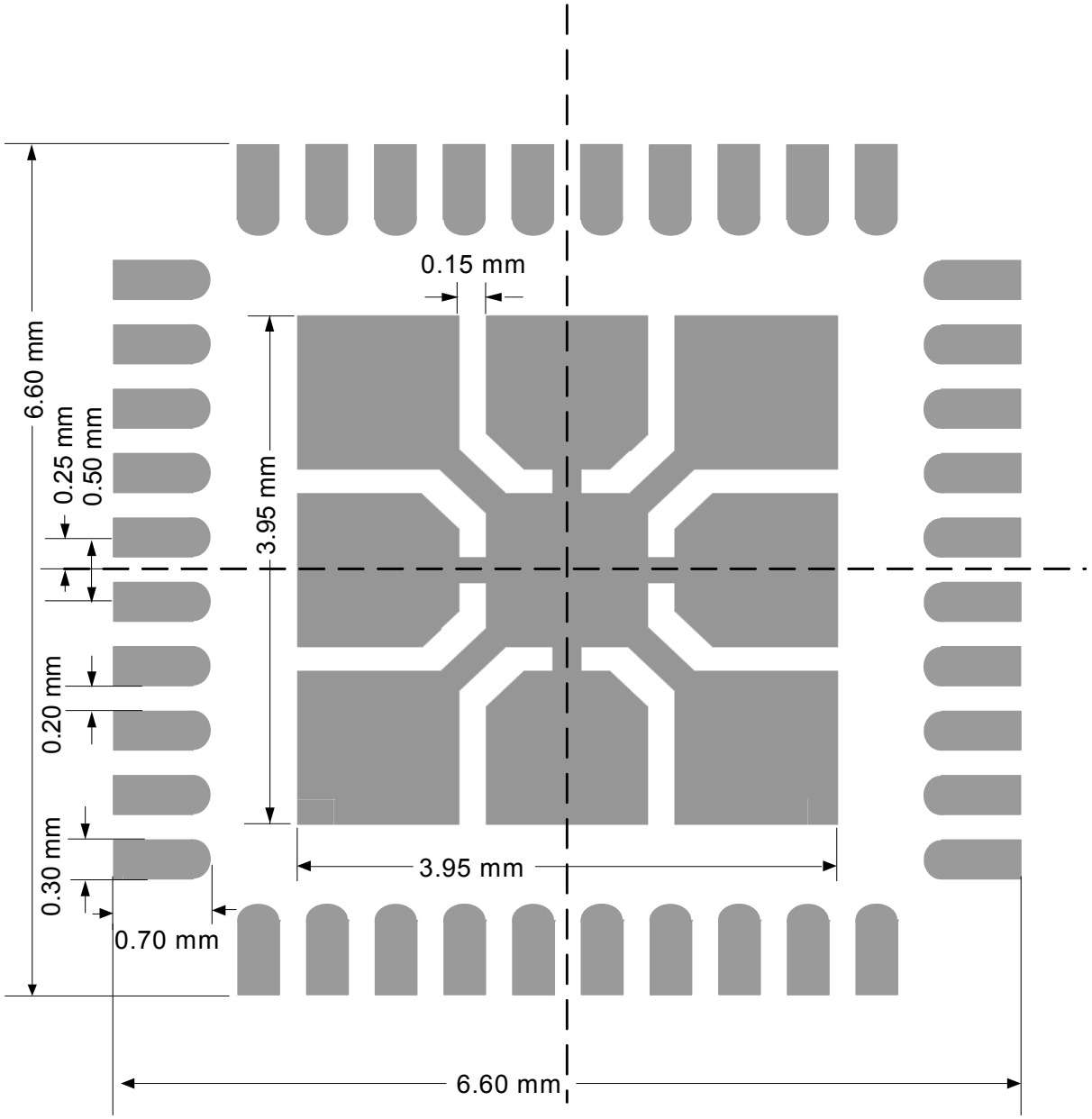

Figure 1. Component Copper Layer

3 Solder Mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask. The IC contact openings actually touch, so there is no septum between openings. The lines shown are an artifact of the CAD drawing.

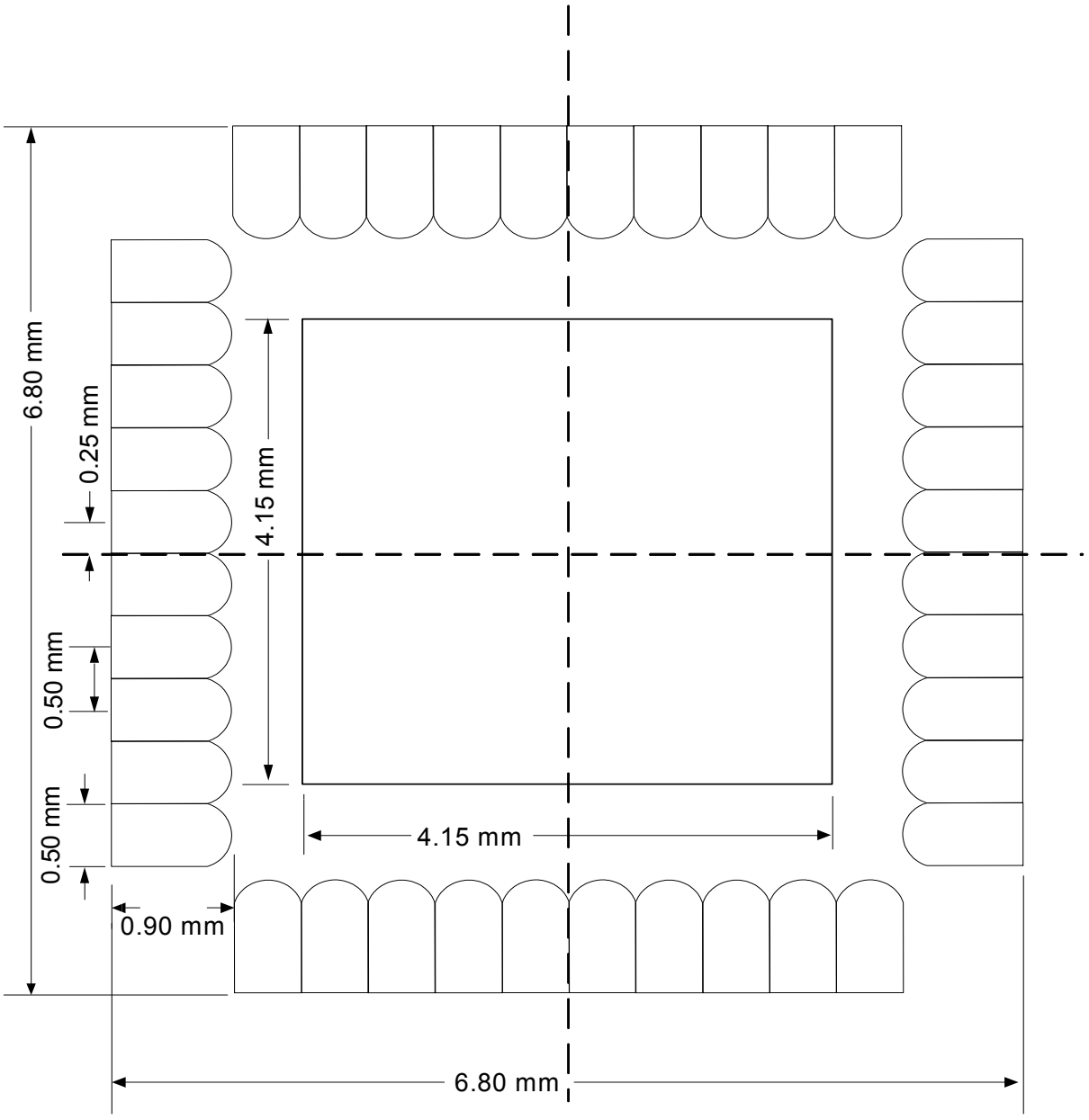

Figure 2. Solder Mask Pattern

4 Solder Paste Stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 3 shows a recommended solder stencil pattern. Stencil thickness should be 0.13 mm–0.15 mm. Other patterns and opening sizes can be used if too much solder is being applied. See Section 5, "Problems with Excess Solder," for more information.

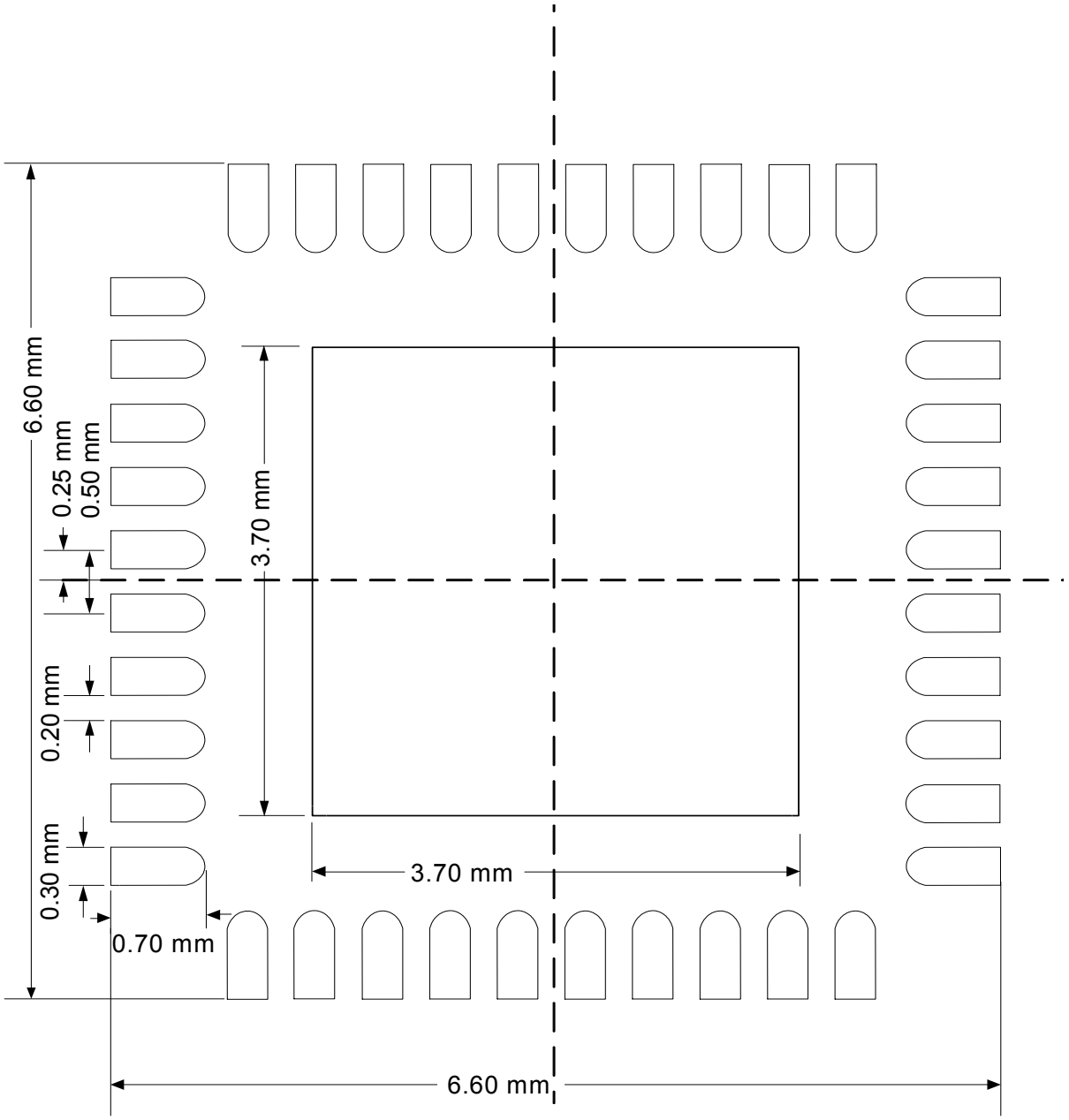

Figure 3. Solder Stencil Pattern

5 Problems with Excess Solder

Excess solder may cause the QFN to “float” or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

Package floating can be eliminated by reducing the area of solder paste on the centered pad. Figure 4 shows alternative solder stencil patterns to reduce the amount of solder paste applied to the centered pad.

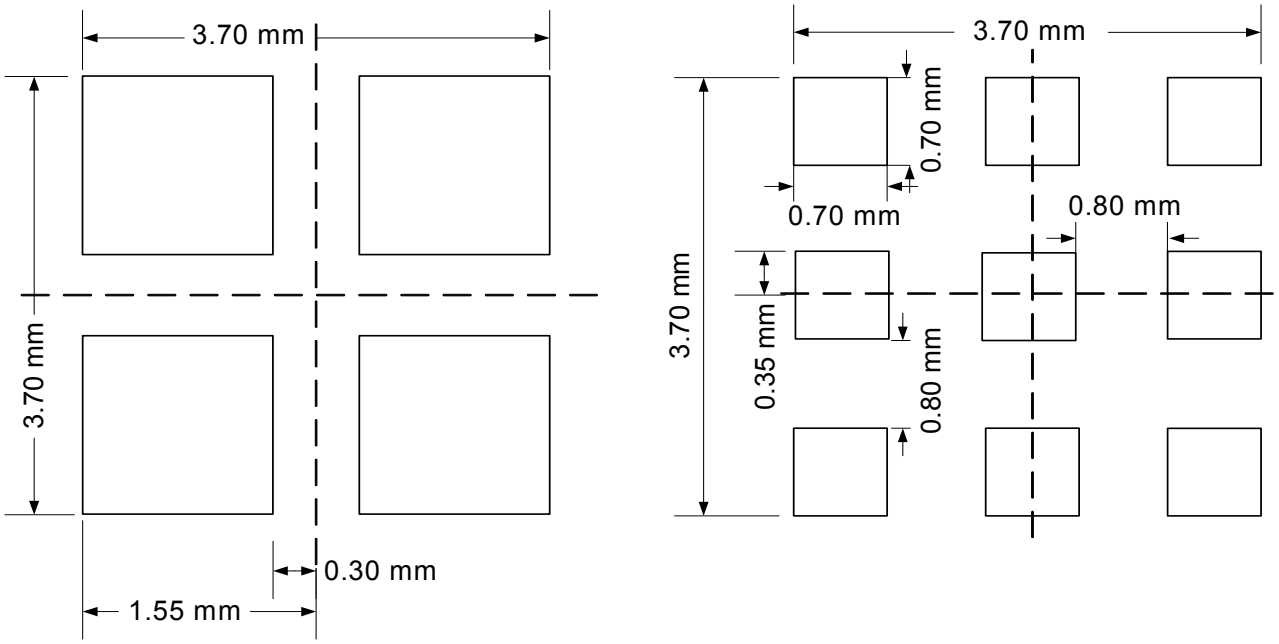

Figure 4. Alternative Solder Stencil Patterns

Solder bridging between package contacts can be reduced by adjusting the metal contact pad widths in Figure 1 from 0.3 mm to 0.25 mm and the solder mask pad openings from 0.5 mm to 0.4 mm. This allows for a 0.1 mm septum of solder mask between the pads. However, this approach may not be feasible for all board houses and may increase assembly cost.

6 QFN40 Package Dimensions

Figure 5 through Figure 8 show the QFN40 package dimensions. The package information shown in these figures is available from the Freescale web site at:

http://www.freescale.com/files/shared/doc/package_info/98ASA10655D.pdf

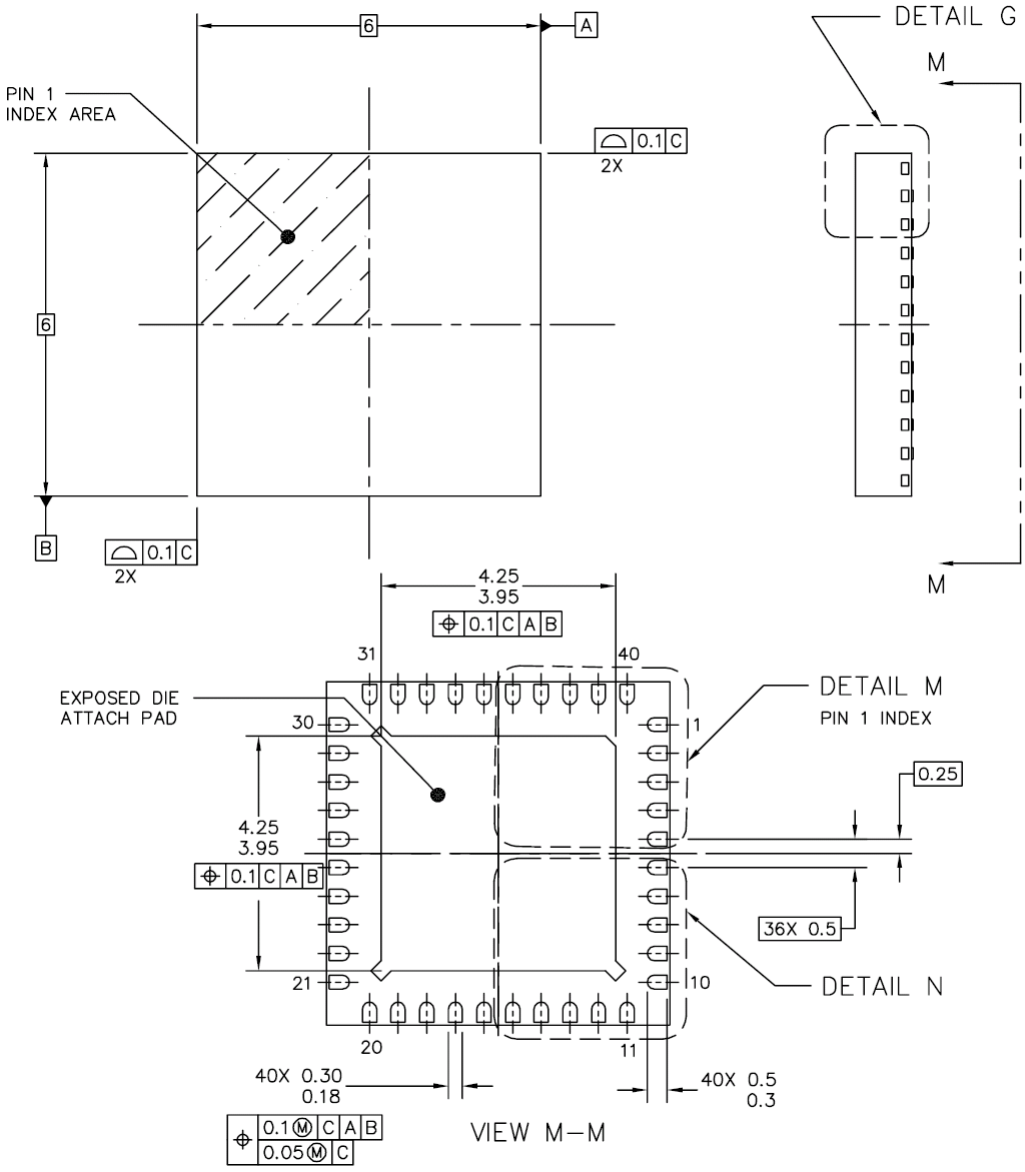

Figure 5. Outline Dimensions for QFN40, 6x6 mm
(Case Outline 1624-01, Issue O)

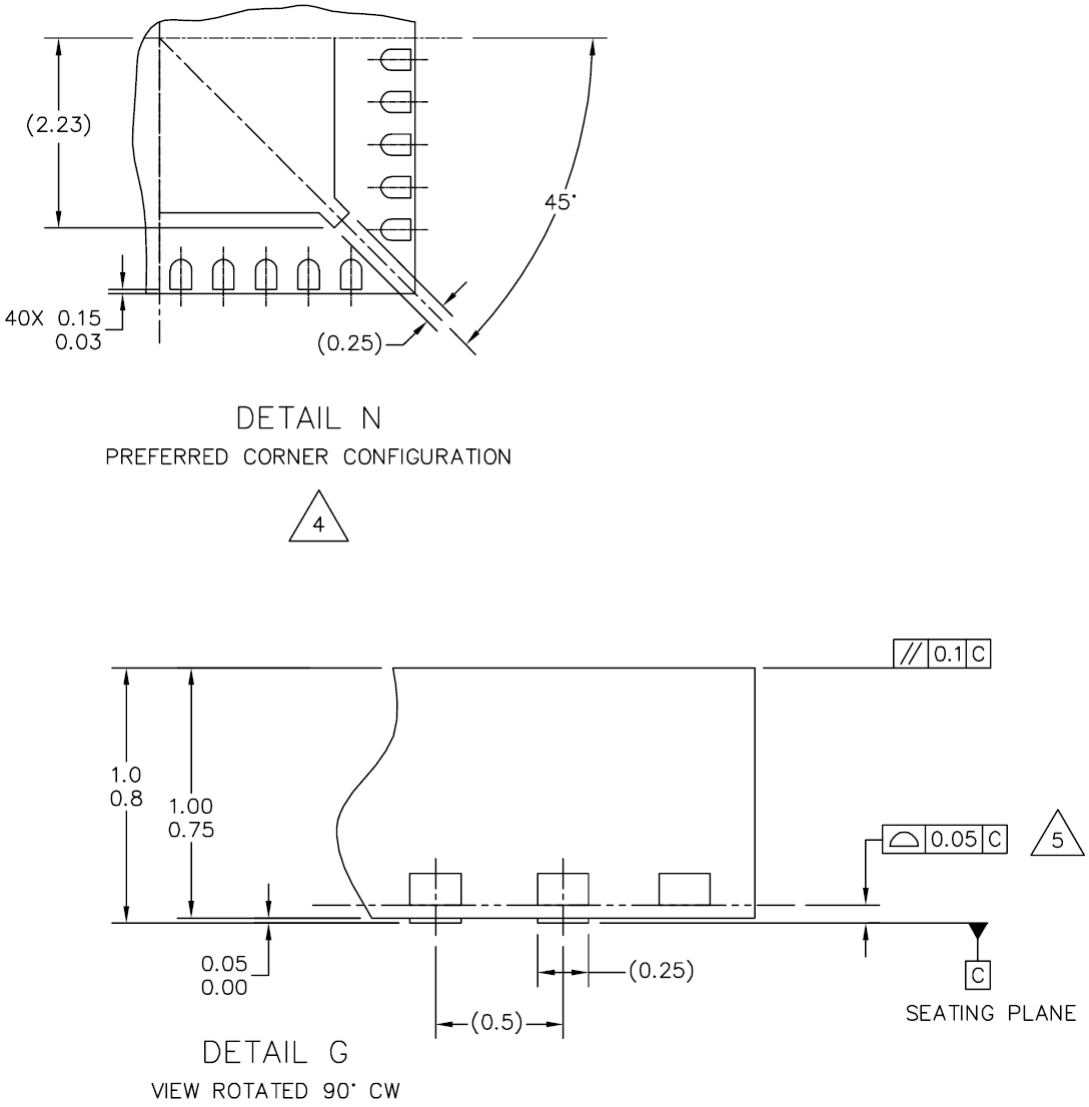

Figure 6. Outline Dimensions for QFN40, 6x6 mm - Continued
(Case Outline 1624-01, Issue O)

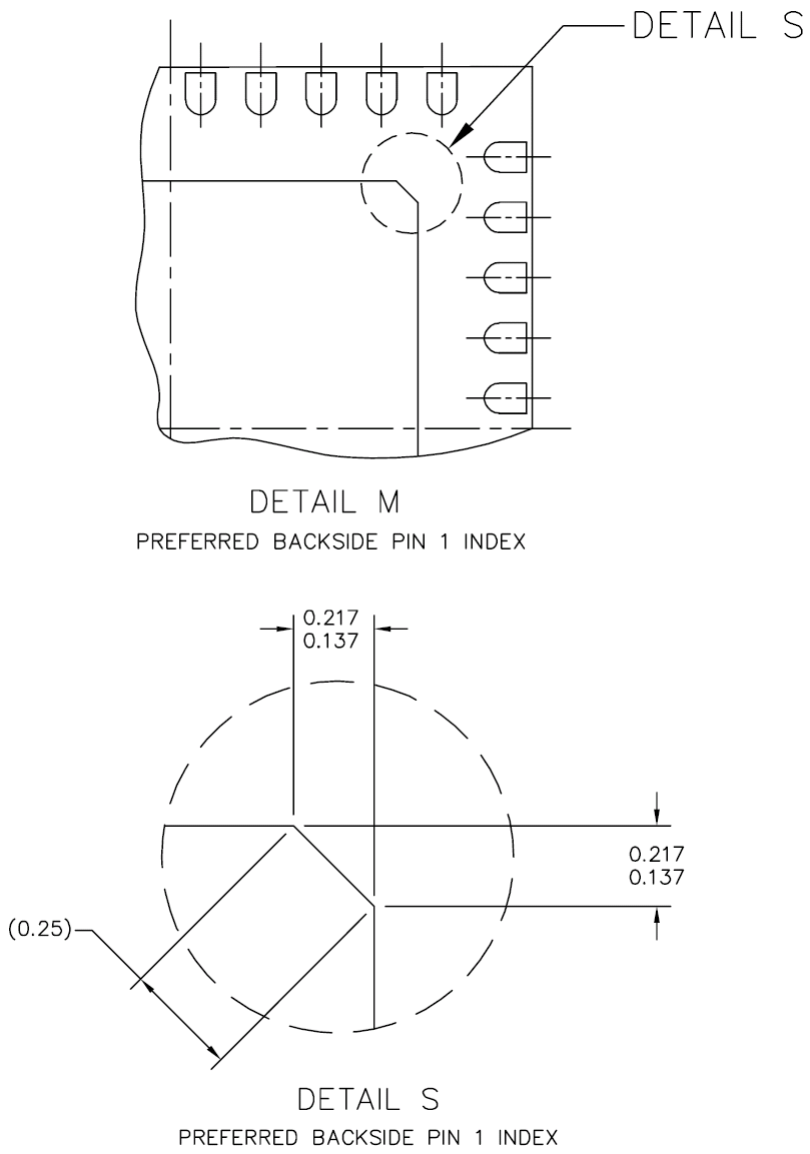

Figure 7. Outline Dimensions for QFN40, 6x6 mm - Continued
(Case Outline 1624-01, Issue O)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
6. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.
7. MINIMUM METAL GAP 0.2 MM.

Figure 8. Outline Dimensions for QFN40, 6x6 mm - Continued
(Case Outline 1624-01, Issue O)

7 Layout Considerations

- DP/DM lines need to be 45 ohms.
- The capacitor on VC should be close to the VC pin.
- The capacitor on BG_BYP should be close to the BG_BYP pin.
- The path impedance from VBUS to Battery should be minimized to reduce the voltage drop along this path.
- The impedance in the charge path from ISENSE to BATTP should minimal so that the current is accurately controlled.
- The sense lines from RSENSE to MC13883 should be short and isolated from any noise to maintain the accuracy of the charger. These lines should be connected directly from the pads of RSENSE resistor to the ISENSE and BP pins of the IC.
- No components should be placed on the gates of the control lines CHRGCTRL, BATTFET, BPFET.

8 Component Selection

- The 2.2uF capacitor on VBUS must be greater than 1.3uF at 5V.
- The recommend devices for M1, M2, and M4 are as shown in Table 1.

Table 1. Recommended Devices

	M1	M2	M4
Combination 1	Si8415	Si8401	Si8401 or FDZ293P
Combination 2	FDZ293P	FDZ293P	Si8401 or FDZ293P

9 Document Revision History

Revision 0.1: Copyright date change in preparation for public release.

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