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Application Note

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MCF5445*x* Configuration and Boot Options

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1 Configuration Modes

The Freescale ColdFire® MCF5445*x* embedded microprocessor family offers a selection of reset configuration and boot modes. This application note describes all of the mode options available to the user and some of the benefits and implications of each.

There are several operating parameters of the MCF5445*x* devices that can be configured at reset and there are three modes available for configuring these parameters. The processor samples two input signals at reset, BOOTMOD[1:0], to determine which configuration method is used. Table 1 shows the encoding for these two signals and the following sections describe each mode in detail.

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Table 1. Reset Configuration Modes

BOOTMOD[1:0]	Meaning
00	Default configuration
01	Reserved
10	Parallel configuration—configuration data obtained from FlexBus signals
11	Serial configuration—configuration data obtained from serial memory device

The configurable operating parameters differ depending on the reset configuration mode used. Also, some settings can be set or changed following reset configuration. Table 2 shows all possible configuration parameters, the modes that are capable of setting them at reset, and whether or not they are run-time configurable.

Table 2. Summary of Configurable Parameters

Parameter	Configured by			Run-time Configurable
	Default[1]	Parallel	Serial	
FlexBus Multiplexing[2]	•	•	•	No
FlexBus Boot Port Size	•	•	•	No
PLL Enable	•	•	•	Yes
PLL VCO Multiplier	•	•	•	Yes
Oscillator Mode[3]	•	•	•	No
PCI Enable[4]	•	•	•	No
PCI Slew Rate	•	•	•	Yes
PCI Interrupt Enable	•[5]	•[5]	•	Yes
PCI Configuration Retry	•[5]	•[5]	•	Yes
PCI BAR Enables	•[5]	•[5]	•	Yes
PCI Device ID	—	—	•	No
PCI Vendor ID	—	—	•	No
PCI Class Code	—	—	•	No
PCI Revision ID	—	—	•	No
PCI Subsystem ID	—	—	•	Yes
PCI Subsystem Vendor ID	—	—	•	Yes
Bus Monitor Enable	—	—	•	Yes
Bus Monitor Timeout	—	—	•	Yes
Timer /SSI DMA Channel Mux Select	—	—	•	Yes
USB Clock Source	—	—	•	Yes

Table 2. Summary of Configurable Parameters (continued)

Parameter	Configured by			Run-time Configurable
	Default[1]	Parallel	Serial	
USB VBUS Overcurrent Sense Polarity	—	—	•	Yes
SSI RXD/TXD Pull Enable	—	—	•	Yes
SSI RXD/TXD Pull Select	—	—	•	Yes
SSI Clock Source	—	—	•	Yes

1 The default configuration mode loads preset values into these parameters and they cannot be overridden by the user at reset. Refer to Section 1.1, "Default Configuration" for details.

2 The FB_AD[31:0] can be multiplexed (used for address and data) or the PCI_AD[31:0] signals can be used for the FlexBus address. The FB_AD[31:0] can also be configured as GPIO if using serial configuration mode.

3 Defines the use of an external crystal oscillator or an external clock source as the input clock reference.

4 PCI parameter settings are valid for 360-pin devices only.

5 In default and parallel configuration modes, these parameters are affected by the host/agent mode selection. In serial configuration mode, these parameters can be set directly.

1.1 Default Configuration

The default configuration mode is the simplest option. This mode forces parameters to a predetermined default state. If the BOOTMOD[1:0] input pins are driven to 2'b00 during reset, the MCF5445*x* is configured according to data in the Reset Configuration (RCON) register. The contents of the RCON register depend on the version of the MCF5445*x* device being used; a 256-pin, non PCI-capable device, or a 360-pin, PCI-capable device.

Table 3 shows the default parameter settings for the 360-pin devices. This mode enables PCI operation and prohibits the use of an external crystal as the clocking device.

Table 3. 360-pin Default Configuration Settings

Parameter	Setting
FlexBus multiplexing	Muxed
FlexBus boot port size	8-bit
PLL enable	PLL enabled
PLL VCO multiplier	6 x input clock
Oscillator mode	Oscillator bypass
PCI enable	PCI enabled
PCI slew rate	66MHz
PCI interrupt enable	Interrupt disabled (host mode)
PCI configuration retry	Inbound accesses allowed
PCI BAR enables	All BARs enabled

Table 4 shows the default parameter settings for the 256-pin devices. This mode forces the use of a crystal oscillator circuit as the input clock source. Also, since the PLL is enabled by default and the default PLL VCO multiplier is x16, the maximum crystal frequency allowed to stay within the PLL VCO specification is 33.33 MHz.

Table 4. 256-pin Default Configuration Settings

Parameter	Setting
FlexBus multiplexing	Non-muxed
FlexBus boot port size	16-bit
PLL enable	PLL enabled
PLL VCO multiplier	16 x input clock
Oscillator mode	Crystal oscillator
PCI enable	PCI disabled
PCI slew rate	N/A
PCI interrupt enable	N/A
PCI configuration retry	N/A
PCI BAR enables	N/A

1.2 Parallel Configuration

The parallel configuration mode is more flexible then the default configuration mode. If the BOOTMOD[1:0] input pins are driven to 2'b10 during reset, the MCF5445*x* is configured according to data read from the FlexBus FB_AD[7:0] pins. Table 5 shows the parallel configuration settings for both the 360-pin and 256-pin devices.

Table 5. Parallel Configuration Settings[1]

Override Pins in Reset[2,3]	Function
FB_AD[7:5]	**FlexBus, PCI, Port Size Mode (360-pin Devices)**
111	PCI, muxed FB addr/data, 8-bit boot
110	No PCI, muxed FB addr/data, 16-bit boot
101	No PCI, muxed FB addr/data, 8-bit boot
100	No PCI, muxed FB addr/data, 32-bit boot
011	PCI, muxed FB addr/data, 16-bit boot
010	No PCI, non-muxed FB addr/data, 16-bit boot
001	No PCI, non-muxed FB addr/data, 8-bit boot
000	No PCI, non-muxed FB addr/data, 32-bit boot
FB_AD[7:5]	**FlexBus, PCI, Port Size Mode (256-pin Devices)**
111	Reserved

Table 5. Parallel Configuration Settings[1] (continued)

Override Pins in Reset[2,3]	Function
110	No PCI, muxed FB addr/data, 16-bit boot
101	No PCI, muxed FB addr/data, 8-bit boot
100	No PCI, muxed FB addr/data, 32-bit boot
011	Reserved
010	No PCI, non-muxed FB addr/data, 16-bit boot
001	No PCI, non-muxed FB addr/data, 8-bit boot
000	No PCI, non-muxed FB addr/data, 32-bit boot
FB_AD4	**PLL Mode**
1	Limp mode
0	PLL mode
FB_AD3	**PCI Host/Agent Mode (360-pin PCI Enabled Devices)**
1	PCI host mode (Interrupt disabled, inbound configuration accesses allowed, all BARs enabled)
0	PCI agent mode (Interrupt enabled, inbound configuration accesses retried, all BARs disabled)
FB_AD3	**Oscillator Mode (360-pin PCI Disabled Devices and 256-pin Devices)**
1	Oscillator bypass mode
0	Crystal oscillator mode
FB_AD2	**PCI Slew Rate Mode (360-pin PCI Enabled Devices)**
1	66 MHz slew rate mode
0	33 MHz slew rate mode
FB_AD[2:0]	**PLL Multiplier (360-pin PCI Disabled Devices and 256-pin Devices)**
111	VCO = 8 x REF
110	VCO = 16 x REF
101	VCO = 6 x REF
100	VCO = 12 x REF
011	VCO = 18 x REF
010	VCO = 24 x REF
001	VCO = 10 x REF
000	VCO = 20 x REF

Table 5. Parallel Configuration Settings[1] (continued)

Override Pins in Reset[2,3]	Function
FB_AD[1:0]	**PLL Multiplier (360-pin PCI Enabled Devices)**
11	VCO = 8 x REF CPU = 266/200; PCI = 66/50
10	VCO = 16 x REF CPU = 266/200; PCI = 33/25
01	VCO = 6 x REF CPU = 200/180; PCI = 66/50
00	VCO = 12 x REF CPU = 200/240; PCI = 33/40

1 Modifying the default configurations through the FB_AD[7:0] pins is possible only if the external BOOTMOD[1:0] pins are 10 while $\overline{\text{RSTOUT}}$ is asserted.

2 The FB_AD[7:0] pins must be actively driven. The FB_AD[31:8] pins do not affect reset configuration and should be pulled high or allowed to float.

3 The external reset override circuitry drives the data bus pins with the override values while $\overline{\text{RSTOUT}}$ is asserted. It must stop driving the data bus pins within one FB_CLK cycle after $\overline{\text{RSTOUT}}$ is negated. To prevent contention with the external reset override circuitry, the reset override pins are forced to inputs during reset and do not become outputs until at least one FB_CLK cycle after $\overline{\text{RSTOUT}}$ is negated.

1.3 Serial Configuration

The serial configuration mode provides the most flexibility and configurability of the MCF5445*x* at reset. If the BOOTMOD pins are 2'b11 during reset, the MCF5445*x* is configured according to the data obtained from an external SPI memory through serial boot using the SBF_DI, SBF_DO, $\overline{\text{SBF\_CS}}$, and SBF_CK signals. (See Table 6.) Many of the PCI Type 0 configuration registers (PCI device ID, etc.) can only be overridden by serial configuration mode. If the other modes are used, then the system must use the default values. They cannot be changed, even at run-time.

Table 6. Serial Configuration During Reset

Override Serial RCON Bits	Function
SBF_RCON[127:126]	**Boot Port Size**
11	0-bit port (FB_AD[31:0] configured for GPIO)
10	8-bit port
01	16-bit port
00	32-bit port
SBF_RCON[125]	**PCI and FlexBus A/D Pin Mode (360-pin Devices)**
1	PCI disabled FlexBus non-muxed address/data mode

Table 6. Serial Configuration During Reset (continued)

Override Serial RCON Bits	Function
0	PCI enabled FlexBus muxed address/data mode
SBF_RCON[124]	**Oscillator Mode**
1	Oscillator bypass mode
0	Crystal oscillator mode
SBF_RCON[123]	**Bus Monitor Enable**
1	Bus monitor enabled
0	Bus monitor disabled
SBF_RCON[122:120]	**Bus Monitor Timeout (FB_CLK Cycles)**
000	65536
001	32768
010	16384
011	8192
100	4096
101	2048
110	1024
111	512
SBF_RCON[119:112]	**PLL Reference Clock Multiplier** This is the value loaded into the PCR[PFDR] field
SBF_RCON[111]	**PLL Mode**
1	Limp mode
0	PLL mode
SBF_RCON[110]	**Timer/SSI DMA Channel Mux Select**
1	Timer 0-3 DMA signals mapped to DMA channels 9-12, respectively
0	SSI RX0, SSI RX1, SSI TX0, SSI TX1 DMA signals mapped to DMA channels 9-12, respectively
SBF_RCON[109]	**USB Clock Source**
1	PLL drives USB serial interface clocks
0	USB_CLKIN pin drives USB serial interface clock
SBF_RCON[108]	**USB VBUS Overcurrent Sense Polarity**
1	USB_VBUS_OC is active-high

Table 6. Serial Configuration During Reset (continued)

Override Serial RCON Bits	Function
0	USB_VBUS_OC is active-low
SBF_RCON[107]	**SSI RXD/TXD Pull Enable**
1	SSI_RXD,SSI_TXD pull cells enabled
0	SSI_RXD,SSI_TXD pull cells disabled
SBF_RCON[106]	**SSI RXD/TXD Pull Select**
1	SSI_RXD,SSI_TXD pulled high
0	SSI_RXD,SSI_TXD pulled low
SBF_RCON[105]	**SSI Clock Source**
1	PLL drives SSI clock
0	SSI_CLKIN pin drives SSI clock
SBF_RCON[104]	**PCI Pad Slew Rate Mode (360-pin Devices)**
1	66 MHz slew rate mode
0	33 MHz slew rate mode
SBF_RCON[103]	**PCI Interrupt (360-pin Devices)**
1	PCI interrupt enabled
0	PCI interrupt disabled
SBF_RCON[102]	**PCI Configuration Retry (360-pin Devices)**
1	PCI configuration retry enabled
0	PCI configuration retry disabled
SBF_RCON[101]	**PCI BAR5 Enable (360-pin Devices)**
1	BAR5 enabled
0	BAR5 disabled
SBF_RCON[100]	**PCI BAR4 Enable (360-pin Devices)**
1	BAR4 enabled
0	BAR4 disabled
SBF_RCON[99]	**PCI BAR3 Enable (360-pin Devices)**
1	BAR3 enabled
0	BAR3 disabled
SBF_RCON[98]	**PCI BAR2 Enable (360-pin Devices)**
1	BAR2 enabled

Table 6. Serial Configuration During Reset (continued)

Override Serial RCON Bits	Function
0	BAR2 disabled
SBF_RCON[97]	**PCI BAR1 Enable (360-pin Devices)**
1	BAR1 enabled
0	BAR1 disabled
SBF_RCON[96]	**PCI BAR0 Enable (360-pin Devices)**
1	BAR0 enabled
0	BAR0 disabled
SBF_RCON[95:80]	**PCI Device ID (360-pin devices)**
SBF_RCON[79:64]	**PCI Vendor ID (360-pin devices)**
SBF_RCON[63:40]	**PCI Class Code (360-pin devices)**
SBF_RCON[39:32]	**PCI Revision ID (360-pin devices)**
SBF_RCON[31:16]	**PCI Subsystem ID (360-pin devices)**
SBF_RCON[15:0]	**PCI Subsystem Vendor ID (360-pin devices)**

2 Boot Options

In conjunction with the configuration mode options, the MCF5445*x* devices offer two booting methods: from a parallel memory device on the FlexBus interface, or from a serial (SPI) memory device via the serial boot facility. The boot mode is selected by the BOOTMOD[1:0] pins (see Table 7) and, when in serial configuration mode, the BLL field.

Table 7. Configuration and Boot Modes

BOOTMOD[1:0]	Meaning
00	Boot from FlexBus with defaults
01	Reserved.
10	Boot from FlexBus with parameters determined by FB_AD[7:0]
11	Boot from either FlexBus or SPI memory with parameters determined by data read from SPI memory

2.1 Boot from FlexBus

This boot mode is selected when the BOOTMOD[1:0] signals are driven to either 2’b00 or 2’b10 during reset. This is the classic ColdFire boot method. In this mode, the device connected to $\overline{\text{FB\_CS0}}$ is the boot device where the initial stack pointer and program counter are loaded. A minimal amount of initialization code, enough to initialize another peripheral interface for instruction code retrieval, must also be in the

boot device. Refer to the ColdFire core chapter's "Reset Exception" section and Flexbus's "Global Chip-Select Operation" section of the *MCF54455 Reference Manual* for more details.

2.2 Boot from SPI Memory

Using serial configuration mode requires that an external SPI memory is loaded with data prior to reset as shown in Table 8. The second and third data bytes in the SPI memory specify the boot code length (boot load length, BLL). If this value is zero, the MCF5445*x* defaults to the FlexBus boot method. However, if the BLL is non-zero, the serial boot facility reads boot code from the SPI memory device into the MCF5445*x*'s on-chip SRAM. After the data is loaded, the processor's reset exception is allowed to proceed. This is identical to the other boot method except that, in this case, the initial program counter, stack pointer, and initialization code are read from the on-chip SRAM instead of an external FlexBus device. Refer to the "Serial Boot Facility" chapter of the *MCF54455 Reference Manual* for more details on serial boot.

Table 8. SPI Memory Organization

Byte Address	Data Contents
0x0	{0000,BLDIV[3:0]}
0x1	BLL[7:0]
0x2	BLL[15:8]
0x3	RCON[7:0]
0x4	RCON[15:8]
...	...
0x12	RCON[127:120]
0x13[1]	CODE_BYTE_0[2]
0x14[1]	CODE_BYTE_1
...	...
0x12 + 4 × (BLL + 1)[1]	CODE_BYTE_[4 × (BLL + 1) - 1]

1 This assumes BLL ≠ 0. If BLL equals 0, the SBF does not access data at these addresses.

2 Start of the user code that is copied into the on-chip SRAM.

Using serial boot mode can help reduce the overall system cost by reducing or removing the need for an external non-volatile parallel memory device. For example, consider a system with an external HDD on the ATA interface or an external PCI device that contains a system boot image. In this case, the boot code in the SPI memory device need only initialize the appropriate interface and load the boot image from that device.

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