Freescale Semiconductor
Application Note

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Rev. 0, 07/2009

MPC8548E Version 2.1.x Changes

Changes in Silicon from Version 2.0 to Version 2.1.x

The MPC8548E Version 2.1.x silicon incorporates changes to fix known errata and address expanded capabilities. Silicon changes with respect to particular erratum fixes are addressed separately in the *Device Errata for the MPC8548E PowerQUICC™ III Processor* (MPC8548ECE) document for the MPC8548E family of devices.

The purpose of this document is to highlight, block by block, any other changes or enhancements in the Version 2.1.x device different from the Version 2.0 silicon.

Contents

1 Processor and System Version

Table 1 provides a cross-reference to match the revision level to the processor version register (PVR) and the system version register (SVR) to the revision level marked on the device. Software that uses the PVR or the SVR must take into account the changes in these values with silicon version 2.1.x.

Table 1. Revision Level to Part Marking Cross-Reference

MPC8548/E Revision	e500 v2 Core Revision	Processor Version Register Value	System Version Register Value	Device Marking
2.0	2.0	0x8021_0020	With security 0x8039_0020 Without security 0x80310020	2M39E 3M39E
2.1.1	2.2	0x8021_0022	With security 0x8039_0021 Without security 0x80310021	6M39E
2.1.2	2.2	0x8021_0022	With security 0x8039_0021 Without security 0x80310021	7M39E

2 Errata Addressed in Version 2.1

Table 2 details the errata that were addressed in the MPC8548E Version 2.1.x. Unless noted, all the errata in the table can be left in place for use with Version 2.1.x silicon. For more details on a particular erratum, please refer to the current revision of the *Device Errata for the MPC8548E PowerQUICC™ III Processor.*

Table 2. Errata fixed in Version 2.1.x Silicon

Erratum	Description	Disposition	Notes
CPU 2	A core hang possible while executing a *msync* or *mbar 0* instruction and a snoopable transaction from an I/O master tagged to make quick forward progress is present	Fixed in Ver. 2.1.x	—
DDR 15	Automatic calibration hardware may calibrate to an invalid driver impedance	Fixed in Ver. 2.1.x	1
DDR 16	On-die termination at the DDR IOs has been measured 75 Ω too high	Fixed in Ver. 2.1.x	2
DDR 17	DDR performance monitoring and tracing functionality does not work	Fixed in Ver. 2.1.x	—
DDR 19	DDR IOs default receiver biasing may not work across voltage and temperature	Fixed in Ver. 2.1.x	3
eTSEC 36	TX_EN of may be driven randomly during reset	Fixed in Ver. 2.1.x	—
eTSEC 37	eTSEC Parser does not properly parse L3 fields	Fixed in Ver. 2.1.x	—
eTSEC 44	FIFO8, FIFO16 TX hang	Fixed in Ver. 2.1.x	—
eTSEC 45	Tx Data Corruption in FIFO16 mode	Fixed in Ver. 2.1.x	—

Table 2. Errata fixed in Version 2.1.x Silicon (continued)

Erratum	Description	Disposition	Notes
eTSEC 46	RSTAT[RXF0] set regardless of destination ring if WWR=0	Fixed in Ver. 2.1.x	—
eTSEC 49	Tx IP and TCP/UDP Checksum Generation not supported for some Tx FCB offsets	Fixed in Ver. 2.1.x	—
eTSEC 52	Error in arbitrary extraction offset	Fixed in Ver. 2.1.x	—
eTSEC 55	Transmit jumbo frames greater than 2400 bytes may cause lost data, loss of BD synchronization, or false underrun error	Fixed in Ver. 2.1.x	—
eTSEC 56	Parser results may be lost if TCP/UDP checksum checking is enabled	Fixed in Ver. 2.1.x	—
eTSEC 59	Arbitrary Extraction on Short Frames Uses Data From Previous Frame	Fixed in Ver. 2.1.x	—
eTSEC 60	Some combinations of Tx packets may trigger false Data Parity Error (DPE	Fixed in Ver. 2.1.x	—
eTSEC 61	eTSEC Data Parity Error (DPE) does not abort transmit frames	Partial Fix in Ver. 2.1.x	—
eTSEC 75	Back-to-back Rx frames may lose parser results of second frame	Fixed in Ver. 2.1.x	—
eTSEC 86	eTSEC receivers may not be properly initialized	Fixed in Ver. 2.1.x	—
JTAG 2	eTSEC receivers may not be properly initialized	Fixed in Ver. 2.1.x	—
GEN1	Some pins do not meet 500V CDM ESD criteria	Improvements for Ver. 2.1.x	—
PCI 6	PCI/PCI-X erroneous error detection	Fixed in Ver. 2.1.x	—
PCI 7	Asynchronous mode PCI1 and PCI2 input hold violation	Fixed in Ver. 2.1.x	—

Note:
1. Refer to Section 2.1, “Removing the DDR-15 Workaround.”
2. Refer to Section 2.2, “Difference in ODT Value per DDR-16.”
3. Refer to Section 2.3, “Removing the DDR-19 Workaround.”

2.1 Removing the DDR-15 Workaround

The DDR-15 erratum workaround should be removed if hardware calibration is needed. However, there is no negative impact if the workaround is not removed.

2.2 Difference in ODT Value per DDR-16

As stated in the DDR16 erratum disposition, the DDR-16 erratum version 2.1.x silicon gives the correctly stated termination values in the DDR I/Os, different from Version 2.0 silicon. Depending on the desired on-die termination, DDRCDR[ODT] may need to be updated.

2.3 Removing the DDR-19 Workaround

As stated in the DDR-19 erratum disposition, the workaround of writing to CCSR offset 0xE_0F24 with a value of 0x9000_0000 for DDR2 and a value of 0xA800_0000 for DDR1 before enabling the DDR controller must be removed when running a Version 2.1 device. The Version 2.1.x fix swapped the bit settings in this internal register at CCSR offset 0xE_0F24. If the workaround for the Version 2.0 device is

implemented on the Version 2.1.x device, the user will in effect have reset the DDR receiver bias point back to the failing value.

3 Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	07/2009	Initial public release.

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