MPC8568E Design Checklist

This application note describes the general recommendation for new designs based on the Freescale Semiconductor MPC8568E processor family. These devices include the following:

- MPC8568E
- MPC8568
- MPC8567E
- MPC8567

It may also serve as a useful guide to debug a newly designed system by highlighting those areas of a design that merit special attention during initial system startup.

To locate any published errata or updates for this document, visit the website at http://www.freescale.com.

Contents

1 Introduction

This section outlines recommendations to simplify the first phase of design. Before designing a system with a PowerQUICC™ III device, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

1.1 References

Note that some of the references below may only be available under a Non-Disclosure Agreement (NDA). For those documents, contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - *MPC8568E PowerQUICC III Integrated Host processor Family Reference Manual*. It includes two parts: Platform manual MPC8568ERM and QUICC Engine manual QERM.
  - *MPC8568E PowerQUICC III Family Device Errata* (MPC8568ECE)
  - *MPC8568E Integrated Host Processor Hardware Specifications* (MPC8568EEC)

    Note: MPC8568E and MPC8567E shares the Device Errata and Hardware Specification documents.
- Available tools:
  - QE utility tool
  - Boot sequencer generator tool
  - UPM programming tool
- Models:
  - IBIS
  - BSDL

1.2 Device Errata

The device errata document (MPC8568ECE) describe the latest fixes and work-arounds for the MPC8568E family and should be thoroughly researched prior to starting a design.

1.3 Product Revisions

Table 1 provides the product revisions.

Table 1. MPC8568E Family PVR and SVR

Device	SVR (Rev 1.1)	PVR (Rev 1.1)
MPC8568E	0x807D_0011	0x8021_0022
MPC8568	0x8075_0011	0x8021_0022
MPC8567E	0x807D_0111	0x8021_0022
MPC8567	0x8075_0111	0x8021_0022

2 Power

This section provides design considerations for the MPC8568E power supplies, as well as power sequencing. For information on AC and DC electrical specifications and thermal characteristics, refer to the MPC8568E Hardware Specification (MPC8568EEC).

2.1 Power Supply

Refer to the MPC8568E Hardware Specification (MPC8568EEC) for the recommended and maximum range for each power supply. No external signals on MPC8568E are 5-V-tolerant. Note that absolute maximum ratings are stress ratings only, the functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

LV_{DD} is used to supply the eTSEC1 and eTSEC2 interfaces on the device. TV_{DD} supplies UCC1/UCC2 Ethernet interface. For the respective eTSEC or UCC Ethernet, LV_{DD}/TV_{DD} must be 3.3 V for GMII, MII, RMII, or TBI modes of operation, and must be 2.5 V for RGMII, RTBI or FIFO modes of operation. QE Gigabit Ethernet Power on Reset Configuration voltage selection (PA[6]/cfg_ce_vddsel) must match selected UCC operation.

NOTE

As a result, 3.3 V and 2.5 V modes cannot be paired on eTSECs or UCC Ethernet interface. For example, TSEC1 GMII + TSEC2 RGMII is not supported. Similarly, UCC1 GMII + UCC2 RGMII is not supported.

2.2 Power Dissipation

The MPC8568E Hardware Specification (MPC8568EEC) provides the power dissipation of V_{DD} for various configurations of the core complex bus (CCB), QE and the e500 core frequencies. It also provides an estimation of power dissipation of all the IO power rails. Note that IO power highly depends on the application and is just an estimate.

The typical V_{DD} power plus IO power should be used for the thermal solution design. It is required that the junction temperature does not exceed the maximum specified value.

The maximum V_{DD} power is the worst case power consumption. This number is used for the power supply design.

2.3 Power Sequencing

The MPC8568E requires its power rails to be applied in specific sequence to ensure proper device operation. These requirements are as follows for power up:

1. VDD, AVDD_*n*, BVDD, SCOREVDD, LVDD, TVDD, XVDD, OVDD
2. GVDD

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another.

Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs. To guarantee MCKE low during power-up, the above sequencing for GVDD is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, the sequencing for GVDD is not required.

2.4 Power Planes

Each V_{DD} pin should be provided with a low-impedance path to the board's power supply. Similarly, each ground pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on-chip. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and ground should be kept to less than half an inch per capacitor lead.

2.5 Decoupling

Due to large address and data buses and high operating frequencies, the MPC8568E device can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerQUICC III system, and the PowerQUICC III itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, GV_{DD}, LV_{DD}, TV_{DD}, BV_{DD}, XV_{DD}, SCOREVDD, OV_{DD} pin. These decoupling capacitors should receive their power from separate V_{DD}, GV_{DD}, LV_{DD}, TV_{DD}, BV_{DD}, XV_{DD}, SCOREVDD, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors must be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 1 µF, 0.1 µF, 0.01 µF, 1000 pF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. It is recommended that 0402 size capacitors be used.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, GV_{DD}, LV_{DD}, TV_{DD}, BV_{DD}, XV_{DD}, SCOREVDD, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–300 µF.

Simulation is strongly recommended to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.6 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_PCI}, AV_{DD_LBIU}, and AV_{DD_SRDS}, AV_{DD_CE} respectively). The AV_{DD}

level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 1, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of 1023FC-PBGA the footprint, without the inductance of vias.

Figure 1 shows the PLL power supply filter circuits for all PLLs except SerDes PLL.

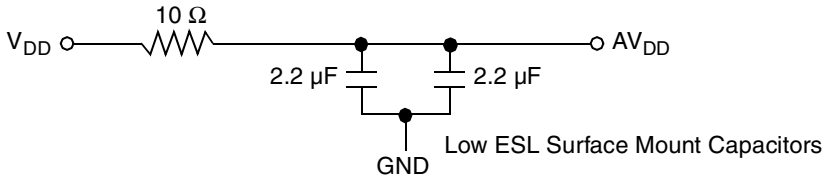
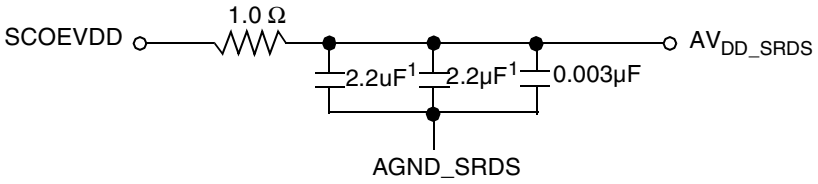


Figure 1. MPC8568E PLL Power Supply Filter Circuit

The AV_{DD_SRDS} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 2. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDS} and AGND_SRDS ball to ensure it filters out as much noise as possible. The 0.003-µF capacitor is closest to the ball, followed by the 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 2. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD_SRDS} should be a filtered version of SCOREVDD.
- The transmitter output signals on the SerDes interface are fed from the XV_{DD} power plan.

- Power: XVDD consumes less than 300 mW. SCOREVDD + AV_{DD_SRDS} consumes less than 750 mW.

2.7 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SCOREVDD and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has through vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board has blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum or ceramic chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

2.8 Power Supplies Checklist

Table 2 provides a summary of the MPC8568E power supply checklist for the designer.

Table 2. Power Supplies Checklist

Item	Description	Completed
1	All power supplies have a voltage tolerance no greater than 5% from the nominal value.	
2	eTSEC/UCC Ethernet supplies are chosen according to the mode of operation used.	
3	Power supply selected is based on MAXIMUM power dissipation.	
4	Thermal design is based on TYPICAL power dissipation.	
5	Power-up sequence is less than 50 ms.	
6	Power sequencing is understood and based on whether or not latch-up or garbage data written to DDR is a concern.	
7	Recommended PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CORE, and AV_{DD}_LBIU.	
8	If PCI is used in asynchronous mode, then the recommended PLL filter circuit is applied to AV_{DD}_PCI.	
9	If SerDes is used, then the recommended PLL filter circuit is applied to AV_{DD}_SRDS.	
10	PLL filter circuits are placed as close to the respective AV_{DD} pin as possible.	
11	Decoupling capacitors of 1 µF, 0.1 µF, 0.01 µF and 1000 pF (should be equally spaced) are placed at each V_{DD}, B/G/L/O/TV_{DD} pin.	

Table 2. Power Supplies Checklist (continued)

Item	Description	Completed
12	Bulk capacitors are placed on each V_{DD}, B/G/L/O/TV_{DD} plane.	
13	If SerDes is used, the recommended decoupling for S/XV_{DD} is used.	

3 Internal Test Modes

Several pins double as test mode enables. These test modes are for internal use only, and if enabled during reset could result in the MPC8568E not coming out of reset. Table 3 lists these pins and how they should be terminated during the reset sequence.

Table 3. Internal Test Mode Pins

Pin Group	Pins	Guideline for Reset
Internal Test	TRIG_OUT/READY	Because these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (for example, by a PLD), if the device to which they are connected does not three-state these pins during reset.
	MSRCID2	
	MSRCID3	
	MSRCID4	
	ASLEEP	
	HRESET_REQ	
	PA[5]	
Design For Test	LSSD_MODE	These pins must be pulled to OV_{DD} via a 100 Ω -1kΩ resistor.
	L1_TSTCLK	
	L2_TSTCLK	
	TEST_SEL	
	THERM0, THERM1	Leave as no connect if not used. These two pins are not ESD protected.

4 System Control/Debug Pins

Table 4 provides the checklist for system control and debug pins.

Table 4. System Control and Debug Pins Checklist

Item	Description
1	$\overline{\text{HRESET}}$: Minimum assertion time is 100 us.
2	SRESET: Minimum assert time is 512 SYSCLKs.
3	$\overline{\text{CKSTP\_IN}}$: It must be pulled up to OVdd with 2-10K resistor.
4	TRIG_IN: It must be tied to GND with 2-10K resistor if not used.
5	$\overline{\text{CKSTP\_OUT}}$: This is an open drain signal. It must be pulled up to OVdd with 2-10K resistor.

5 Power-On Reset Configuration Pins

Various device functions are initialized by sampling certain signals during the assertion of HRESET. The values of all these signals are sampled into registers while HRESET is asserted. These inputs are to be pulled high or low by external resistors. During HRESET, all other signal drivers connected to these signals must be in the high-impedance state. Most POR configuration signals have internal pull-up resistors so that if the desired setting is high, there is no need for a pull-up resistor on the board. Other POR configuration signals do not use pull-ups and therefore must be pulled high or low.

5.1 Reset Configuration Pins Timing Spec

Table 5 provides the timing requirement documented in the MPC8568E Hardware Specification (MPC8568EEC), Section 6, “RESET Initialization.”

Table 5. Reset Timing Requirement

Parameter/Condition	Min	Max	Unit
PLL input setup time with stable SYSCLK before HRESET negation	100	—	us
Input setup time for POR configs (other than PLL config) with respect to negation of HRESET	4	—	SYSCLKs
Input hold time for all POR configs (including PLL config) with respect to negation of HRESET	2	—	SYSCLKs
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of HRESET	—	5	SYSCLKs

Table 6 lists all the POR configuration pins without the internal pull-up resistors and must be driven.

Table 6. Configuration Pins Without Internal Pull-Up Resistors

Functional Interface	Functional Signal Name	Reset Configuration Name	Default
LBC	LA[28:31]	cfg_sys_pll[0:3]	No. Must be driven
	LBCTL	cfg_core_pll0	No. Must be driven
	LALE	cfg_core_pll1	No. Must be driven
	LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	cfg_core_pll2	No. Must be driven

Table 7 lists all the POR configuration pins with the internal pull-up resistors. If the desired functionality is configured with “HIGH,” no pull-up resistor is needed.

Table 7. Configuration Pins With Internal Pull-Up Resistors

Functional Interface	Functional Signal Name	Reset Configuration Name	Default
PCI	PCI_GNT4	cfg_pci_clk	1
	PCI_GNT3	cfg_pci_debug	1
	PCI_GNT2	cfg_pci_arb	1
	PCI_GNT1	cfg_pci_impd	1

Table 7. Configuration Pins With Internal Pull-Up Resistors (continued)

Functional Interface	Functional Signal Name	Reset Configuration Name	Default
QE	PA[0:4]	cfg_ce_pll[0:4]	11111
	PA[6]	cfg_ce_vddsel	1
	PE[8:10]	cfg_io_ports[0:2]	111
	PE[21:23]	cfg_rom_loc[0:2]	111
	PE[24]	cfg_srds_en	1
	PF[8:10]	cfg_device_id[5:7]	111
	PF[21:22]	cfg_dram_type[0:1]	11
Ethernet Management	EC_MDC	cfg_tsec1_reduce	1
TSEC1	TSEC1_TXD7	cfg_tsec1_prtcl1	1
	TSEC1_TXD0	cfg_tsec1_prtcl0	1
	TSEC1_TX_ER	cfg_tsec2_reduce	1
TSEC2	TSEC2_TXD7	cfg_tsec2_prtcl1	1
	TSEC2_TXD0	cfg_tsec2_prtcl0	1
LBC	LA[27]	cfg_cpu_boot	1
	$\overline{\text{LWE}}$[1:3]/$\overline{\text{LBS}}$[1:3]	cfg_host_agt[0:2]	111
	LGPL0/LSDA10	cfg_rio_sys_size	1
	$\overline{\text{LWE}}$[0]/$\overline{\text{LBS}}$[0]	cfg_pci_speed	1
	LGPL3/$\overline{\text{LSDCAS}}$	cfg_boot_seq0	1
	LGPL5	cfg_boot_seq1	1
Debug	MSRCID0	cfg_mem_debug	1
	MSRCID1	cfg_ddr_debug	1

The GPPORCR (offset: 0xE_0020) stores the value sampled from the local bus address/data signals, LAD[0:31], during POR, as described in the applicable Reference Manual, Section 4.4.3.25, “General-Purpose POR Configuration.” Software can use this value to inform the operating system about initial system configuration. Typical interpretations include circuit board type, board ID number, or a list of available peripherals. It can be left open if the software does not use it.

Table 8. LAD[0:31] as Configuration Pins

Functional Interface	Functional Signal Name	Reset Configuration Name	Default
LBC	LAD[0:31]	cfg_gpinput[0:31]	No default. Indeterminate if not driven.

6 Clocking

6.1 Pin Listing and Connections

Table 9 provides the clock signal pin listing.

Table 9. Clock Signal Pin Listing

Signal	Connection		Notes
	if used	if not used	
SYSCLK	System clock	Must be used	It must satisfy the AC timing in MPC8568EEC Section 5.1, “System Clock Timing.”
PCI_CLK	PCI clock if PCI runs in asynchronous mode	Tied to GND if PCI is disabled or PCI runs in synchronous mode	If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK. Otherwise the MPC8568E does not boot up. It must satisfy the AC timing in MPC8568EEC Section 5.2, “PCI Clock Timing.”
RTC	Real time clock input	Tied to GND	RTC is used by e500 time base unit and PIC Global Timers. RTC minimum high time is 2 × tCCB, and minimum low time is 2 × tCCB. There is no minimum RTC frequency.
SD_REF_CLK/ SD_REF_CLK	For x4 3.125Gbps SRIO, it is 125 MHz. For all others, it is 100 MHz. See MPC8568ERM Section 4.4.3.5, “I/O Port Selection” for more details.	Tied to GND	When the interface is used for PCI Express only, SD_REF_CLK and SD_REF_CLK was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30-33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation. If the interface is used for SIRO only or simultaneous SRIO/PCI Express, then the spread spectrum clock cannot be used.

7 Local Bus Controller

7.1 LBC Signal Termination

Table 10 provides the checklist for the local bus.

Table 10. Local Bus Checklist

Item	Description
1	LGPL1 must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ because it has internal pull-up resistor.
2	LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE. This signal is used for terminate GPCM or UPM. If not driven by external logic, it must be pulled up to OVdd with 2-10K resistor. If driven by external logic for LUPWAIT, it must be driven to high for non-UPM cycle. Otherwise it may cause undesired premature termination of non-UPM access (such as flash access)
3	Connect LSYNC_IN to LSYNC_OUT regardless of DLL mode. For DLL bypass mode, LSYNC_IN is not used. Connect to LSYNC_OUT keeps it from floating.
4	If parity is not used, tie LDP[0:3] to ground or the power supply rail via a 4.7K resistor.

Table 10. Local Bus Checklist (continued)

Item	Description
5	The local bus is 32 bits wide. If fewer than 32 bits is needed, for example, flash is 16 bits wide, connect to LAD[0:15] for data and $\overline{\text{LWE}}$[0:1]/$\overline{\text{LBS}}$[0:1] for byte select. ALE is used to latch LAD[0:31] and form the address bus for the memory device, denoted as latch_addr[0:31]. latch_addr[0] is MSB, latch_addr[31] is LSB. For 16-bit memory, latch_addr[31] is no connect. For 32-bit memory, latch_addr[30:31] is no connect.
6	For some RAM devices, LA[27:31] can be used for column address offset for burst access. If no such RAM is used, address latched from LAD[27:31] can be used instead of LA[27:31].

7.2 UPM Programming Tool

The local bus supports three user programmable machines (UPMs), which can be used to generate flexible and complex waveform. Freescale provides this tool to help the user program the controller. It features a GUI for a user-friendly programming interface. The GUI consists of a “wave editor,” “table editor,” and “report generator.” The user can edit directly the waveform or the RAM array. At the end of programming, the “report generator” prints out the UPM ram array that can be used in a C-program.

8 DDR Controller

Table 11 provides the checklist for the DDR controller.

Table 11. DDR Controller Checklist

Item	Description
1	MDIC[0] must be connected to GND with 18.2 Ω 1%. MDIC[1] must be connected to GVDD with 18.2 Ω 1%.
2	For MDQ[0:63], MDQ[0] is the most-significant bit (msb), MDQ[63] is the least-significant bit (lsb). If 32-bit DDR is used, it must be connected to MDQ[0:31]. Unused MDQ may be left unconnected.
3	For MA[0:15], MA[15] is the msb, MA[0] is the lsb. This is the same as the DDR memory convention.

Refer to the following application notes for detailed information on layout consideration and DDR programming guidelines:

- AN2582: *Hardware and layout Design Considerations for DDR Memory Interfaces* for detailed information on signal integrity and layout considerations.
- AN2583: *Programming the PowerQUICC III DDR SDRAM Controller* on DDR programming guidelines.
- AN2910: *Hardware and layout Design Considerations for DDR2 SDRAM Memory Interfaces* for detailed information on signal integrity and layout considerations.

9 PCI Bus

9.1 Checklist if PCI Bus is Used

Table 12 provides the checklist for the PCI bus if it is used.

Table 12. Checklist for PCI Bus

Item	Description
1	Follow the PCI spec for the signal termination.
PCI_AD[0:31]	No need for any pull-up/pull-down resistors
PCI_C/$\overline{\text{BE}}$[3:0]	
PCI_PAR	
PCI_FRAME	A weak pull-up resistor (2–10K) needs to be placed on this pin to OVDD.
PCI_DEVSEL	
PCI_IRDY	
PCI_TRDY	
PCI_STOP	
PCI_PERR	
PCI_SERR	
PCI_IDSEL	For PCI host mode, tied to GND. For agent mode, connected to PCI host.
2	If PCI is configured as asynchronous mode, a valid clock must be provided on pin PCI_CLK. Otherwise the device does not boot up.
3	For PCI speed 33 MHz and above, cfg_pci_speed (LWE0) must be set to 1.
4	Any unused $\overline{\text{PCI_REQ}}$s must be pulled up. Any unused $\overline{\text{PCI_GNT}}$s can be left no connect.

9.2 PCI Termination if PCI is Not Used

Table 13 provides the checklist for PCI bus termination.

Table 13. Unused PCI Bus Termination

Item	Description
1	If MPC8568E PCI bus is disabled but the bus is connected to other PCI devices, it must be configured to select external PCI arbiter to avoid contention.
2	If MPC8568E PCI bus is not connected to any other devices, and PCI arbiter is enabled during POR, PCI_AD[0:31], PCI_C/$\overline{\text{BE}}$[0:3], PCI_PAR pins is driven to the stable states after POR. Therefore, PCI_AD[0:31], PCI_C/$\overline{\text{BE}}$[0:31], PCI_PAR pins can be floating.
3	All PCI control pins can be grouped together and tied to OVdd through a single 10K-Ω resistor. It is optional to disable PCI block through DEVDISR register after POR reset to save power.

10 I²C Controller

Table 14 provides the checklist for I²C interface.

Table 14. I²C Interface Checklist

Item	Description
1	I²C 1 interface: • IIC1_SDA, IIC1_SCL are open drain signals. Tied high to OVdd through 4.7K resistors.
2	I²C 2 interface (IIC2_SDA/PC19, IIC2_SCL/PC18): • I²C 2 pins are muxed with PC18 and PC19 pins. • If those pins are used for I²C 2, they must be programmed as open drain signals and tied high to OVdd through 4.7K resistors. • If I²C 2 is not used, those pins can be programmed as PC pins.

10.1 Boot Sequencer Tool

The MPC8568E features the boot sequencer to allow configuration of any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I²C EEPROM. It requires a particular data format as outlined in the MPC8568ERM. The boot sequencer tool is a C code file.

It must first be compiled. For example,

```
gcc -Wall i2c_bootseq_generator.c -o i2c_bootseq_generator
```

The user then generates a CSV text file with the following format:

```
ACS,BYTE_EN[0:3](hex),ADDR[0:17](hex),DATA[0:31](hex)<newline>
```

where ACS specifies whether to use the default or alternate CCSRBAR, BYTE_EN specifies the DATA[0:31] bytes to be written to the register, ADDR[0:17] specifies the CCSRBAR register offset, and DATA[0:31] specifies the register data. Refer to the I²C chapter of the applicable Reference Manual for additional details on these parameters.

Finally, the “i2c_bootseq_generator” executable is executed as follows:

```
i2c_bootseq_generator <input file> [output file]
```

It generates appropriate S-record file to be used to program the EEPROM.

11 eTSEC

Table 15 provides the checklist for eTSEC interface.

Table 15. eTSEC Blocks Design Checklist

Item	Description
1	TSEC1_TX_EN, TSEC2_TX_EN needs an external 4.7K pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.
2	MDIO must be pulled up with 2-10K resistor to OVdd.

Table 15. eTSEC Blocks Design Checklist (continued)

Item	Description
3	If the interface is not used: • All the input signals (TSECx_RX[7:0], TSECx_RX_ER, TSECx_RX_DV, TSECx_RX_CLK, TSECx_COL, TSECx_CRS, TSECx_TX_CLK) must be tied to GND. • All the output signals (TSECx_TX[7:0], TSECx_TX_EN, TSECx_TX_ER, TSECx_GTX_CLK) may be left unconnected.
4	EC_GTX_CLK125 must be connected to 125 MHz reference clock.
5	For MII interface, TSECx_RX[7:4] is not used. They must be tied to GND. TSECx_TX[7:3] may be left unconnected.

12 PIC

Table 16 provides the checklist for PIC interface.

Table 16. PIC Checklist

Item	Description
1	Unused IRQ[0:7] must be driven to inactive state. Note the polarity of IRQs is programmable via EIVPRx[P].
2	$\overline{\text{MCP}}$ must be pulled up if not used.
3	$\overline{\text{UDE}}$ must be pulled up if not used.
4	If IRQ8/PC11, IRQ9/$\overline{\text{DMA\_DREQ3}}$/PC12, IRQ10/$\overline{\text{DMA\_DACK3}}$/PC13, IRQ11/$\overline{\text{DMA\_DDONE}}$/PC14 are not used as IRQ pins, they may be programmed as PC port to avoid termination.
5	$\overline{\text{IRQ\_OUT}}$ is an open drain signal; it must be tied to OVdd with 4.7K resistor.

13 SerDes (SRIO and PCI Express)

Table 17 provides the checklist for SerDes.

Table 17. SerDes Checklist

Item	Description
1	Tie any unused SD_RX[7:0]/$\overline{\text{SD\_RX}}$[7:0] to GND.
2	Tie $\overline{\text{SD\_RX\_FRMCTL}}$ and $\overline{\text{SD\_RX\_CLK}}$ with 300 Ω to GND.
3	Tie SD_IMP_CAL_TX with 100 Ω to GND.
4	Tie SD_IMP_CAL_RX with 200 Ω to GND.
5	Any unused SD_TX[7:0]/$\overline{\text{SD\_TX}}$[7:0] may be left unconnected.
6	SD_PLL_TPA, SD_PLL_TPD must be left unconnected.

14 DUART Interface

Table 18 provides the checklist for DUART interface.

Table 18. DUART Checklist

Item	Description
1	UART0: • UART_SIN0/PCI_REQ[4] • UART_SOUT0/PCI_GNT[4] • UART_CTS0/PCI_REQ[3] • UART_RTS0/PCI_GNT[3] Assume it is programmed as UART0 interface (via PMUXCR register). If handshake signals are not used, tie UART_CTS0 to GND, leave UART_RTS0 no connect.
2	UART1: • UART_SIN1/PC3/PC31 • UART_SOUT1/PC0/PD28 • UART_CTS1/PC2/PD30 • UART_RTS1/PC1/PD29 If UART1 is not used, they can be used as PC or PD ports. No termination is needed. Similarly, if UART1 is used but handshake is not needed, program them as PC/PD to avoid termination.

15 DMA Interface

Table 19 provides the checklist for DMA interface.

Table 19. DMA Interface Checklist

Item	Description
1	DMA_DACK[0] must be tied to GND with 4.7K resistor for MPC8567E. It is no connect for 8568/E
2	If DMA0 is not used, DMA_REQ[0] should be tied to OVdd with 4.7K resistor. DMA_ACK[0] and DMA_DONE[0] are output and can be left floating.
3	DMA1 signals are muxed with PC[15:17]. DMA2 signals are muxed with LCS[5:7]. DMA3 signals are muxed with PC[12:14]. If DMA1-3 is not used, they can be used as corresponding alternate function pins.

16 QUICC Engine Communication Interfaces

16.1 QE Utility Tool

QE utility tool may be used to configure the device pins for the desired functionality. The output of the tool is the values for the registers that control the pin multiplexing.

QE utility tool includes three tools:

- Pin mux tool
- QE driver API tool

- QE performance calculator

QE performance calculator needs a license to run.

16.2 QE Interfaces

16.2.1 UCC Ethernet Interface

Table 20 provides the checklist for UCC Ethernet interface.

Table 20. UCC Ethernet Checklist

Item	Description
1	UCC1 Ethernet and UCC2 2 Ethernet share the same power supply TVDD. This puts the limitation on the interface choices. For example, UCC1 GMII and UCC2 RGMII is not supported because GMII requires 3.3 V while RGMII requires 2.5 V.
2	The third Gigabit Ethernet interface on the QUICC Engine block must be assigned to the UCC4 and must use the GMII. UCC4 can also use the RMII and MII for the 10/100 operation.
3	QE Gigabit Ethernet Power on Reset Configuration voltage selection (PA[6]/cfg_ce_vddsel) must match selected UCC1 and UCC2 operation.
4	Program GUMR[MODE] to Ethernet mode. Then configure the QE port pin.
5	For 1000Mbps operation, 125Mhz reference clock, which is typically from PHY device, must be provided to the corresponding UCC TX_CLK. For example, for UCC1, 125Mhz clock can be connected to PB[31]. Configure PB[31] to function as CLK16, and in CMXUCR1 register, configure transmit clock as CLK16.

17 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1™ specification, but is provided on all processors that implement Power Architecture™. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

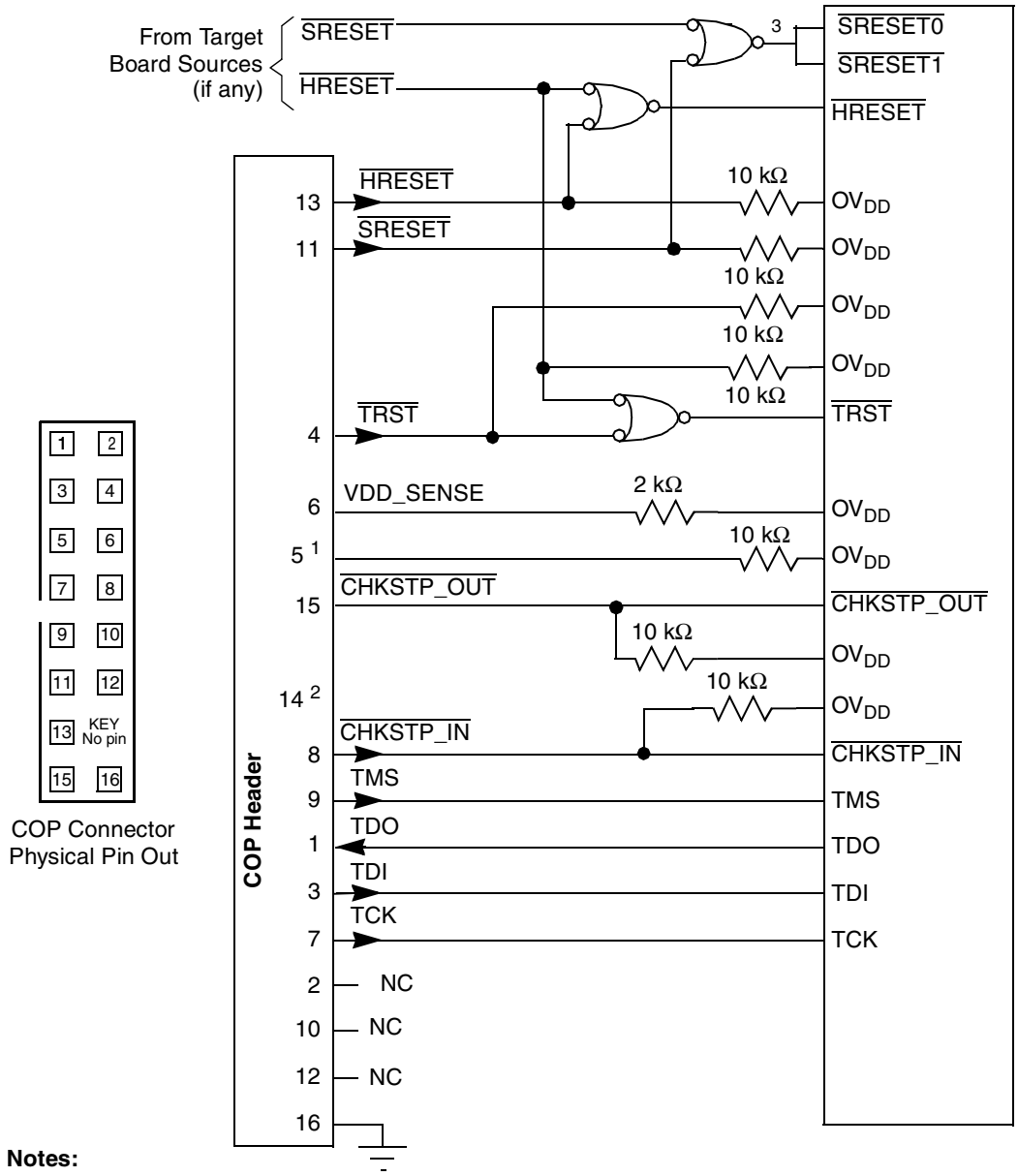
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 3 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header is not used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted.

The COP header shown in Figure 3 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 3; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 3 is common to all known emulators.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Use a NOR gate with sufficient drive strength to drive two inputs.

Figure 3. JTAG Interface Connection

18 Heatsink Attachment

Table 21 provides the checklist for heatsink attachment.

Table 21. Heatsink Attachment

Item	Description
1	The heatsink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

19 Revision History

Table 22 provides a revision history for this application note.

Table 22. Document Revision History

Revision Number	Date	Substantive Change(s)
1	12/1/2008	Update Section 16.2.1, “UCC Ethernet Interface”. Add PA[5] to Section Table 3., “Internal Test Mode Pins”.
0	1/30/2008	Initial release.

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