MSC8157/8 Design Checklist

This application note identifies resources and provides guidance for developing applications using the MSC8157/8 DSP devices. It includes a check list for design phases of projects that incorporate the MSC8157/8 DSPs, including:

- *Definition phase*. This document highlights MSC8157/8 design requirements, such as pin multiplexing, reset timing, and other design considerations.
- *Design implementation phase*. This document reviews relevant issues for schematic development and testing.

NOTE

The MSC8157/8 family includes the following products:

— MSC8157
— MSC8157E
— MSC8158
— MSC8158E

Contents

1 Background

Developing a project that integrates one or more MSC8157/8 devices requires planning that identifies:

- The specific interfaces required for the design.
- How the interfaces are used including whether the interfaces use dedicated signal lines or must share signal lines during device initialization and/or operation (signal multiplexing).
- How the device is initialized/booted during normal operation.

After identifying the high-level system requirements, the designer must define the following hardware requirements:

- Basic power system
- Clocking system
- Reset/initialization system
- Power-up/start-up sequencing system
- Required memory and memory interface system
- Interface connections
- Disposition of unused signal connections to minimize power consumption.

To support the hardware configuration, the designer must also provide software (not discussed in this document) to support device operation, including:

- Device initialization software (reset sequence, booting, and interface setup).
- Interrupt service routines (ISRs) to handle normal DSP core intervention tasks and error interrupts/exceptions.
- Protocol-defined data management and processing software (which may include standard Ethernet frame processing or any of several vocoder implementations, security algorithms for security-enabled devices, and so forth).
- Other software, such as power-management and reporting or overall process management, as required.

The device specific reference manual and core subsystem reference manuals supply the configuration programming information required to develop the application-specific system environment as well as data transfer management and coprocessor execution. The core reference manual provides detailed programming information required to develop the application-specific algorithm core processing software including ISR processing. Support can be provided or recommended by Freescale Semiconductor. Contact your local sales office or representative for additional information.

2 Supporting Documentation

The MSC8157/8 devices are supported by the following types of documentation:

- *Product brief*. Device specific document that includes a high-level description of critical performance metrics, detailed lists of product features, and an overview of available hardware and software development environment tools.
- *Data sheet*. Device specific document that provides a general description of product features, functional block diagrams, signal/pin assignment for the device packaging, detailed physical and electrical specifications including operating parameter values, general hardware design guidelines, ordering information, and detailed packaging specifications.
- *Reference manuals*. Each device is supported by four reference manuals:
  - *Device specific reference manual*. Includes detailed information about the device for each module/subsystem with specific programming models to allow configuration, programming, and operation monitoring. In addition, this document describes device level functionality including interrupt processing and debugging.
  - *SC3850 DSP Core Reference Manual*. Includes a detailed description of core functionality and operation including the core instruction set programming.
  - *SC3850 DSP Core Subsystem Reference Manual*. Includes a detailed description and programming information for the memory management unit (MMU), extended programmable interrupt controller (EPIC), and internal memories (including cache memories) supported in each subsystem.
  - *QUICC Engine Block Reference Manual with Protocol Interworking*. Includes a detailed description and programming information for the QUICC Engine subsystem including the dual RISC processors, internal memory, communication controllers and interfaces, baud rate generators and counters, and lists which components in this subsystem are used by the MSC8157/8 DSPs.
- *Application notes*. Individual documents that provide specific recommendations and guidelines for configuration and operation of the device for specific applications or for specific interface enablement and optimization.

NOTE

Before starting an application design, refer to the latest device errata document for the corresponding device, currently available under NDA. Contact your local sales office or representative for details.

3 Power Supply Requirements

The following sections discuss the various aspects to consider for power supply selection and design.

3.1 Power Supply and Ground Inputs

Each MSC8157/8 device requires the power supplies and grounds listed in **Table 1**. Refer to the device specific technical data sheet for minimum and maximum voltage levels.

Table 1. MSC8157/8 Power Inputs

Signal Name	Symbol	Description	Nominal Voltage
POWER			
VDD	V_{DD}	Core supply voltage	1.0 V
PLL0_AVDD PLL1_AVDD PLL2_AVDD	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	System PLL supply voltage	
M3VDD	V_{DDM3}	Power for the upper 2 MB of M3 memory. Power can be disabled and 1 MB of M3 memory remains active.	
CPRIVDD	V_{DDCPRI}	CPRI supply voltage. Power can be disabled.	
CRPEVDD	V_{DDCRPE}	CRPE supply voltage. Power can be disabled.	
MAVDD	V_{DDPLLM}	DDR PLL supply voltage	
SXCVDD	V_{DDSXC}	SerDes core supply voltage	
SD_PLL1_AVDD SD_PLL2_AVDD	V_{DDPLL}	SerDes PLL supply voltage	
SXPVDD	V_{DDSXP}	SerDes pad voltage	1.5 V
GVDD	V_{DDDDR}	DDR memory supply voltage	
MVREF	MV_{REF}	DDR reference voltage	= GVDD x 0.5 V
NVDD	V_{DDIO}	RGMII and GPIO supply voltage	2.5 V
QVDD	V_{DDIO}	I/O clocks, reset, and JTAG supply voltage	
GROUND			
VSS	GND	System Ground	0 V
SD_PLL1_AGND SD_PLL2_AGND	GND_{SDPLL1} GND_{SDPLL2}	SerDes PLL 1 and 2 Ground	
SXCVSS	GND_{SXC}	SerDes Core Ground	
SXPVSS	GND_{SXP}	SerDes Pad Ground	

3.2 Unused Power Supplies

Some applications which do not use some of the device modules can minimize power consumption by not activating the power supply. **Table 2** summarizes the connection for unused power supply signals.

- If the CPRI is not used, CPRIVDD can be tied to GND.
- If the MAPLE-B2 CRPE is not used, CRPEVDD can be tied to GND.
- If the upper 2048 KB of M3 memory is not used, M3VDD can be tied to GND. The other 1024 KB of M3 memory remains active.
- If the DDR interface is not used, GVDD and MVREF can be left unconnected.

Table 2. Unused Module Supply Signals

Module	Signal Name	Connection
CPRI	CPRIVDD	GND
CRPE	CRPEVDD	GND
M3 2048 KB	M3VDD	GND
DDR Controller	MVREF, GVDD	NC

3.3 Power Supply Decoupling

When developing a specific board design, include decoupling capacitors to minimize noise propagation and maintain proper power levels. It is very important that particular attention is paid to decoupling for the supplies for the PLL circuits to minimize radiated emissions and promote stable frequency generation and clocking. Refer to **Section 3.4**, *Global PLL Power Supply Design Considerations* and **Section 3.5**, *SerDes PLL Power Supply Design Considerations* for decoupling guidelines for the global PLL and SerDes PLL power circuits. As a reference, one can review the schematic design of the MSC8157/8ADS, available under NDA from Freescale. The ADS board design includes:

- Bulk capacitors for V_{DD}. The bulk capacitors decrease low frequency voltage spikes on V_{DD}. In the case of the MSC8157/8ADS board, seven 150 µF capacitors are placed close to the MSC8157/8 device as shown in **Figure 1**.

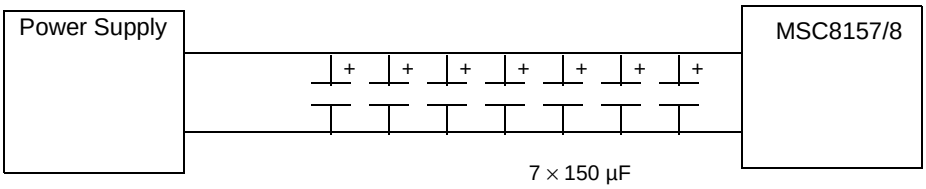


Figure 1. Bulk Capacitors Placement for MSC8157/8

- Bulk Capacitors for V_{DDDDR}. Two 47 µF bulk capacitors are placed on V_{DDDDR} in the MSC8157/8ADS to decrease low frequency voltage spikes.
- Bulk Capacitor for V_{DDM3}. One 47 µF bulk capacitor is placed on V_{DDM3} in the MSC8157/8ADS to decrease low frequency voltage spikes.
- Bulk Capacitor for V_{DDCPRI}. One 47 µF bulk capacitor is placed on V_{DDCPRI} in the MSC8157/8ADS to decrease low frequency voltage spikes.

- Bulk Capacitor for V_{DDCRPE}. One 47 µF bulk capacitor is placed on V_{DDCRPE} in the MSC8157/8ADS to decrease low frequency voltage spikes.
- Bypass Capacitors for all power supplies on the MSC8157/8ADS. 0.01 µF, 0.1 µF, 1 µF, 4.7 µF with low ESR/ESL are used for filtering high frequency noise.
- **Figure 2** shows the SerDes core SXCVDD and pad SXPVDD filter circuits. The SXCVSS and SXPVSS can be joined to a low noise, solid reference ground plane. It is recommended that noise coupling simulation be performed on actual PCB design implementation. The target noise specification is:
  - Maximum noise on SerDes core (SXCVDD, SXCVSS) and SerDes pad (SXPVDD, SXPVSS) supply is 15 mV peak-to-peak

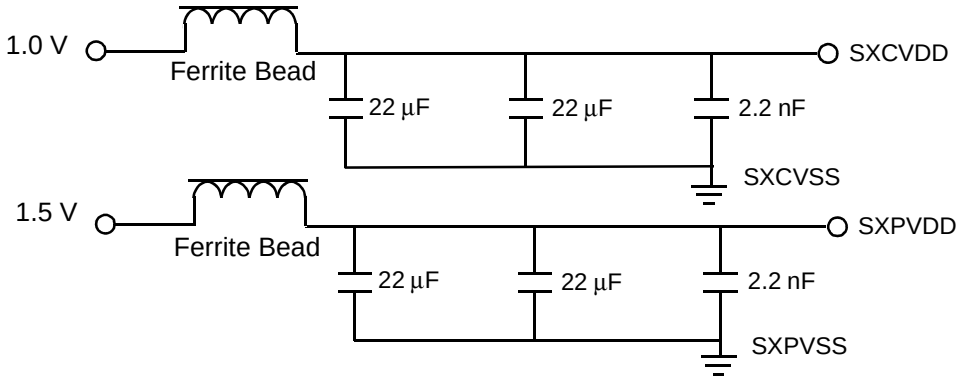


Figure 2. SXCVDD and SXPVDD Supplies

3.4 Global PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLL*n*_AVDD input (see **Figure 3**) where:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change. All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to PLL*n*_AVDD inputs.

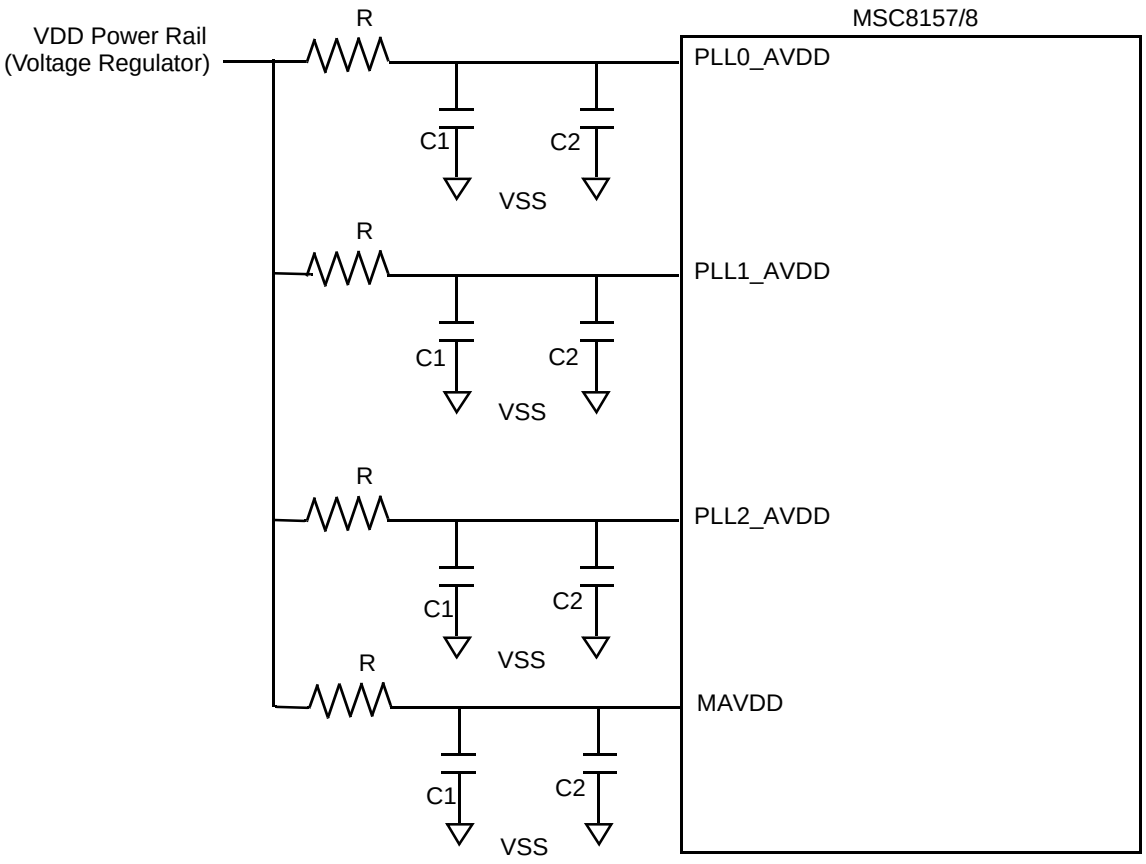


Figure 3. PLL Supplies

3.5 SerDes PLL Power Supply Design Considerations

The SerDes PLL power supply must be filtered using a circuit similar to the one shown in **Figure 4** to ensure stability of the internal clock. All traces should be kept short, wide and direct. Use separate islands/wide traces for each PLL bank's SD_PLL*n*_AVDD and SD_PLL*n*_AGND connections. The ground islands/wide traces of individual PLL banks should be joined to a single ground plane either through an inductor or through a zero-ohm resistance. While it is possible to connect the power islands together to a single supply via a resistor or a ferrite bead, it is recommended to have multiple power islands as close to the source and as far away from the DSP as possible. Do not place any digital or other bank traces near the PLL power and ground planes.

For maximum effectiveness, the filter circuit should be placed as close as possible to the SD_PLL*n*_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SD_PLL*n*_AGND ball. To provide effective bypass capacitance at high frequencies, these two islands/wide traces should be directly over each other and on the nearest PCB layer, that is, layers 3 and 4 of a 6 layer board. The capacitors are connected from the SD_PLL*n*_AVDD to the ground plane. Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to reduce inductance further. The 2.2 nF capacitor is placed closest to the package pin, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane.

The capacitors are connected from SD_PLL*n*_AVDD to the ground plane. The 2.2 nF decoupling capacitor should be within about 0.5 cm of each power pin. The target noise specification is:

- Maximum noise on SerDes PLL (SD_PLL*n*_AVDD, SD_PLL*n*_AGND) is 25 mV peak-to-peak

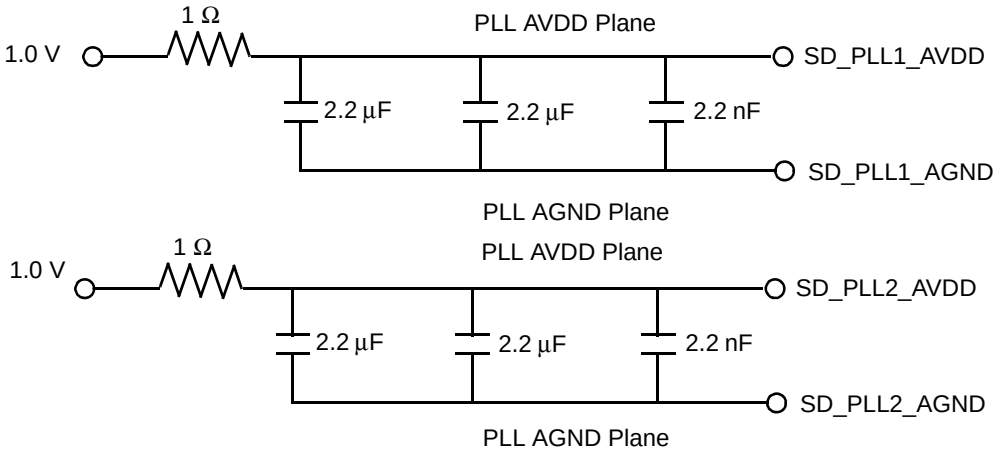


Figure 4. SerDes PLL Supply

3.6 DDR PLL Power Supply Design Considerations

The DDR PLL power supply must have an external RC filter for the MAVDD input (see **Figure 3**) where:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change. For optimal noise filtering, place the circuit as close as possible to the MAVDD inputs.

3.7 Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD:* G7, H18
- *VSS:* H7, H17, AB13

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Power-Up Sequence

The following sections describe the required device initialization sequence.

4.1 Power Supply Coupling and Sequence

Use the following guidelines for coupling the power supplies:

- Couple the M3VDD, CPRIVDD and CRPEVDD with the VDD power rail using an extremely low impedance path.
- Couple the PLL0_AVDD, PLL1_AVDD, PLL2_AVDD and MAVDD with the VDD power rail using an RC filter as shown in **Figure 3**.
- Couple inputs SD_PLL*n*_AVDD with SXCVDD power rail respectively using an RC filter as shown in **Figure 4**.
- Since MVREF = 0.5 * GVDD, see step 2 of the power-on sequence of the power rails below.

External voltage applied to any input line must not exceed the I/O supply voltage related to this line by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8157/8 device in the system during power-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

The device power rails should rise in the following sequence as shown in **Figure 5**:

1. VDD and all coupled 1.0 V supplies (M3VDD, CPRIVDD, CRPEVDD, PLL0_AVDD, PLL1_AVDD, PLL2_AVDD, MAVDD)
2. After the above supplies rise to 90% of their nominal value, the following I/O power rails may rise in any sequence: QVDD, NVDD, GVDD and MVREF coupled one to another.

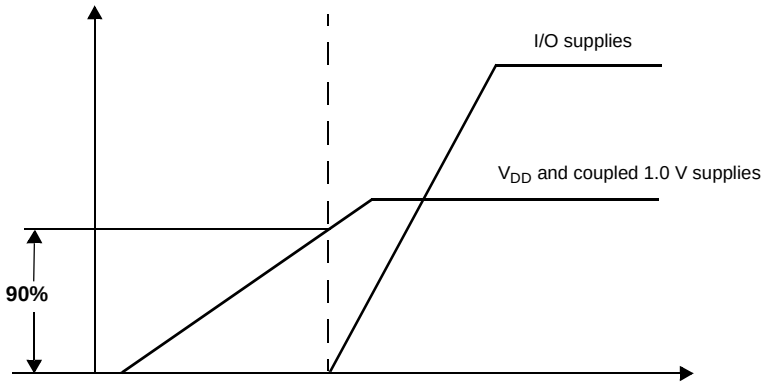


Figure 5. V_{DD} and I/O supplies Power-on Sequence

There is no dependency in power-up/power-down sequence between the GVDD, NVDD, and QVDD power rails. There is also no dependency in power-up/power-down sequence between the SerDes supplies SXCVDD and SXPVDD and other MSC8157/8 supplies. All supplies must be at their stable values within 50 ms as shown in Table 3 on page 11.

4.2 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow these ramp-up guidelines when starting up an MSC8157/8 device:

1. $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. However, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct functionality of the device.
2. V_{DD} is applied and ramps up. See **Section 4.3**, *Power-On Ramp Time* for the required ramp rate.
3. V_{DDIO} is applied and ramps up. See **Section 4.3**, *Power-On Ramp Time* for the required ramp rate.
4. CLKIN/MCLKIN starts toggling. It should swing within the V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.
5. CLKIN/MCLKIN should toggle at least 32 cycles before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value.
6. $\overline{\text{PORESET}}$ is deasserted.

Figure 6 shows a sequence in which V_{DDIO} ramps up after V_{DD} and CLKIN/MCLKIN begins toggling as the V_{DDIO} supply rises.

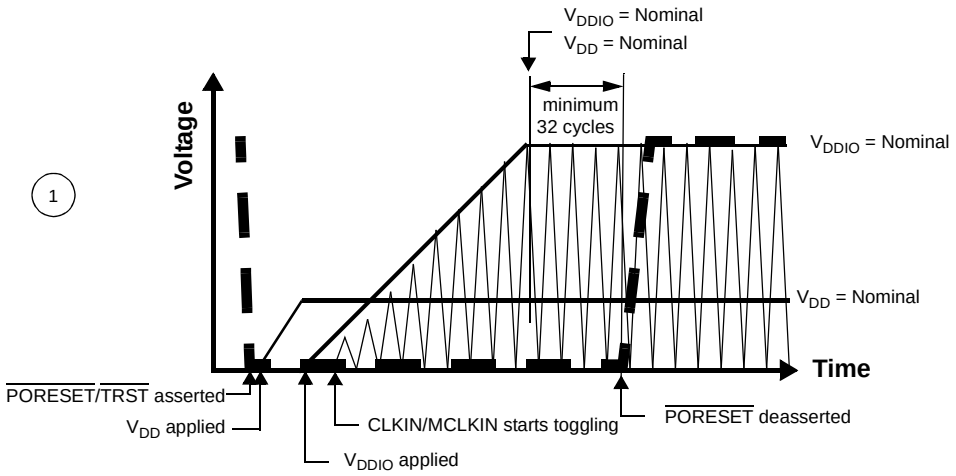


Figure 6. Supply Ramp-Up Sequence

4.3 Power-On Ramp Time

The power-on ramp rate applies to all voltage supplies (including GVDD/SXPVDD/SXCVDD/QVDD/GVDD/NVDD, all VDD supplies, MVREF, and all AVDD supplies). Controlling the maximum power-on ramp time is required to avoid falsely triggering the ESD circuitry. **Table 3** defines the power supply ramp rate and time specification.

Table 3. Power Supply Ramp Rate

Parameter	Min	Max	Unit
Required ramp rate	—	36000	V/s
Required ramp time.	—	50	ms

Note: 1. Ramp period is specified as a linear ramp from 10% to 90% of nominal voltage of the specific voltage supply.
2. All MCKE signals must remain low during the power up sequence.

4.4 Reset Connectivity

When a debugger is not used, implement the connection scheme shown in **Figure 7**. $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ can be tied together.

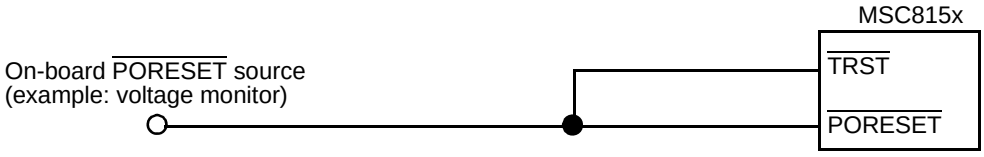


Figure 7. Reset Connection in Functional Application

When a debugger is used, implement the connection scheme shown in **Figure 8**.

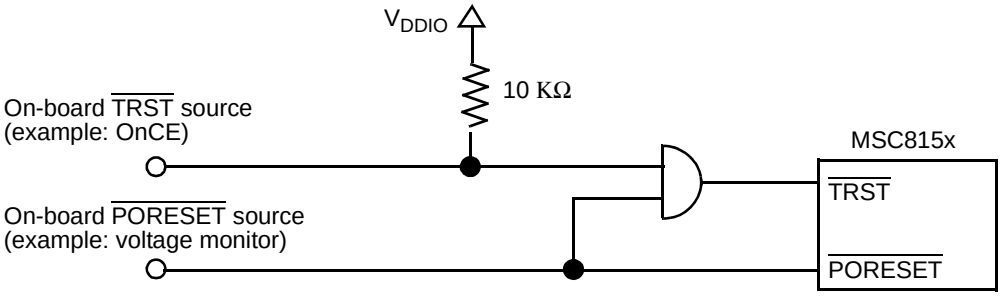


Figure 8. Reset Connection in Debugger Application

4.5 $\overline{\text{HRESET\_IN}}$ Usage

The $\overline{\text{HRESET\_IN}}$ signal allows resetting of the MSC8157/8 device without evoking hard reset of other devices that are connected in the same $\overline{\text{HRESET\_IN}}$ chain. In a multiprocessor system, the $\overline{\text{HRESET\_IN}}$ pin can be optionally used instead of the $\overline{\text{HRESET}}$ pin to allow individual reset. It can also be used to allow individual reset over the JTAG interface.

4.6 Reset Flow

The reset process and the reset configuration word (RCW) are described in detail in **Chapter 5,** *Reset* in the device specific reference manual.

A full reset is started by asserting the $\overline{\text{PORESET}}$ signal. The signal must remain asserted for a minimum time that is specified in the device specific technical data sheet. The contents of the RCW determine how the device is initialized and selects the basic I/O multiplexing mode, clock mode, and boot method. The reset configuration signals must be driven to the correct levels and held for the minimum time specified in the technical data sheet after the $\overline{\text{PORESET}}$ signal is deasserted. The reset sequence includes assertion of $\overline{\text{HRESET}}$.

After $\overline{\text{HRESET}}$ is deasserted, it can take 62000 OCN cycles (500 MHz clock) for the SerDes block (HSSI) to exit reset and lock its internal PLL. The user should poll the HSSI_SR[SERDES1_RST_DONE] and HSSI_SR[SERDES2_RST_DONE] bits to determine when the SerDes reset is complete if the relevant PLL is enabled. See the High Speed Serial Interface Status Register (HSSI_SR) description in **Chapter 8,** *General Configuration Registers* of the device specific reference manual for details.

The individual configuration signal selection determines the overall timing for the reset sequences, as described in **Chapter 5,** *Reset* in the reference manual. The $\overline{\text{HRESET}}$ signal is both an input and an output and can be asserted by external input or by software. An application can use these reset sequences to initialize specific internal device structures. Once asserted the MSC8157/8 device controls when the signals are deasserted based on the hard reset sequence, as defined in the reference manual.

NOTE

$\overline{\text{HRESET}}$ is an open-drain input/output pin. Make sure you use a pull-up resistor. After the initial assertion by an external host, make sure that the host releases the signal so that the MSC8157/8 device can deassert the signal. When using $\overline{\text{HRESET}}$, use **Table 5-2** *Reset Actions for Each Reset Source* in the device specific reference manual to verify that the selected signal supports the required reset functionality. Calculate and check the expected reset process duration. See **Section 5.2.3** *Reset Configuration Input Signal Selection and Reset Sequence Duration* in the device reference manual for details.

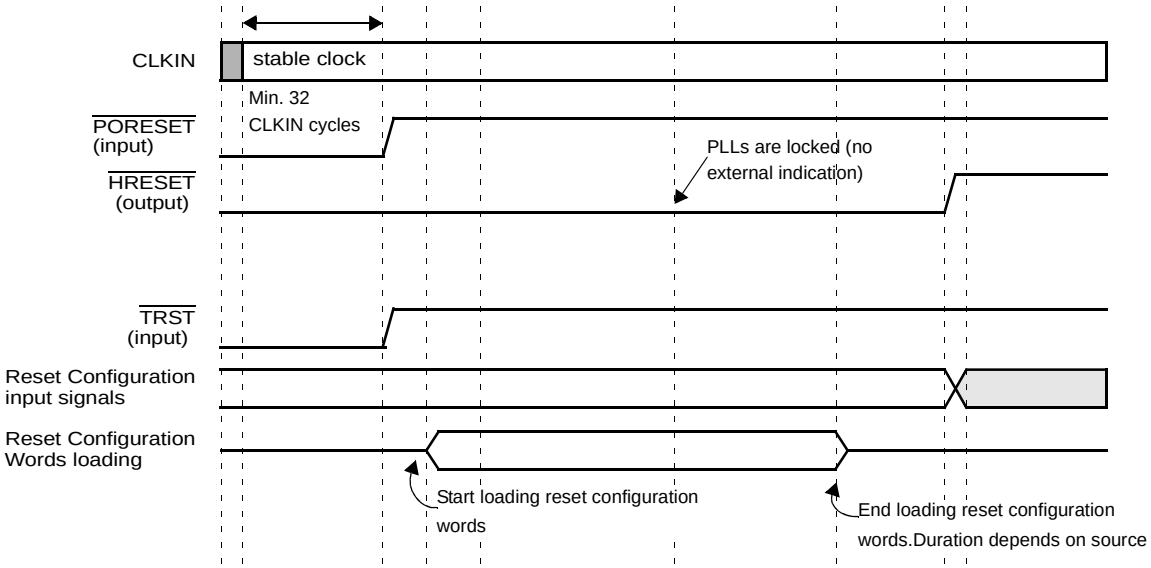


Figure 9. Power-On Reset Flow

4.7 Reset Configuration Word

See **Section 5.2.2** *Reset Configuration Word Source* in the device specific reference manuals for details about selecting the reset configuration input settings. Depending on the selected RCW source, use the following guidelines to assure proper device initialization:

- Using the information from **Section 5.2.2** *Reset Configuration Word Source* in the reference manual, select the correct RCW_SRC[0–2] combination that fits your design.
- You must use external pull up or pull down resistors in order to set the correct values of the RCW_SRC and RC signals during the $\overline{\text{PORESET}}$ flow. You must not rely on the internal pull up inside the GPIO signals for this purpose.
- If you are using the I^2C interface with a single EEPROM to initialize more than one MSC8157/8 device, use the connection guidelines given in **Chapter 5,** *Reset* of the reference manual. Verify that you are correctly connecting the I2C_SDA and I2C_SCL signal lines and are providing correct sequencing for asserting and deasserting the STOP_BS signal for each device.
- If RC[21–0] are used, make sure that the design supports the correct values during the reset sequence and then switches to required levels to support the configured functionality as GPIO, $\overline{\text{IRQ}}$ or DMA external signals. See **Chapter 5,** *Reset* of the device specific reference manual to see how the RC signals are used to define the RCW.
- If one of the two hard coded RCW is being used, make sure that RCW_SRC[0–2] has relevant setting for your configuration. See **Chapter 5,** *Reset* of the device specific reference manual for the hard-coded options for the RCW.

NOTE

Pay special attention to a configuration in which the signals RC[0–3] are being used during loading of the RCW in the multiplexed RCW loading mode (RCW_SRC[0–2] = 000) to a device and the device is configured as a reset master (RCWHR[RM] = 1). In such configuration the device will be using one or more of the GPIO[0–3] signals (which are shared with RC[0–3]) during its boot sequence to drive the STOP_BS of the reset slaves in the system (see **Section 5.2.1.5** *Loading Multiple Devices From a Single I^2C EEPROM* for more details) so the values driven on the RC[0–3] during the device $\overline{\text{PORESET}}$ sequence must be disconnected before the device start to drive the GPIO[0–3] signals in order to avoid contention. This can be done using tri-state buffers as in the example shown in the device specific reference manual in **Chapter 5,** *Reset,* **Section 5.2.5.2** *Loading Multiplexed RCW from External Pins (RCW_SRC[0–2] = 000).*

- If the application relies on loading RCW from I^2C EEPROM, consider how to initialize the I^2C EEPROM on a board fresh out of the assembly that is presumably filled with all 1s. To initialize I^2C EEPROM, the MSC8157/8 must be reset properly using another reset configuration such as the RC[21–0] signal lines or one of the two hard coded RCWs.

For additional information, see also:

- *Using an I^2C EEPROM During MSC8157 Initialization* (AN4205)

5 Boot

The boot process completes the initialization by setting up the selected interfaces and subsystems and loading the basic processing and data management software. **Chapter 6,** *Boot Program* in the reference manual gives a detailed description of the boot process for each possible boot scenario.

The boot program initializes the MSC8157/8 after it completes a reset sequence. The MSC8157/8 can boot from an external host through the RapidIO interface or download a user boot program through the I^2C, SPI, or Ethernet ports. The default boot code is located in an internal 96 KB ROM at 0xFEF00000–0xFEF17FFF and is accessible to all cores. For readability, the internal boot code is written in C and is based on the Freescale SmartDSP OS. Refer to **Chapter 6**, *Boot Program* in the device-specific reference manual for boot details.

The boot port is determined by the RCWHR[BPRT] field as listed in **Table 4**.

Table 4. Boot Port Select

Boot Port	RCWHR[BPRT]	Description
I^2C	0000	I^2C
RapidIO interface	0001	RapidIO interface without I^2C
	0010	RapidIO interface with I^2C
SPI	0011	SPI
RGMII1	0100	RGMII1 without I^2C
	0110	RGMII1 with I^2C
SGMII1	0101	SGMII1 without I^2C
	0111	SGMII1 with I^2C

Table 4. Boot Port Select (continued)

Boot Port	RCWHR[BPRT]	Description
SGMII2	1001	SGMII2 without I^2C
	1011	SGMII2 with I^2C
—	1000 1010 1100– 1111	Reserved

Chapter 6, *Boot Program* of the device specific reference manual describes the functionality and operation of the boot program. You must consider the following guidelines with regard to the boot program:

- The MSC8157/8 boot code uses the lower 25 KB of M3 memory starting from 0xC0000000. Make sure that the user boot code/application code that is being loaded to memory does not overwrite this memory space.
- Remember that MSC8157/8 uses both data cache (DCache) and instruction cache (ICache). If you download code to MSC8157/8 memory and there is valid data in the cache, the core uses the data from the cache. Use the INVALIDATE command on all caches (L1 ICache and DCache and L2 Cache) to ensure that the core reads updated data.
- If you are using an MMU setting during the boot or application download, remember to clear/update the MMU setting after the download is completed.
- After boot, all unused HSSI lanes should b powered down. Only used HSSI lanes should be powered up. Refer to **Section 8.1.6**, *HSSI Specific Lane Is Not Used on page 28* for connectivity of unused lanes.

For additional information, see:

- *Using an I^2C EEPROM During MSC8157 Initialization* (AN4205)
- *MSC81xx Ethernet Boot Test* (AN3436)

6 Clocking Guidelines

The following sections provides guidelines and descriptions for the various clocking systems used with and in the MSC8157/8.

6.1 Clock Signals

MSC8157/8 devices use clock signals for internal clocking and for synchronous interfaces. Each of the clock signals has its own unique requirements. **Table 5** shows the clock signals.

Table 5. MSC8157/8 Clock Signals

Module	Signal Name	Signal Description
General	CLKIN	Clock input to the MSC8157/8 PLLs
	CLKOUT	Clock output of PLL
SerDes	SD_REF_CLK[1-2]	SerDes reference clock. Differential pair.
	$\overline{\text{SD\_REF\_CLK[1-2]}}$	

Table 5. MSC8157/8 Clock Signals (continued)

Module	Signal Name	Signal Description
Timers	TMR0:TMR6	Timer input or output
JTAG	TCK	JTAG test clock
DDR	MCLKIN	Optional clock input to the DDR PLL
	MCK0:MCK2	DDR clock. Differential pair.
	$\overline{\text{MCK0:MCK2}}$	
QUICC Engine	GE1_RX_CLK	Ethernet 1 receive clock
	GE1_TX_CLK	Ethernet 1 transmit clock
	GE1_GTX_CLK	Ethernet 1 output transmit clock
	GE2_RX_CLK	Ethernet 2 receive clock
	GE2_TX_CLK	Ethernet 2 transmit clock
	GE2_GTX_CLK	Ethernet 2 output transmit clock
	GE_MDC	Ethernet management data clock
SPI	SPI_SCK	SPI clock
I^2C	I2C_SCL	I^2C clock

Refer to the device specific technical data sheet in for the individual signals requirements. For each clock signal, make sure that you comply with each of the following specifications:

- Clock frequency limits
- Clock slope limits
- Jitter limits
- Output clock load requirements
- Clock tree for the DDR-SDRAM balancing with zero delay buffers for large loads
- Special startup sequencing requirements for clock signals during reset

Refer to the individual functional block sections in the device specific reference manual for specific clock guidelines.

6.2 Clock Mode

As shown in **Chapter 7**, *Clocks* in the device-specific reference manual, the MSC8157/8 device has a flexible clocking scheme to deliver the clock frequencies used by the various subsystems and external interfaces. During power-on reset, the user configures a specific clock mode that defines the various clock frequencies and domains in the device. The specific clock mode is selected using the MODCK[5–0] field in the Reset Configuration Word Low Register (RCWLR). **Figure 7-1** in the device specific reference manual shows the relationships between the input clock (CLKIN), the optional DDR input clock (MCLKIN) and the mode (MODCK), and the internal clock domains.

Note that for each MODCK selected, a specific frequency is selected for each clock domain, and a CLKIN frequency of 133.333 MHz is required. **Table 7-1** in the device specific reference manual lists detailed information about the MODCK options. Evaluate each clock and make sure that CLKIN frequency and clock mode (MODCK) yield the desired internal frequencies as listed in **Table 7-2**.

6.3 Clock Mode Tool

A spreadsheet tool that calculates all component frequencies depending clock mode and clock source for the MSC8157/8 DSPs is available under NDA. This tool also validates configured clock schemes by clock specifications.

6.4 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance for single-ended signals and 100 Ω impedance for differential signals.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to calculate the resistor value:

  $R_{term} = R_{im} – R_{buf}$

  where R_{im} = trace characteristic impedance and

  R_{buf} = clock buffer internal impedance.

6.5 Unused Internal Clocks

The following section provides additional information about the individual subsystems to minimize power consumption and noise on the PCB buses in cases when one or more of the device subsystems is not used by the application.

6.5.1 DDR Memory Controller

In addition to providing proper termination for the unused DDR signal lines, the user should also set SCCR[DDRDIS] to disable the clock to the DDR controller.

In order to reduce DDR IO power consumption when the DDR controller is not in use, the user should set the DDR I/O into sleep mode in the DDR_GCR[DDR_DOZE]. This should be performed as soon as possible after PORESET sequence end.

6.5.2 QUICC Engine Subsystem

In addition to providing proper termination for the unused Ethernet and SPI signal lines, if none of the interfaces are used, you should also set SCCR[QEDIS] to disable the clock to the QUICC Engine subsystem. See **Chapter 7,** *Clocks* in the reference manual for detailed programming information.

6.5.3 HSSI Subsystem

In addition to providing proper termination for unused HSSI signal lines in case non of the HSSI interfaces (Serial RapidIO, PCI Express, SGMII, CPRI) are working (for non of the interfaces to work, RCWLR[SP] should be “0”, see **Chapter 5,** *Reset* in the reference manual for detailed programming information) you should also set SCCR[HSSIDIS] to disable the clock to the HSSI sub system. See **Chapter 7,** *Clocks* in the reference manual for detailed programming information.

6.5.4 CLKOUT

If CLKOUT is not used, set RCWLR[CLKO] = 11 and RCWLR[P3V] = 0 in order to configure CLKOUT to be always “low”. See **Chapter 5,** *Reset* and **Chapter 7,** *Clocks* in the reference manual for detailed programming information.

7 I/O Multiplexing

The MSC8157/8 devices support two groups of I/O configurations:

- SerDes Multiplexing
  - MSC8157/E: 2 Serial RapidIO interfaces, PCI Express interface, 2 SGMII interfaces and 6 lanes CPRI sharing the SerDes interface (10 lanes total).
  - MSC8158/E: 2 Serial RapidIO interfaces, 2 SGMII interfaces and 6 lanes CPRI sharing the SerDes interface (8 lanes total).
  - Selected during power-on reset by the RCWLR[SP] bits in the low part of the Reset Configuration Word (see **Chapter 5**, *Reset* for details).
- GPIO Multiplexing
  - GPIOs are shared with IRQs, external DMA, Timers, UART, SPI, I^2C and CPRI
  - Configured by GPIO configuration registers (see **Chapter 21**, *GPIO* for details).

Based on the system requirements, select the required interfaces, including external DDR memory, and the type of memory to be used. Refer to the pin-multiplexing tool that is available under NDA. Contact your local sales office or representative for details. This tool helps to define which interfaces can be selected simultaneously. See **Section 7.4** *Pin Multiplexing Tool* in this document for details

7.1 MSC8157 SerDes (HSSI) Multiplexing

The Serial RapidIO, PCI Express, SGMII, and CPRI signals are multiplexed on the 10 lanes of the SerDes interface on the MSC8157.

The required combination of interfaces is selected during power-on reset by the RCWLR[SP] bits in the low portion of the Reset Configuration Word. Table 6 describes the functionality of each lane of the HSSI ports, depending on the selected protocol. The number next to # specifies the controller number and the number between () specifies the lane number. Note the restrictions associated with the various RCWLR[SP] modes.

Note that there may be restrictions in some HSSI multiplexing modes as shown in the exceptions column. For example, in modes where RapidIO and SGMII are used, the RapidIO controller cannot operate at 3.125 GHz unless the SGMII is disabled by software.

Table 6. MSC8157 HSSI Multiplexing

RCWLR[SP] Protocol Select	Mode	SerDes Lanes										Exceptions
		A	B	C	D	E	F	G	H	I	J	
0000000	0	—	—	—	—	—	—	—	—	—	—	None
0000001	1	PEX(0)	PEX(1)	PEX(2)	PEX(3)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0000101	5	PEX(0)	PEX(1)	SGMII #1	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0000110	6	PEX(0)	RIO #2(1)	RIO #2(0)	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 3
0000111	7	PEX(0)	RIO #2(0)	SGMII #1	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 3
0001010	10	RIO #2(0)	RIO #2(1)	RIO #2(2)	RIO #2(3)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0001011	11	RIO #2(0)	RIO #2(1)	SGMII #1	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 3
0001100	12	RIO #2(0)	RIO #2(1)	SGMII #1	RIO #1(0)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2, 3
0001101	13	RIO #2(0)	RIO #2(1)	RIO #1(1)	RIO #1(0)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	2
0001110	14	RIO #2(0)	SGMII #2	SGMII #1	RIO #1(0)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2, 3
0010001	17	PEX(0)	PEX(1)	PEX(2)	PEX(3)	SGMII #1	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0010011	19	PEX(0)	PEX(1)	RIO #2(0)	RIO #2(1)	SGMII #1	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 3
0010100	20	PEX(0)	PEX(1)	RIO #2(0)	RIO #2(1)	RIO #1(0)	RIO #1(1)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2, 3

Exceptions

1. RIO cannot run at 3.125 GHz. unless SGMII is powered down by software.
2. If 3.125 GHz RIO is required, both RIO controllers must run at the same frequency.
3. Boot from RIO at 3.125 GHz is not supported.
4. Boot from RIO at frequencies other than 3.125 GHz is not supported.

Table 6. MSC8157 HSSI Multiplexing

RCWLR[SP] Protocol Select	Mode	SerDes Lanes										Exceptions
		A	B	C	D	E	F	G	H	I	J	
0010110	22	PEX(0)	PEX(1)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 3
0011101	29	RIO #2(0)	RIO #2(1)	RIO #2(2)	RIO #2(3)	RIO #1(0)	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2, 3
0011110	30	RIO #2(0)	RIO #2(1)	RIO #2(2)	RIO #2(3)	RIO #1(0)	RIO #1(1)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	2
0011111	31	RIO #2(0)	RIO #2(1)	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2, 3
0100011	35	PEX(0)	PEX(1)	PEX(2)	PEX(3)	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	CPRI #2	CPRI #1	1, 3
0100100	36	PEX(0)	PEX(1)	PEX(2)	PEX(3)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	1, 3
0100101	37	PEX(0)	PEX(1)	SGMII #1	SGMII #2	RIO #2(1)	RIO #2(0)	RIO #1(0)	RIO #1(1)	CPRI #2	CPRI #1	1, 2, 3
0101000	40	RIO #2(0)	RIO #2(1)	RIO #2(2)	RIO #2(3)	SGMII #1	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 3
0101110	46	PEX(0)	PEX(1)	RIO #2(0)	RIO #2(1)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	1, 2, 3
0110000	48	PEX(0)	PEX(1)	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	1, 3
0111101	61	RIO #2(0)	RIO #2(1)	RIO #2(2)	RIO #2(3)	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	CPRI #2	CPRI #1	1, 2, 3
1000001	65	RIO #2(0)	RIO #2(1)	RIO #2(2)	RIO #2(3)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	2
1000010	66	PEX(0)	PEX(1)	PEX(2)	PEX(3)	RIO #2(1)	RIO #2(0)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 2, 3
1000101	69	PEX(0)	PEX(1)	PEX(2)	PEX(3)	SGMII #1	SGMII #2	RIO #2(1)	RIO #2(0)	RIO #1(0)	RIO #1(1)	1, 2, 3
1010001	81	PEX(0)	PEX(1)	PEX(2)	PEX(3)	SGMII #1	RIO #2(0)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 2, 3
1010011	83	PEX(0)	PEX(1)	PEX(2)	PEX(3)	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 3
1010100	84	PEX(0)	PEX(1)	PEX(2)	PEX(3)	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 4
1010101	85	PEX(0)	PEX(1)	SGMII #1	SGMII #2	RIO #2(1)	RIO #2(0)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 3
1100110	102	RIO #2(0)	RIO #2(1)	RIO #2(2)	RIO #2(3)	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	SGMII #1	SGMII #2	1, 2, 3

Exceptions

1. RIO cannot run at 3.125 GHz. unless SGMII is powered down by software.
2. If 3.125 GHz RIO is required, both RIO controllers must run at the same frequency.
3. Boot from RIO at 3.125 GHz is not supported.
4. Boot from RIO at frequencies other than 3.125 GHz is not supported.

The frequency of each protocol is configured in the RCWLR as shown below. Refer to the reference manual for more details on the protocol frequency.

- RCWLR[R1FREQ] selects the frequency for the RapidIO port 1

- RCWLR[R2FREQ] selects the frequency for the RapidIO port 2
- RCWLR[PFREQ] selects the frequency for the PCI Express
- RCWLR[CFREQ] selects the frequency for the CPRI
- RCWLR[SCLK1, SCLK2] select the SerDes reference clock

7.2 MSC8158/E SerDes (HSSI) Multiplexing

The Serial RapidIO, SGMII and CPRI signals are multiplexed on the 8 lanes of the SerDes interface on the MSC8158/E.

The needed combination of interfaces is selected during power-on reset by the RCWLR[SP] bits in the low portion of the Reset Configuration Word. Table 7 describes the functionality of each lane of the HSSI ports, depending on the selected protocol. The number next to # specifies the controller number and the number between () specifies the lane number. Note the restrictions associated with the various RCWLR[SP] modes.

Note that there may be restrictions in some HSSI multiplexing modes as shown in the exceptions column. For example, in modes where RapidIO and SGMII are used, the RapidIO controller cannot operate at 3.125 GHz unless the SGMII is disabled by software.

Table 7. MSC8158 HSSI Multiplexing

RCWLR[SP] Protocol Select	Mode	SerDes Lanes								Exceptions
		C	D	E	F	G	H	I	J	
0000000	0	—	—	—	—	—	—	—	—	None
0000001	1	—	—	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0000101	5	SGMII #1	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0000110	6	—	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0000111	7	SGMII #1	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0001010	10	—	—	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0001011	11	SGMII #1	SGMII #2	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0001100	12	SGMII #1	RIO #1(0)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0001101	13	RIO #1(1)	RIO #1(0)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0001110	14	SGMII #1	RIO #1(0)	CPRI #6	CPRI #5	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2

Exceptions

1. RapidIO interface cannot run at 3.125 GHz.
2. Boot from RapidIO interface at 3.125 GHz is not supported.
3. RIO #2 is powered down by boot. If needed, this controller should be powered up by the user code according to the power up sequence requirements.
4. If 3.125 GHz RapidIO interface is required, both RapidIO controllers must run at the same frequency

Table 7. MSC8158 HSSI Multiplexing (continued)

RCWLR[SP] Protocol Select	Mode	SerDes Lanes								Exceptions
		C	D	E	F	G	H	I	J	
0010001	17	—	—	SGMII #1	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0010010	19	—	—	SGMII #1	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0010011	20	RIO #2(0)	RIO #2(1)	RIO #1(0)	RIO #1(1)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	2, 3, 4
0010110	22	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0011101	29	—	—	RIO #1(0)	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0011110	30	—	—	RIO #1(0)	RIO #1(1)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	None
0011111	31	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0100011	35	—	—	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	CPRI #2	CPRI #1	1, 2
0100100	36	—	—	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	None
0100101	37	SGMII #1	SGMII #2	RIO #2(1)	RIO #2(0)	RIO #1(0)	RIO #1(1)	CPRI #2	CPRI #1	1, 2, 3
0101000	40	—	—	SGMII #1	SGMII #2	CPRI #4	CPRI #3	CPRI #2	CPRI #1	1, 2
0101110	46	—	—	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	None
0110000	48	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	1, 2
0111101	61	—	—	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	CPRI #2	CPRI #1	1, 2
1000001	65	—	—	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	CPRI #2	CPRI #1	None
1000010	66	—	—	—	—	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	None
1000101	69	—	—	SGMII #1	SGMII #2	—	—	RIO #1(0)	RIO #1(1)	1, 2
1010001	81	—	—	SGMII #1	—	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 2
1010011	83	—	—	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 2
1010100	84	—	—	SGMII #1	SGMII #2	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 3

Exceptions

1. RapidIO interface cannot run at 3.125 GHz.
2. Boot from RapidIO interface at 3.125 GHz is not supported.
3. RIO #2 is powered down by boot. If needed, this controller should be powered up by the user code according to the power up sequence requirements.
4. If 3.125 GHz RapidIO interface is required, both RapidIO controllers must run at the same frequency

Table 7. MSC8158 HSSI Multiplexing (continued)

RCWLR[SP] Protocol Select	Mode	SerDes Lanes								Exceptions
		C	D	E	F	G	H	I	J	
1010101	85	SGMII #1	SGMII #2	—	—	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	1, 2
1100110	102	—	—	RIO #1(0)	RIO #1(1)	RIO #1(2)	RIO #1(3)	SGMII #1	SGMII #2	1, 2

Exceptions

1. RapidIO interface cannot run at 3.125 GHz.
2. Boot from RapidIO interface at 3.125 GHz is not supported.
3. RIO #2 is powered down by boot. If needed, this controller should be powered up by the user code according to the power up sequence requirements.
4. If 3.125 GHz RapidIO interface is required, both RapidIO controllers must run at the same frequency

The frequency of each protocol is configured in the RCWLR as shown below. Refer to the reference manual for more details on the protocol frequency.

- RCWLR[R1FREQ] selects the frequency for the RapidIO port 1
- RCWLR[R2FREQ] selects the frequency for the RapidIO port 2
- RCWLR[CFREQ] selects the frequency for the CPRI
- RCWLR[SCLK1, SCLK2] select the SerDes reference clock

7.3 GPIO Multiplexing

One GPIO signal is dedicated (GPIO22). The remainder of the signals have multiplexed functionality as either GPIO or $\overline{\text{IRQ}}$, DMA external requests, Timers, UART, SPI, I^2C, or CPRI. See the product specific reference manual in **Section 3.9** *GPIO/Maskable Interrupt Signal Summary* for details. In addition, some of the GPIO signals are served during the PORESET sequence for configuration. See **Section 3.3** *Reset and Configuration Signals* and **Chapter 5**, *Reset* in the reference manual for details.

NOTE

Some GPIO signal lines have specific reset functionality during the reset process and different functionality in normal operation. See **Section 3.3** *Reset and Configuration Signals* in the device reference manual for details. Verify the following with regard to reset signal lines:

- Make sure that the reset signals have the proper value during the reset process and that the alternate functionality is disabled.
- After reset is complete, make sure that the required alternate signal functionality is enabled
- In order to use GPIO input, the corresponding GPIO input pins must be enabled in the GIER register. The default setting is disabled
- If you want to use the GPIO pin as either IRQ, DMA external requests, Timers, UART, SPI, I^2C or CPRI, you must also program the GPUER and GIER registers to set their correct values. They are not

automatically set by the settings of the PAR register as dedicated peripheral.

7.4 Pin Multiplexing Tool

To validate the pin multiplexing plan and verify the status of all pins for your application, there is a pin multiplexing tool available under NDA. The tool spreadsheet confirms all pin availability based on application requirements, such as DDR memory, peripherals, GPIO/$\overline{\text{IRQ}}$ pins, and so on. In addition, this tool validates power supplies and displays all pin mapping based for the application. Contact your local sales office or representative for details.

8 Connectivity Guidelines

Select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

- GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
- V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
- Mandatory use of a pull-up or pull-down resistor is clearly indicated as “pull-up/pull-down.” For buses, each pin on the bus should have its own resistor.
- NC indicates “not connected” and means do not connect anything to the pin.
- The phrase “in use” indicates a typical pin connection for the required function

8.1 Disposition of Unused Signal Lines

Some applications may not use all available MSC8157/8 interfaces. For the unused signal lines, proper system design should include correct termination to achieve the following:

- Allow proper functionality for the device.
- Reduce power consumption.
- Reduce number of signal connection.
- Reduce PCB design complexity.

8.1.1 Unused GPIO Signal Connections

Unused GPIO signals should be left not connected, as long as they are not used as their other function (IRQ, DMA external signals, Timers, UART, SPI or I^2C). Because all GPIO signals are configured as GPIO with inputs and outputs disabled and the internal 20 kΩ pull up is enabled by default after reset, those that remain unused pins should be left unconnected.

8.1.2 DDR Interface Is Not Used

Table 8. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MCLKIN	GND
MDQ[0–63]	NC
MDQS[7–0]	NC
$\overline{\text{MDQS[7–0]}}$	NC
MA[15–0]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[1–0]}}$	NC
MDM[7–0]	NC
MBA[2–0]	NC
$\overline{\text{MCAS}}$	NC
MCKE[1–0]	NC
MODT[1–0]	NC
MMDIC[1–0]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC
MAPAR_OUT	NC

Table 8. Connectivity of DDR Related Pins When the DDR Interface Is Not Used (continued)

Signal Name	Pin Connection
$\overline{\text{MAPAR\_IN}}$	NC
MVREF	NC
GVDD	NC
Note: If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DR_GCR[DDR_DOZE]. See the *Clocks* and *General Configuration Registers* chapters in the ***MSC8157/8 Reference Manual*** for details.	

8.1.3 DDR Interface Is Used With 32-Bit DDR Memory Only

Table 9 lists unused pin connection when using 32-bit DDR memory. The 32 most significant data lines are not used.

Table 9. Connectivity of DDR Related Pins When Using 32-bit DDR Memory Only

Signal Name	Pin Connection
MCLKIN	optional
MDQ[31–0]	in use
MDQ[63–32]	NC
MDQS[3–0]	in use
MDQS[7–4]	NC
$\overline{\text{MDQS[3–0]}}$	in use
$\overline{\text{MDQS[7–4]}}$	NC
MA[15–0]	in use
MCK[2–0]	in use
$\overline{\text{MCK[2–0]}}$	in use
$\overline{\text{MCS[1–0]}}$	in use
MDM[3–0]	in use
MDM[7–4]	NC
MBA[2–0]	in use
$\overline{\text{MCAS}}$	in use
MCKE[1–0]	in use
MODT[1–0]	in use
MMDIC[1–0]	in use
$\overline{\text{MRAS}}$	in use
$\overline{\text{MWE}}$	in use
MVREF	= GVDD x 0.5 V
GVDD	1.5 V

8.1.4 DDR ECC Is Not Used

When the error code correction mechanism is not used in any 32- or 64-bit DDR configuration, refer to **Table 10** to determine the correct pin connections.

Table 10. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC

8.1.5 HSSI Port Is Not Used

The signal names in **Table 11** are inclusive names for the SerDes interfaces. For individual pin names refer to **Table 12**.

Table 11. Connectivity of HSSI Related Pins When No HSSI Lanes Are Used

Signal Name	Pin Connection
SD_IMP_CAL_RX	NC
SD_IMP_CAL_TX	NC
$\overline{\text{SD\_REF\_CLK[1–2]}}$	SXCVSS
SD_REF_CLK[1–2]	SXCVSS
SD_[A–J]_RXD	SXCVSS
$\overline{\text{SD\_[A–J]\_RXD}}$	SXCVSS
$\overline{\text{SD\_[A–J]\_TXD}}$	NC
SD_[A–J]_TXD	NC
SD_PLL[1–2]_AVDD	1.0 V
SD_PLL[1–2]_AGND	0 V
SXPVSS	0 V
SXCVSS	0 V
SXPVDD	1.5 V
SXCVDD	1.0 V
Note: All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8157/8 Reference Manual* for details.	

8.1.6 HSSI Specific Lane Is Not Used

Removing power to an unused HSSI lane could cause unpredictable voltage levels on lane outputs or a high leakage situation on lane inputs. **Table 12** shows the connectivity when a specific HSSI lane is not used.

Table 12. Connectivity of HSSI Related Pins When a Specific Lane Is Not Used

Signal Name	Pin Connection
SD_IMP_CAL_RX	Pull up to SXCVDD with 200 Ω resistor
SD_IMP_CAL_TX	Pull up to SXPVDD with 200 Ω resistor
$\overline{\text{SD\_REF\_CLK[1–2]}}$	In use
SD_REF_CLK[1–2]	In use
SD_[A–J]_RXD	SXCVSS
$\overline{\text{SD\_[A–J]\_RXD}}$	SXCVSS
$\overline{\text{SD\_[A–J]\_TXD}}$	NC
SD_[A–J]_TXD	NC
SD_PLL[1–2]_AVDD	1.0 V
SD_PLL[1–2]_AGND	0 V
SXPVSS	0 V
SXCVSS	0 V
SXPVDD	1.5 V
SXCVDD	1.0 V
Note: The signal names indicate a signal series. Connectivity guidelines should only be applied for the specific lane/lanes that are not used.	

8.1.7 RGMII Ethernet Is Not Used

Table 13. Connectivity of RGMII Related Pins When the RGMII Interface Is Not Used

Signal Name	Pin Connection
GE1_RD0	GND
GE1_RD1	GND
GE1_RD2	GND
GE1_RD3	GND
GE1_RX_CLK	GND
GE1_RX_CTL	GND
GE1_TD0	NC
GE1_TD1	NC
GE1_TD2	NC
GE1_TD3	NC
GE1_TX_CLK	NC
GE1_TX_CTL	NC
GE1_GTX_CLK	NC

Table 13. Connectivity of RGMII Related Pins When the RGMII Interface Is Not Used (continued)

Signal Name	Pin Connection
GE2_RD0/CP_LOS6	GND
GE2_RD1	GND
GE2_RD2/CP_LOS1	GND
GE2_RD3/CP_LOS2	GND
GE2_RX_CLK	GND
GE2_RX_CTL	GND
GE2_TD0	NC
GE2_TD1	NC
GE2_TD2/CP_LOS3	GND
GE2_TD3/CP_LOS5	GND
GE2_TX_CLK	NC
GE2_TX_CTL	NC
GE2_GTX_CLK/CP_LOS4	GND

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. Table 14 lists the recommended management pin connections.

Table 14. Connectivity of GE Management Pins When RGMII Is Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

8.1.8 Unused Miscellaneous Pins

Table 15 lists the board connections for the pins not required by the system design. It assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 15. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{HRESET\_IN}}$	NC
$\overline{\text{INT\_OUT}}$/CP_TX_INT	NC
$\overline{\text{IRQ[15–0]}}$	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$/CP_RX_INT	NC
RC[21–0]	GND

Table 15. Connectivity of Individual Pins When They Are Not Required (continued)

Signal Name	Pin Connection
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[6–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	See **Section 4** *Power-Up Sequence* for guidelines.
GPIO28/UART_RXD/CP_LOS1	See the GPIO connectivity guidelines in this table.
GPIO29/UART_TXD//CP_LOS2	See the GPIO connectivity guidelines in this table.
DDN[1–0]	See the GPIO connectivity guidelines in this table.
DRQ[1–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{RCW\_LSEL\_0}}$	GND
$\overline{\text{RCW\_LSEL\_1}}$	GND
$\overline{\text{RCW\_LSEL\_2}}$	GND
$\overline{\text{RCW\_LSEL\_3}}$	GND
CP_SYNC1	See the GPIO connectivity guidelines in this table.
CP_SYNC2	See the GPIO connectivity guidelines in this table.
CP_SYNC3	See the GPIO connectivity guidelines in this table.
GPIO17/SPI_SCK/CP_LOS3	See the GPIO connectivity guidelines in this table.
GPIO19/SPI_MISO/CP_LOS5	See the GPIO connectivity guidelines in this table.
GPIO18/SPI_MOSI/CP_LOS4	See the GPIO connectivity guidelines in this table.
GPIO20/$\overline{\text{SPI\_SL}}$/CP_LOS6	See the GPIO connectivity guidelines in this table.

Note: For details on configuration, see the *MSC8157/8 Reference Manual*. For additional information, refer to the *MSC815x and MSC825x DSP Family Design Checklist*.

8.2 Open Drain Pins

The following signals use open drain pins and must have appropriate pull up resistor attached to them on the board: $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and $\overline{\text{HRESET}}$.

The GPIO signals can be configured as open drain in the PODR register, and in that case they also need a pull up resistor.When GPIO signals are configured as I^2C, UART or SPI, the signals are configured as open drain in some cases. See the relevant chapters in the reference manual for additional details, and also the following sections in this document: **Section 8.6**, *UART* and **Section 8.7**, *I^2C*.

8.3 DDR External Memory Use

Careful consideration must be given to the design and implementation of the external memory subsystem. The DDR memory supported by MSC8157/8 devices is a high-frequency memory interface and the printed circuit board (PCB) design must be done carefully and verified with a simulation tool. The following list highlights the main issues to consider in such a design:

- Perform simulation for board layout to select proper termination. Use simulation output for AC timing calculation.
- Perform detailed timing analysis for AC spec between MSC8157/8 and DDR-SDRAM device, include signal propagation delay, coupling, termination mismatch, trace mismatch, and clock skew.

8.3.1 SSTL-1.5 Interface and Board Design Guidelines

DDR3 memory adopts the SSTL-1.5 interface shown in **Figure 10**. V_{TT} and V_{REF} are half the voltage level of V_{DDQ} in the DDR memory. V_{DDQ} and V_{DDDDR} in MSC8157/8 device share a power supply of 1.5 V for DDR3. V_{REF} in DDR memory and MV_{REF} in MSC8157/8 device share half the voltage of V_{DDDDR}.

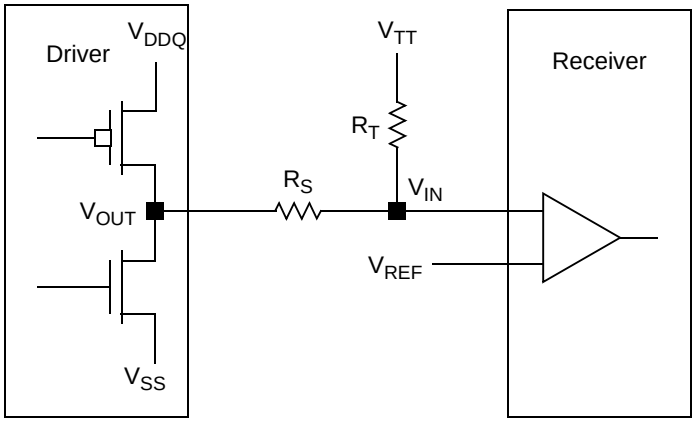


Figure 10. Typical Memory Interface Using Class II Option

Use the following guidelines for designing your system:

- V_{TT} and V_{REF} should have DC values as close as possible. To reduce temperature impact, use a single IC to generate both.
- V_{TT} should support high current. Calculate based on the worst case high current and design the V_{TT} source to support it. Use distributed decoupling capacitance.
- V_{REF} should be isolated from noise by space and decoupling capacitance.
- Use on-die termination for data, strobe and mask pins. Use R_T termination for address and control pins.
- MV_{REF} voltage can be generated by a resistor divider of V_{DDDDR} voltage. Both of the resistors must be the same resistance with 1% tolerance. Design the resistance of the resistor divider so that the resistor divider can feed maximum MV_{REF} current to MSC8157/8 device and maximum V_{REF} current to DDR memory.
- Use the following DDR routing order:

  - 1. Power ($V_{TT,}$ V_{REF})
  - 2. Data
  - 3. Address / command
  - 4. Control
  - 5. Clocks
- Select appropriate power supply level for design and simulation.
- If multiple MSC8157/8 DSP devices reside closely on a board, route adjacent DDR data groups on alternating critical board layers.
- In DSP farms, simultaneous switching draws more power if the DDR clocks on DSPs are synchronized. MSC8157/8 PLL outputs are synchronized to a relevant CLKIN. Using a clock tree on the board that provides a phase-shifted CLKIN to each MSC8157/8 on the board prevents simultaneous switching.

8.3.2 DDR Data Bits Connectivity

It is very important to connect the lowest data bit of each byte at the memory component to the corresponding lowest data bit at the DDR controller as shown in **Table 16**. The same guideline applies to the ECC bits. Without this connection, the write levelling calibration required by DDR3 will not be functional. It is not important how the other 7 bits of each byte are connected.

Table 16. DDR Controller to DDR SDRAM Connection

DDR SDRAM Pin	MSC8157/8 Pin
DQ0	MDQ0
DQ8	MDQ8
DQ16	MDQ16
DQ24	MDQ24
DQ32	MDQ32
DQ40	MDQ40
DQ48	MDQ48
DQ56	MDQ56
ECC0	MECC0

Use the following guidelines for the DDR3 memory device connectivity:

- DDR memory device $\overline{\text{RESET}}$ needs to be asserted low at power up.
- DDR memory device VREFCA needs to be routed to V_{REF} for address/command.
- DDR memory device VREFDQ needs to be routed to V_{REF} for data.

8.3.3 Memory Signal Termination

The DDR controller supports DDR3 SDRAM. This memory type requires the following signal termination:

- If the DDR interface is not used, refer to **Table 8** for proper signal termination.
- If the DDR interface is in 32-bit mode, refer to **Table 9** for proper signal termination.
- If the ECC is not used, refer to **Table 10** for proper signal termination.
- Connect MMDIC0 to GND through an 36-Ω precision 1% resistor.
- Connect MMDIC1 to V_{DDDDR} through an 36-Ω precision 1% resistor.

NOTE

MMDIC0 and MDIC1 are used for the automatic impedance calibration.
The drive calibration is independently enabled/disabled while in full strength mode. There is no drive calibration while in half strength mode.

- The DDR controller supports the ZQ calibration commands ZQCL, ZQCS by DDR_ZQ_CNTL. To use the ZQ calibration function, a 240 Ω ± 1% tolerance resistor must be connected between the ZQ pin of the DDR3 memory and ground.

8.3.4 DDR Clock During Reset

During any RESET signal assertion ($\overline{\text{HRESET}}$, $\overline{\text{HRESET\_IN}}$, $\overline{\text{PORESET}}$), MCKE[0–1] are driven low (deasserted).

8.4 HSSI-SerDes Interface for Serial RapidIO, PCI Express, SGMII and CPRI Connections

The MSC8157/8 supports Serial Rapid IO, PCI Express (only MSC8157/E), SGMII and CPRI interfaces in many combinations over the HSSI (High Speed Serial Interface) port. Use the following considerations when implementing these interfaces in your design:

- The signal list in the technical data sheet identifies the signals by ball location. Use this list to check your schematic for proper connectivity.
- The HSSI uses dedicated power supplies. Connect proper supply levels according to the specifications defined in the technical data sheet.
- The HSSI uses a dedicated PLL power supply. Connect proper supply levels according to the specifications defined in the technical data sheet using appropriate decoupling capacitors.
- Because it is a high frequency interface, use simulations to perform detailed signal integrity analysis for the HSSI. Check that the eye opening fits the definition for your system and baud rate using **Section 2.6.2.3** *Serial RapidIO AC Timing Specifications* in the device specific data sheet.
- The HSSI differential output voltage comply with the RapidIO protocol for both “short” and “long” run without any change in the device supply levels (unlike the MSC814x devices in which different voltages were used for “short” and “long” run configurations). Make sure your system fits the transmitter supply output voltages of the device as defined in the device specific data sheet.
- Refer to “Motherboard/BIOS Compliance Checklist for the PCI Express Base 2.0 Specification,” available from http://www.pci-sig.org for a list of PCI Express PCB design recommendations.

8.4.1 Impedance Calibration Signals

There are two inputs used for automatic impedance calibration by the SerDes initialization when the RCW activates SerDes interface during the reset sequence. These pins must be terminated as follows.

- The receiver impedance control external calibration signal SD_IMP_CAL_RX is pulled up to SXCVDD with 200 Ω (±1%) resistor.
- The transmitter impedance control external calibration signal SD_IMP_CAL_TX is pulled up to SXPVDD with 200 Ω (±1%) resistor.

8.4.2 SerDes Reference Clocks Guidelines

The SerDes differential reference clock inputs are SD_REF_CLK[1-2] and $\overline{\text{SD\_REF\_CLK[1-2]}}$. Refer to specific device technical data sheet for the DC-level requirements for the SerDes reference clocks. Requirements for the input amplitude differ depending on the signaling mode, differential or single-ended, used to connect the clock driver chip to the SerDes reference clock inputs.

8.4.3 SerDes Data Lane Guidelines

Use the following guidelines for designing data lanes into a system:

- The board must have an AC coupling capacitor on each one of the MSC8157/8 receive connections. These capacitors ensure proper conditions for the RapidIO receivers independent of the driving device, as long as the driving device complies with the RapidIO standard. To clarify, two capacitors are required for each lane. Therefore, for a x4 connection, 8 capacitors are required. The maximum external AC coupling capacitor value to be used is 200 nF and the minimum is 75 nF, however a lower value which should be higher then 10 nF can be used. The values in the range 10 nF–75 nF were not tested by Freescale but are likely to work.
- The on chip AC coupling must be enabled together with the on board AC coupling capacitor, resulting 2 series capacitors.
- The transmit direction probably does not need similar capacitors because the MSC8157/8 ensures that in x1 mode the outputs of the other three lanes are tri-stated.
- There is a possibility that the counter part will require AC-coupling, to ensure its input stage.
- The capacitor is required only if the device attached to MSC8157/8 device cannot guarantee an AC-coupled (no DC signal offset) output or if the lanes connection current is higher than 8–10 mA.

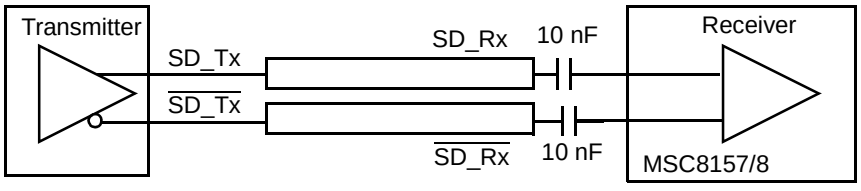


Figure 11. SerDes Transmitter and Receiver

The following document provides additional detailed design guidelines:

- MSC8156 High Speed Serial Interface Hardware Design Considerations *(AN3656)*.

8.5 Ethernet

The MSC8157/8 has two Ethernet controllers supported by the QUICC Engine™ subsystem. Each controller supports two standard MAC-PHY interfaces to connect to an external Ethernet transceiver. Supported interfaces include:

- 1000 Mbps RGMII interface
- 1000 Mbps SGMII interface (connected externally using SerDes lines via the HSSI)

8.5.1 Ethernet Clocks

The QUICC Engine subsystem requires input clocks as shown on the right of **Figure 12** to drive the UCC clock signals. For example, the 125 MHz clock source GTX_CLK125 as shown in **Figure 13** is input to GE1_TX_CLK, which is used to drive the GE1_GTX_CLK clock output from the MSC8157/8 to the Ethernet PHY. In another example, RX_CLK of the Ethernet PHY in **Figure 13** is input to the GE1_RX_CLK, which is used to drive UCC1 Rx as clock input from the Ethernet PHY.

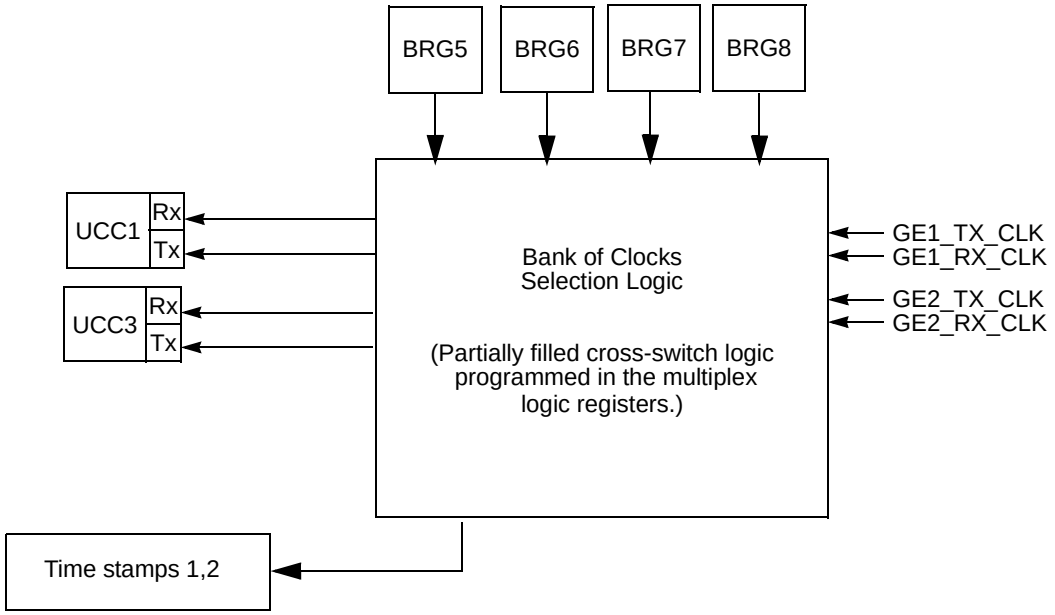


Figure 12. Bank of Clocks in the QUICC Engine Subsystem

Table 17. Clock Source Options Using External Clock Signals

Clock	External CLK			
	GE1_RX_CLK	GE1_TX_CLK	GE2_RX_CLK	GE2_TX_CLK
UCC1 Rx	V			
UCC1 Tx		V		
UCC3 Rx			V	
UCC3 Tx				V
Time Stamp 1			V	V
Time Stamp 2			V	V

8.5.2 General Ethernet Guidelines

Use the following guidelines for designing an Ethernet interface into a system:

- **Section 19.7.2** *Ethernet Physical Interfaces* in the reference manual identifies the correct signals to use for each Ethernet controller and interface type.
- The signal list in the technical data sheet identifies the signal by ball location. Use this list to check your schematic for proper connectivity.
- The SGMII mode uses a SerDes interface with differential pair signals. Refer to the technical data sheet for detailed specifications and operating descriptions. The RCW selects the SerDes interface for SGMII, see description in **Section 5.3.1** *Reset Configuration Word Low Register (RCWLR)* in the device reference manual.
- For using the GE_MDIO and GE_MDC signals consider whether an external host processor can manage Ethernet PHY instead of MSC8157/8 device. If GE_MDIO and GE_MDC are not used, terminate the signals as described in Table 14 in this document.
- Terminate any unused Ethernet signal lines (that are also not multiplexed for any other use) as described in Table 13 in this document.
- The Ethernet transceivers in the MSC8157/8 have 50 Ω internal buffer resistance. As a general rule:
  - If you are not sure about 50 Ω impedance in the PHY, you should add 22 Ω impedance in series between the MSC8157/8 and the PHY placed close to the transmitter side to help terminate the line.
  - If a long trace (>2 inches) exists between the MSC8157/8 and the PHY, you should also add a 22 Ω termination resistor.
  - If the trace that exists between the MSC8157/8 and the PHY is very short, connect directly without the additional termination resistor.

For additional information, see the following:

- *MSC8156 Ethernet Performance: Maximizing QUICC Engine™ Throughput* (AN3873)

8.5.3 RGMII Considerations

Figure 13 is an example is provided for connecting each of the controllers to an RGMII PHY or switch.

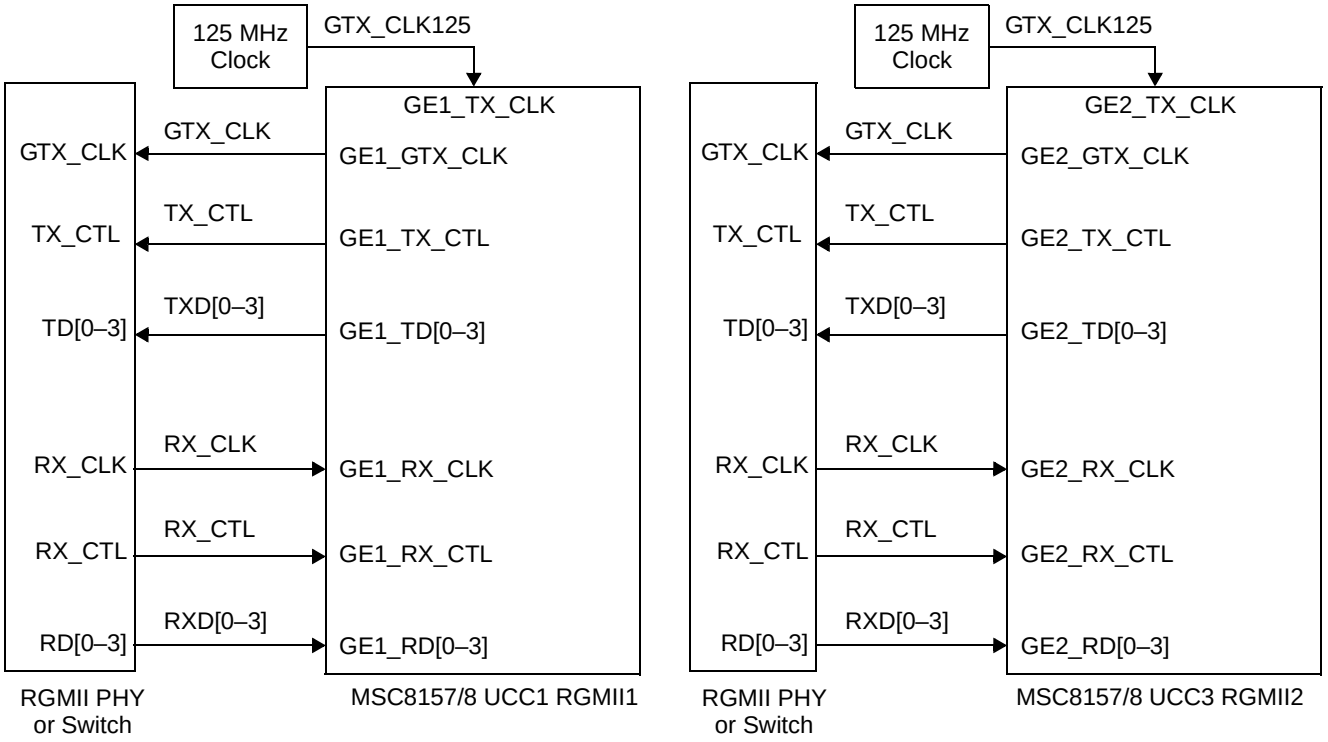


Figure 13. RGMII Connection Diagram Example

NOTE

The RGMII AC value, data-to-clock-output skew at the transmitter in MAC-to-MAC mode does not meet the RGMII specification in the MSC8157/8 devices. The tSKEWT maximum value is –0.9 ns instead of –1.0 ns. Therefore, when designing a board for a specific application, route GTX_CLK such that an additional trace delay of between 0.1 and 0.2 ns is added to the clock signal line.

8.6 UART

The MSC8157/8 devices support a UART interface that can be operated in half duplex (single wire) or full duplex mode (**Chapter 20,** *UART* in the reference manual for more details). The UART is multiplexed on the GPIO signals (GPIO28/UART_RXD and GPIO29/UART_TXD) and must be selected by configuring its functionality through the GPIO configuration (see **Chapter 21,** *GPIO* in the reference manual for programming details). Use the following guidelines when designing the UART signal interface:

- Select the connection type (half duplex single wire or full duplex) and identify the proper signal connection locations (only UART_TXD for half duplex) using the signal list in the technical data sheet.
- MSC8157/8 UART_TXD is driven only when data is transmitted, so connect a pull-up resistor to this connection to avoid a floating signal.

- If UART_RXD is not connected to a full drive initiator, connect a pull-up resistor to avoid a floating signal.

8.7 I^2C

The MSC8157/8 devices support an I^2C interface that is supported in all I/O modes, but must be selected by configuring its functionality through the GPIO configuration (see **Chapter 21,** *GPIO* in the reference manual for programming details). Typically, this interface is used for loading the Reset Configuration Word (RCW) and booting the device from an EEPROM.

The I^2C standard specification requires a pull up resistor on I2C_SDA and I2C_SCL. The I^2C port on the MSC8157/8 devices supports a maximum 400 kHz frequency, also known as I^2C fast mode. The I^2C access frequency varies depending on the following two conditions:

- The rise time, which is determined by the time constant formed by the pull up resistor and bus load capacitance.
- The low assertion duration on I2C_SCL, which is determined by the device with the longest low period. See **Section 24.4.6** *Clock Synchronization* and **Section 24.4.8** *Clock Stretching* in the reference manual for details.

The I^2C standard specification defines the maximum rise time (tr) as 300 ns and the maximum load capacitance on the bus line (Cb) as 400 pF. In order to avoid violating the specification, make sure your design follow these guidelines:

- Use a maximum 1 kΩ pull-up resistor on I2C_SCL.
- Make sure that the I2C_SCL line rise time does not violate the I^2C specification.

Do not stretch I2C_SCL while loading the RCW from I^2C.

8.7.1 I^2C Clock

I2C_SCL is selected by configuring the GPIO30 signal (see **Chapter 21,** *GPIO* in the MSC8157/8 device specific Reference Manual for details). See **Chapter 24,** *I^2C* in the MSC8157/8 device specific Reference Manual for details on the clock operation.

8.8 SPI

The MSC8157/8 SPI can be programmed to work in a single- or multiple-master environment.

8.8.1 SPI Clock

The SPI_SCK is selected by configuring the GPIO19 pin (see **Chapter 21,** *GPIO* in the device specific Reference Manual for details). The clock signal operation (clock invert, clock phase, and clock gap) are configured in the SPIMODE register (see **Section 19.8** *Serial Peripheral Interface (SPI)* in the device specific Reference Manual for details).

8.8.2 SPI as a Master Device

In master mode, the SPI sends a message to the slave peripheral, which sends back a simultaneous reply. A single-master device with multiple slaves can use general-purpose parallel I/O signals to selectively enable slaves, as shown in **Figure 14**. To eliminate the multi-master error in a single-master environment, the master $\overline{\text{SPI\_SL}}$ input can be forced inactive by clearing PAR[DD20] in the GPIO registers to 0 forcing the GPIO20/$\overline{\text{SPI\_SL}}$ signal to function as GPIO.

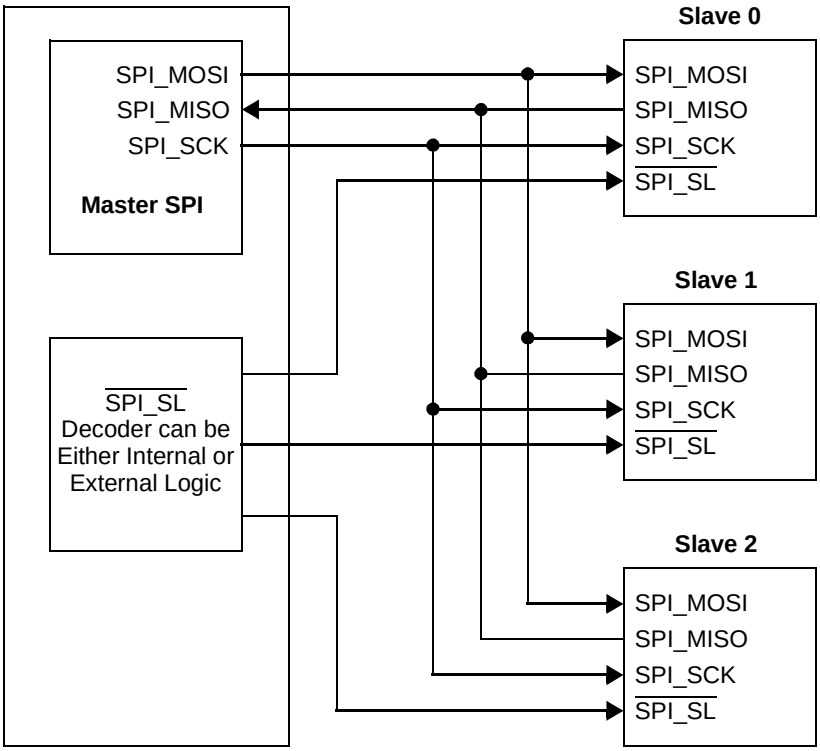
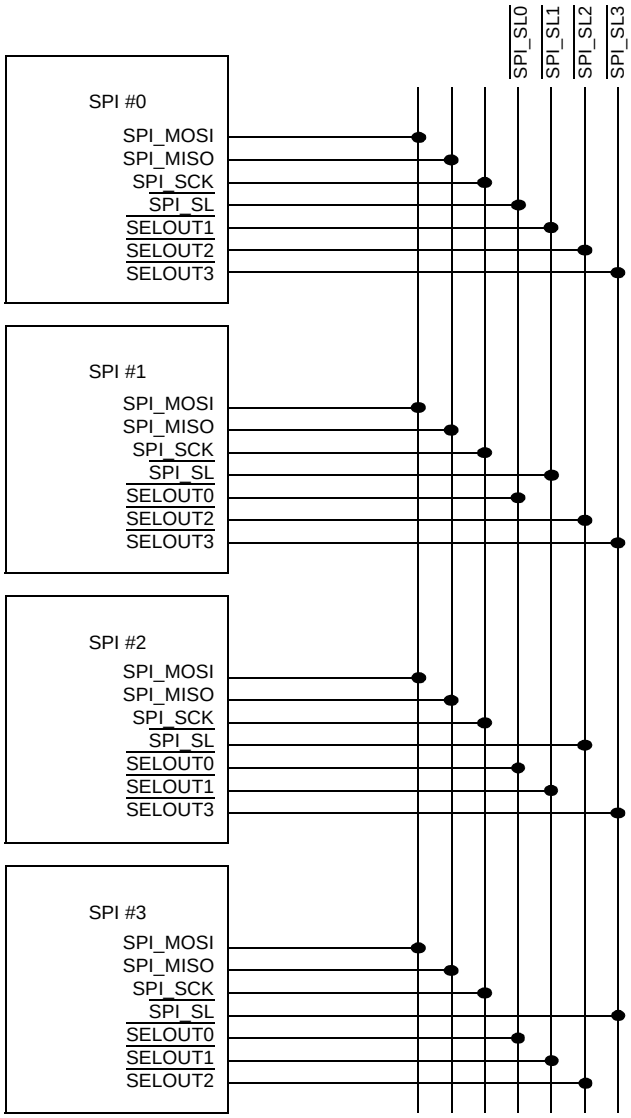


Figure 14. Single-Master/Multi-Slave Configuration

8.8.3 SPI in Multi-Master Operation

The SPI can operate in a multi-master environment in which SPI devices are connected to the same bus. In this configuration, the SPI_MOSI, SPI_MISO, and SPI_SCK signals of all SPI devices are shared. The SPI_SL inputs are connected separately, as shown in **Figure 15**. Only one SPI device at a time can act as a master—all others must be slaves.



Notes:
- All signals are open-drain
- For a multi-master system with more than 2 masters, SPI_SL and SPIE[MME] do not detect all possible conflicts.
- It is the responsibility of the software to arbitrate for the SPI bus (with token passing, for example).
- SELOUTx signals are implemented in the software using general-purpose I/O signals.

Figure 15. Multimaster Configuration

8.8.4 General SPI Guidelines

Use the following guidelines for SPI connections:

- Connect the device as shown in **Figure 14** or **Figure 15** as appropriate for your system.
- A 4.7 to 10 KΩ pull-up resistor is recommended for SPI_MISO.
- If the MSC8157/8 does not actively drive the other SPI signals, similar pull-ups are recommended for the other signals as well.
- Route SPI_SCK, SPI_MOSI, and SPI_MISO in a daisy chain fashion, keeping stubs as minimal as possible.
- Refer to the device specific data sheet from timing specifications. The maximum distance between the MSC8157/8 and other SPI devices on the SPI bus is limited by desired operating frequency.

8.9 JTAG

MSC8157/8 devices provide a JTAG interface for debugging designed to conform to the **IEEE 1149.6** specification. The interface supports the boundary scan architecture and provides access to the standard Test Access Port (TAP) controller that performs the standard JTAG tasks and provides access to the internal OCE blocks in the SC3850 cores. The device specific reference manuals provide detailed signal descriptions in **Chapter 3,** *External Signals* and a detailed functional description in **Chapter 25,** *Debugging, Profiling, and Performance Monitoring.* Signal timing specifications are listed in the device specific technical data sheet. See the MSC8157/8 device specific Reference Manual **Table 3-17**. *JTAG TAP Signals* for signal descriptions. For debugging using the CodeWarrior USB TAP controller to connect to CodeWarrior for StarCore DSP, you must use the JTAG 14-pin connector. If using more than one MSC8157/8 DSP, consider using a single JTAG connector with the DSPs connected in a JTAG chain, as shown in **Figure 16**.

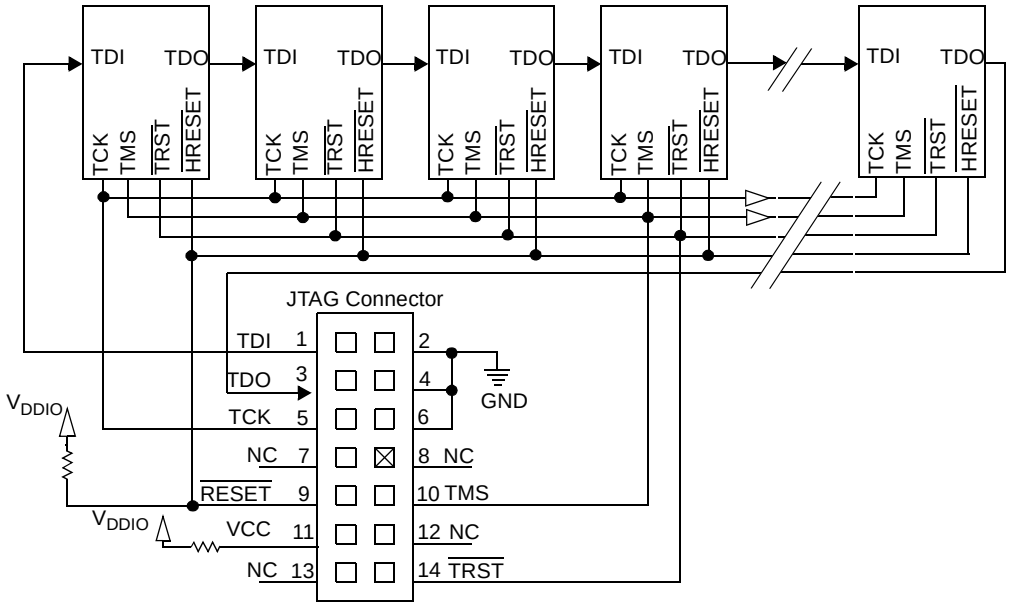


Figure 16. Multiple Target DSP Connection

Special consideration must be given to the assertion/deassertion of the $\overline{\text{TRST}}$ signal. **Section 4.6**, *Reset Flow* in this document mentions that the $\overline{\text{TRST}}$ signal must be asserted during power up. Detailed connectivity guidelines for $\overline{\text{TRST}}$ pin are described in **Section 8.9**, *JTAG* in this document.

To meet the AC timing requirements of the JTAG pins, a buffer should be placed on TCK and TMS to maintain signal integrity when there are more than four DSPs in the chain. Each buffer should drive no more than four loads. The CodeWarrior tool can change TCK frequency and the default setting for TCK frequency is 8 MHz which is slower than maximum TCK frequency specification on an MSC8157/8 device.

The V_{CC} pin (11) on the JTAG connector is merely sensed by the USB TAP. The USB TAP probe uses this signal to determine if power is applied to the target. This signal is also used as a voltage reference for the signals driven by the USB TAP probe (TDI, TCK, TMS, $\overline{\text{RESET}}$, and $\overline{\text{TRST}}$). In the MSC8157ADS, the V_{CC} pin 11 is pulled up to V_{DDIO} using a 22 Ω resistor.

The JTAG of MSC8157/8 devices runs at 2.5 V. Because the USB TAP probe automatically supports target signal levels from 1.8 V to 3.3 V, you can connect the USB TAP directly to JTAG of MSC8157/8. See page 41 in USB TAP Probe User's Guide included in Code Warrior for StarCore DSP IDE for additional details.

In **Figure 16**, all $\overline{\text{HRESET}}$ pins of the DSPs are connected to the $\overline{\text{RESET}}$ pin 9 of JTAG connector so that the debugger tool can assert $\overline{\text{HRESET}}$ to all DSPs at a time. If a user wants to assert $\overline{\text{HRESET}}$ to a specific DSP, only connect the $\overline{\text{RESET}}$ pin 9 to the $\overline{\text{HRESET}}$ of the specific DSP.

The Code Warrior for StarCore DSP tool can work on a single JTAG chain that can include multiple MSC8157/8 devices and also other type of devices, both FREESCALE and Non FREESCALE.

For additional information, see *CodeWarrior™ USB TAP Probe Users Guide* included with the Code Warrior for StarCore DSP IDE. Further information can also be found from the CW “Help” option:

```
Help -> Help Contents -> Targeting StarCore DSPs > Multi-Core Debugging > Debugging Multi-Core Projects
```

9 Boundary Scan

It is the user’s responsibility to make sure that if any device interface is not used for functional application, the generated patterns will not match the expected values for these pins. The BSDL supplied by Freescale assumes all device pins are included.

10 Identifying the Device ID and Revision Number

The MSC8157/8 devices have several places which carry the Device ID and Revision Number information. The following tables summarizes all the locations where software can explore the Device ID and Revision Number and identify the device type and mask set accordingly.

Table 18. MSC8157/8 Rev0 Device ID and Revision Number Sources

Device	SRIO		PEX		GCR		JTAG
	DIDCAR[DI]	DICAR[DR]	Device ID [1]	Revision ID [2]	SPRIDR[PARTID] [3]	SPRIDR[REVID]	JTAGID [4]
8157	0x1828	0	0x1828	0	0x8305	0	0x0188401D
8157E	0x182A	0	0x182A	0	0x830D	0	0x0188401D
8158	0x181C	0	—		0x8303	0	0x0189901D
8158E	0x181E	0	—		0x830B	0	0x0189901D

1 PCI Express Device ID is accessed at offset 0x02 for common PCI configuration registers.
2 PCI Express Revision ID is accessed at offset 0x08 for common PCI configuration registers.
3 SPRIDR resides at address 0xFFF28028.
4 JTAGID is accessed by JTAG initiator through the Test Access Port (TAP).

11 Signals Connection Summary

Table 19 summarizes the functional signals connection recommendation for MSC8157/8. The order of the signals listed in **Table 19** is the same as listed in the Pin Multiplexing Tool discussed in **Section 7.4** *Pin Multiplexing Tool*. Use the following general notes for **Table 19**:

1. GND indicates using a 10 KΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
2. VDD indicates using a 10 KΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor is indicated as “pull-up/pull-down”.
4. NC indicates “Not Connected” and means do not connect anything to the pin.

Refer to the Chapter **3** in the device specific Reference Manual for details on the external signals.

Table 19. MSC8157/8 Pin Connection Summary

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
Reset					
CLKIN	CLKIN	QVDD	—	—	See **Section 4.2** *Clock, Reset, and Supply Coordination* in Design Checklist
CLKOUT	—	QVDD	NC	—	
Reset					

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
PORESET	PORESET	QVDD	—	—	See **Section 4.2** *Clock, Reset, and Supply Coordination* in Design Checklist
HRESET	HRESET	QVDD	—	Pull Up	
HRESET_IN	HRESET_IN	QVDD	NC	—	
STOP_BS	VDD/GND	QVDD	GND	—	Used when loading RCW from an I^2C EEPROM.
NMI and INT_OUT					
INT_OUT /CP_TX_INT	—	QVDD	NC	Pull Up	
NMI	—	QVDD	VDD	—	
NMI_OUT/CP_RX_INT	—	QVDD	NC	Pull Up	
PORESET Configuration, GPIO, IRQ, CPRI Sync and Timer					
RC21	RC21	NVDD	GND	Pull up/down depends on needed value in case using RCx functionality. Pull up is needed in case using GPIO with open drain functionality enabled	**RCx** is used when loading RCW from external pins using reduced mode. **RCW_LSEL_x** is used when loading RCW using multiplexed mode.
RCW_LSEL_0/RC17	RCW_LSEL_0/ RC17	NVDD	GND		
RCW_LSEL_1/RC18	RCW_LSEL_1/ RC18	NVDD	GND		
RCW_LSEL_2/RC19	RCW_LSEL_2/ RC19	NVDD	GND		
RCW_LSEL_3/RC20	RCW_LSEL_3/ RC20	NVDD	GND		
GPIO0/IRQ0/RC0/CP_SYNC1	RC0	NVDD	NC		
GPIO1/IRQ1/RC1/CP_SYNC2	RC1	NVDD	NC		
GPIO2/IRQ2/RC2/CP_SYNC3	RC2	NVDD	NC		
GPIO3/DRQ1/IRQ3/RC3	RC3	NVDD	NC		

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
GPIO4/DDN1/IRQ4/RC4	RC4	NVDD	NC	Pull up/down depends on needed value in case using RCx functionality. Pull up is needed in case using GPIO with open drain functionality enabled	**RCx** is used when loading RCW from external pins using reduced mode. **RCW_LSEL_x** is used when loading RCW using multiplexed mode.
GPIO5/IRQ5/RC5/CP_SYNC4	RC5	NVDD	NC		
GPIO6/IRQ6/RC6/CP_SYNC5	RC6	NVDD	NC		
GPIO7/IRQ7/RC7/CP_SYNC6	RC7	NVDD	NC		
GPIO8/IRQ8/RC8	RC8	NVDD	NC		
GPIO9/IRQ9/RC9	RC9	NVDD	NC		
GPIO10/IRQ10/RC10	RC10	NVDD	NC		
GPIO11/IRQ11/RC11	RC11	NVDD	NC		
GPIO12/IRQ12/RC12	RC12	NVDD	NC		
GPIO13/IRQ13/RC13	RC13	NVDD	NC		
GPIO14/DRQ0/IRQ14/RC14	RC14	NVDD	NC		
GPIO15/DDN0/IRQ15/RC15	RC15	NVDD	NC		
GPIO16/TMR5/RC16	RC16	NVDD	NC		
SPI and GPIO					
GPIO17/SPI_SCK/CP_LOS3	—	NVDD	NC	Pull up is needed in case using GPIO with open drain functionality enabled	See **Section 8.8** *SPI* in Design Checklist
GPIO18/SPI_MOSI/CP_LOS4	—	NVDD	NC		
GPIO19/SPI_MISO/CP_LOS5	—	NVDD	NC		
GPIO20/SPI_SL/CP_LOS6	—	NVDD	NC		
Timers and GPIO					
GPIO21/TMR6	—	NVDD	NC	Pull up is needed in case using GPIO with open drain functionality enabled	
GPIO22	—	NVDD	NC		
GPIO23/TMR0 /BOOT_SPI_SL	—	NVDD	NC		
GPIO24/TMR1/RCW_SRC2	RCW_SRC2	NVDD	NC		
GPIO25/TMR2/RCW_SRC1	RCW_SRC1	NVDD	NC		
GPIO26/TMR3	—	NVDD	NC		
GPIO27/TMR4/RCW_SRC0	RCW_SRC0	NVDD	NC		
UART and GPIO					

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
GPIO28/UART_RXD /CP_LOS1	—	NVDD	NC	Pull up is needed in case using GPIO with open drain functionality enabled	See **Section 8.6** *UART* in Design Checklist
GPIO29/UART_TXD/CP_LOS2	—	NVDD	NC	Pull Up for UART_TXD functionality Pull up is needed in case using GPIO with open drain functionality enabled	
I^2C and GPIO					
GPIO30/I2C_SCL	—	NVDD	NC	Pull Up with 1 kΩ resistor for I2C functionality Pull up is needed in case using GPIO with open drain functionality enabled	Used during PORESET flow when loading RCW from an I^2C EEPROM. See **Section 8.7** *I^2C* in Design Checklist
GPIO31/I2C_SDA	—	NVDD	NC	Pull up is needed in case using GPIO with open drain functionality enabled	
RGMII					
GE2_RD2/CP_LOS1	—	NVDD	GND	—	For RGMII, see **Section 8.5.3** *RGMII Considerations* in DCL. The column "Connection if not used" relates to the case the RGMII functionality is not used. In that case, the connection to GND or NC depends how the interface is defined during PORESET by the RCWHR register fields GE1 and GE2.
GE2_RD3/CP_LOS2	—	NVDD	GND	—	
GE2_TD2/CP_LOS3	—	NVDD	GND	—	
GE2_GTX_CLK/CP_LOS4	—	NVDD	GND	—	
GE2_TD3/CP_LOS5	—	NVDD	GND	—	
GE2_RD0/CP_LOS6	—	NVDD	GND	—	
GE2_RD1	—	NVDD	GND	—	
GE2_TX_CLK	—	NVDD	GND	—	
GE2_RX_CTL	—	NVDD	GND	—	
GE2_RX_CLK	—	NVDD	GND	—	
GE2_TD0	—	NVDD	NC	—	
GE2_TD1	—	NVDD	NC	—	
GE2_TX_CTL	—	NVDD	NC	—	

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
GE1_TD0	—	NVDD	NC	—	For RGMII, see **Section 8.5.3** *RGMII Considerations* in Design Checklist The column "Connection if not used" relate to the case where the RGMII functionality is not used. In that case, the connection to GND or NC depends how the interface is defined during PORESET by the RCWHR register fields GE1 and GE2.
GE1_TD1	—	NVDD	NC	—	
GE1_TD2	—	NVDD	NC	—	
GE1_TD3	—	NVDD	NC	—	
GE1_TX_CLK	—	NVDD	NC	—	
GE1_TX_CTL	—	NVDD	NC	—	
GE1_GTX_CLK	—	NVDD	NC	—	
GE1_RD0	—	NVDD	GND	—	
GE1_RD1	—	NVDD	GND	—	
GE1_RD2	—	NVDD	GND	—	
GE1_RD3	—	NVDD	GND	—	
GE1_RX_CLK	—	NVDD	GND	—	
GE1_RX_CTL	—	NVDD	GND	—	
GE_MDC	—	NVDD	NC	—	See **Section 8.5.2** *General Ethernet Guidelines* in Design Checklist
GE_MDIO	—	NVDD	NC	—	
OCE and JTAG					
DFT_TEST	—	QVDD	GND	—	
EE0	—	QVDD	GND	—	
EE1	—	QVDD	NC	—	
TCK	—	QVDD	GND	—	See **Section 8.8** *SPI* in Design Checklist
$\overline{\text{TRST}}$	—	QVDD	GND	—	
TMS	—	QVDD	GND	—	
TDI	—	QVDD	GND	—	
TDO	—	QVDD	NC	—	
DDR					
MCLKIN	—	GVDD	GND	—	Optional
MAPAR_OUT	—	GVDD	NC	—	
MAPAR_IN	—	GVDD	GND/VDDDDR/NC	—	
MA0	—	GVDD	NC	—	
MA1	—	GVDD	NC	—	
MA2	—	GVDD	NC	—	

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
MA3	—	GVDD	NC	—	
MA4	—	GVDD	NC	—	
MA5	—	GVDD	NC	—	
MA6	—	GVDD	NC	—	
MA7	—	GVDD	NC	—	
MA8	—	GVDD	NC	—	
MA9	—	GVDD	NC	—	
MA10	—	GVDD	NC	—	
MA11	—	GVDD	NC	—	
MA12	—	GVDD	NC	—	
MA13	—	GVDD	NC	—	
MA14	—	GVDD	NC	—	
MA15	—	GVDD	NC	—	
MBA0	—	GVDD	NC	—	
MBA1	—	GVDD	NC	—	
MBA2	—	GVDD	NC	—	
$\overline{\text{MCAS}}$	—	GVDD	NC	—	
MCKE0	—	GVDD	NC	—	
MCKE1	—	GVDD	NC	—	
$\overline{\text{MCK0}}$	—	GVDD	NC	—	
$\overline{\text{MCK1}}$	—	GVDD	NC	—	
$\overline{\text{MCK2}}$	—	GVDD	NC	—	
MCK0	—	GVDD	NC	—	
MCK1	—	GVDD	NC	—	
MCK2	—	GVDD	NC	—	
MCK3	—	GVDD	NC	—	
$\overline{\text{MCS0}}$	—	GVDD	NC	—	
$\overline{\text{MCS1}}$	—	GVDD	NC	—	

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
MDQ0	—	GVDD	NC	—	See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ1	—	GVDD	NC	—	
MDQ2	—	GVDD	NC	—	
MDQ3	—	GVDD	NC	—	
MDQ4	—	GVDD	NC	—	
MDQ5	—	GVDD	NC	—	
MDQ6	—	GVDD	NC	—	
MDQ7	—	GVDD	NC	—	
MDQ8	—	GVDD	NC	—	See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ9	—	GVDD	NC	—	
MDQ10	—	GVDD	NC	—	
MDQ11	—	GVDD	NC	—	
MDQ12	—	GVDD	NC	—	
MDQ13	—	GVDD	NC	—	
MDQ14	—	GVDD	NC	—	
MDQ15	—	GVDD	NC	—	
MDQ16	—	GVDD	NC	—	See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ17	—	GVDD	NC	—	
MDQ18	—	GVDD	NC	—	
MDQ19	—	GVDD	NC	—	
MDQ20	—	GVDD	NC	—	
MDQ21	—	GVDD	NC	—	
MDQ22	—	GVDD	NC	—	
MDQ23	—	GVDD	NC	—	

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
MDQ24	—	GVDD	NC	—	See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ25	—	GVDD	NC	—	
MDQ26	—	GVDD	NC	—	
MDQ27	—	GVDD	NC	—	
MDQ28	—	GVDD	NC	—	
MDQ29	—	GVDD	NC	—	
MDQ30	—	GVDD	NC		
MDQ31	—	GVDD	NC		
MDQ32	—	GVDD	NC		See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ33	—	GVDD	NC		
MDQ34	—	GVDD	NC		
MDQ35	—	GVDD	NC		
MDQ36	—	GVDD	NC		
MDQ37	—	GVDD	NC		
MDQ38	—	GVDD	NC		
MDQ39	—	GVDD	NC		
MDQ40	—	GVDD	NC		See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ41	—	GVDD	NC		
MDQ42	—	GVDD	NC		
MDQ43	—	GVDD	NC		
MDQ44	—	GVDD	NC		
MDQ45	—	GVDD	NC		
MDQ46	—	GVDD	NC		
MDQ47	—	GVDD	NC		

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
MDQ48	—	GVDD	NC		See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ49	—	GVDD	NC		
MDQ50	—	GVDD	NC		
MDQ51	—	GVDD	NC		
MDQ52	—	GVDD	NC		
MDQ53	—	GVDD	NC		
MDQ54	—	GVDD	NC		
MDQ55	—	GVDD	NC		
MDQ56	—	GVDD	NC		See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MDQ57	—	GVDD	NC		
MDQ58	—	GVDD	NC		
MDQ59	—	GVDD	NC		
MDQ60	—	GVDD	NC		
MDQ61	—	GVDD	NC		
MDQ62	—	GVDD	NC		
MDQ63	—	GVDD	NC		
MDM0	—	GVDD	NC		
MDM1	—	GVDD	NC		
MDM2	—	GVDD	NC		
MDM3	—	GVDD	NC		
MDM4	—	GVDD	NC		
MDM5	—	GVDD	NC		
MDM6	—	GVDD	NC		
MDM7	—	GVDD	NC		
MDM8	—	GVDD	NC		
$\overline{\text{MDQS0}}$	—	GVDD	NC		
$\overline{\text{MDQS1}}$	—	GVDD	NC		
$\overline{\text{MDQS2}}$	—	GVDD	NC		
$\overline{\text{MDQS3}}$	—	GVDD	NC		
$\overline{\text{MDQS4}}$	—	GVDD	NC		
$\overline{\text{MDQS5}}$	—	GVDD	NC		

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
$\overline{\text{MDQS6}}$	—	GVDD	NC		
$\overline{\text{MDQS7}}$	—	GVDD	NC		
$\overline{\text{MDQS8}}$	—	GVDD	NC		
MDQS0	—	GVDD	NC		
MDQS1	—	GVDD	NC		
MDQS2	—	GVDD	NC		
MDQS3	—	GVDD	NC		
MDQS4	—	GVDD	NC		
MDQS5	—	GVDD	NC		
MDQS6	—	GVDD	NC		
MDQS7	—	GVDD	NC		
MDQS8	—	GVDD	NC		
MECC0	—	GVDD	NC		See **Section 8.3.2** *DDR Data Bits Connectivity* in the Design Checklist
MECC1	—	GVDD	NC		
MECC2	—	GVDD	NC		
MECC3	—	GVDD	NC		
MECC4	—	GVDD	NC		
MECC5	—	GVDD	NC		
MECC6	—	GVDD	NC		
MECC7	—	GVDD	NC		
MMDIC0	—	GVDD	NC	Pull Down to GND with 36 Ω resistor	See **Section 8.3.3** *Memory Signal Termination* in the Design Checklist
MMDIC1	—	GVDD	NC	Pull Up to VDDDDR with 36 Ω resistor	
$\overline{\text{MRAS}}$	—	GVDD	NC		
$\overline{\text{MWE}}$	—	GVDD	NC		
MODT0	—	GVDD	NC		
MODT1	—	GVDD	NC		
HSSI					

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
SD_IMP_CAL_RX	—	SXCVDD	GND	Pull Up to SXCVDD with 200 Ω resistor	See **Section 8.4.1** *Impedance Calibration Signals* in Design Checklist
SD_IMP_CAL_TX	—	SXPVDD	GND	Pull Up to SXPVDD with 200 Ω resistor	
SD_REF_CLK1	—	SXCVDD	SXCVSS	—	See **Section 8.4.2** *SerDes Reference Clocks Guidelines* in Design Checklist
$\overline{\text{SD\_REF\_CLK1}}$	—	SXCVDD	SXCVSS	—	
SD_REF_CLK2	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_REF\_CLK2}}$	—	SXCVDD	SXCVSS	—	
SD_A_RX	—	SXCVDD	SXCVSS	—	**Not available on MSC8158/E.** See **Section 8.4.3** *SerDes Data Lane Guidelines* in the Design Checklist
$\overline{\text{SD\_A\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_B_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_B\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_C_RX	—	SXCVDD	SXCVSS	—	See **Section 8.4.3** *SerDes Data Lane Guidelines* in the Design Checklist
$\overline{\text{SD\_C\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_D_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_D\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_E_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_E\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_F_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_F\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_G_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_G\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_H_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_H\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_I_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_I\_RX}}$	—	SXCVDD	SXCVSS	—	
SD_J_RX	—	SXCVDD	SXCVSS	—	
$\overline{\text{SD\_J\_RX}}$	—	SXCVDD	SXCVSS	—	

Table 19. MSC8157/8 Pin Connection Summary (continued)

Pin Name	Usage during PORESET Configuration flow	Reference Supply	Connection If not used	Require external pull up/down when used	Comments
SD_A_TXD	—	SXPVDD	NC	—	**Not available on MSC8158/E.** See **Section 8.4.3** *SerDes Data Lane Guidelines* in the Design Checklist
$\overline{\text{SD\_A\_TXD}}$	—	SXPVDD	NC	—	
SD_B_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_B\_TXD}}$	—	SXPVDD	NC	—	
SD_C_TXD	—	SXPVDD	NC	—	See **Section 8.4.3** *SerDes Data Lane Guidelines* in the Design Checklist
$\overline{\text{SD\_C\_TXD}}$	—	SXPVDD	NC	—	
SD_D_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_D\_TXD}}$	—	SXPVDD	NC	—	
SD_E_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_E\_TXD}}$	—	SXPVDD	NC	—	
SD_F_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_F\_TXD}}$	—	SXPVDD	NC	—	
SD_G_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_G\_TXD}}$	—	SXPVDD	NC	—	
SD_H_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_H\_TXD}}$	—	SXPVDD	NC	—	
SD_I_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_I\_TXD}}$	—	SXPVDD	NC	—	
SD_J_TXD	—	SXPVDD	NC	—	
$\overline{\text{SD\_J\_TXD}}$	—	SXPVDD	NC	—	

12 Revision History

Table 20. Document Revision History

Rev.	Date	Change
0	Nov 2011	Initial release.
1	Dec 2011	Added a note at the end of **Section 8.5.3**, *RGMII Considerations* describing special board layout considerations.

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