NXP Semiconductors
Application Note

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MC33978 low-power mode operation

1 Introduction

The MC33978 is a 22 channel switch detection interface designed to monitor multiple system switches and communicate its open/close status via SPI communication protocol. The MC33978 targets various applications such as body control modules, Smart junction Box, and power train controllers in auto applications, as well as machine tool control, PLC controllers, among other industrial applications. NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow integrating precision analog, power functions and dense CMOS logic together on a single cost-effective die.

The purpose of this document is to provide a more detailed description of the LPM (Low-power mode) operation on the MC33978. It explains each programmable feature during LPM, as well as how these parameters affect the performance of the device during stand-by operation and switch detection in LPM.

Contents

2 MC33978 device description

MC33978 features 22 input channels from which, 14 are dedicated Switch-to-Ground (SG) current source, and 8 are programmable inputs (SP) which can be programmed as a Switch-to-Ground (SG) current source or a Switch-to-Battery (SB) current sink. NXP's MC33978 integrates flexible operating modes to improve the overall power consumption during normal operation, as well as providing a superior power consumption and thermal performance during sleep (low-power consumption) conditions.

During the Normal mode, the device is able to be programmed and provide the registers and switches status through SPI protocol, along with detecting a change of status (close or open) on any of the input channels. During the LPM, the operating device has a minimum current consumption state while still being able to detect switch status change at any time. Figure 1 shows a typical application diagram for the MC33978.

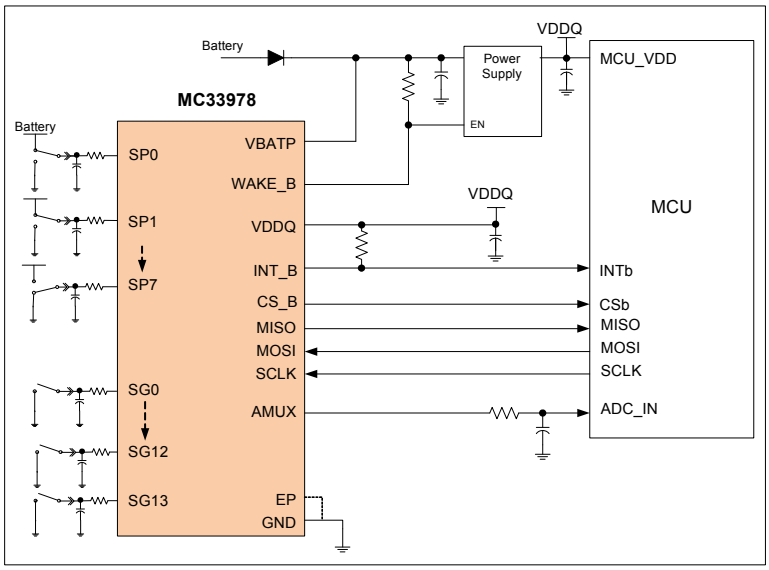

Figure 1. Application diagram

3 Understanding the low-power mode operation

The LPM may be entered only by sending the Enter Low-power mode command. All register settings programmed in Normal mode are maintained while in LPM. Upon an “Enter LPM” SPI command, the device enters into a minimal current consumption state by disconnecting unnecessary blocks for this operation mode. The SPI communication, analog multiplexer block and the fault detection block are disabled. The AMUX pin is tristated as well as the MISO pin, to ensure no false communication is transmitted during LPM. Since the Fault Detection block is not functional during LPM, if a fault condition occurs while the device is in LPM, it is not detected nor stored in the Fault Status Register.

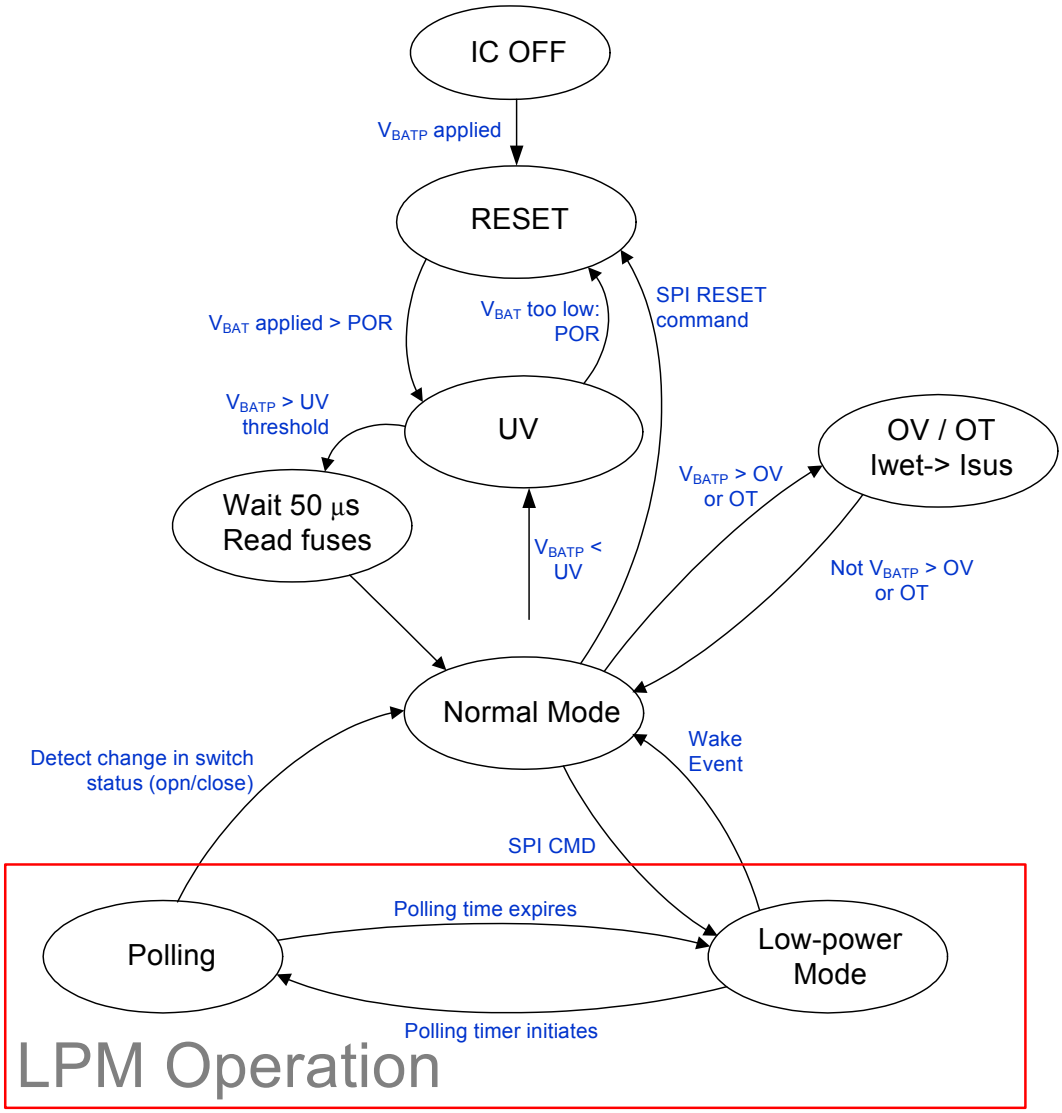

Figure 2. MC33978 state machine

When the MC33978 is in LPM, it uses a polling mode which periodically (selectable in LPM config register) interrogates the input pins to determine in what state the pins are, and decide if there was a change of state from when the chip was in Normal mode. This mode forces the device into a “Virtually Active” condition during TACTIVEPOLL and uses the current sources to pull-up (SG) or down (SB) to determine if a switch is open or closed, as shown in Figure 3.

After the polling ends, if no change was detected, the chip returns to the Low-power mode, in which everything is shutdown and the device consumes a typical current of ~20 µA.

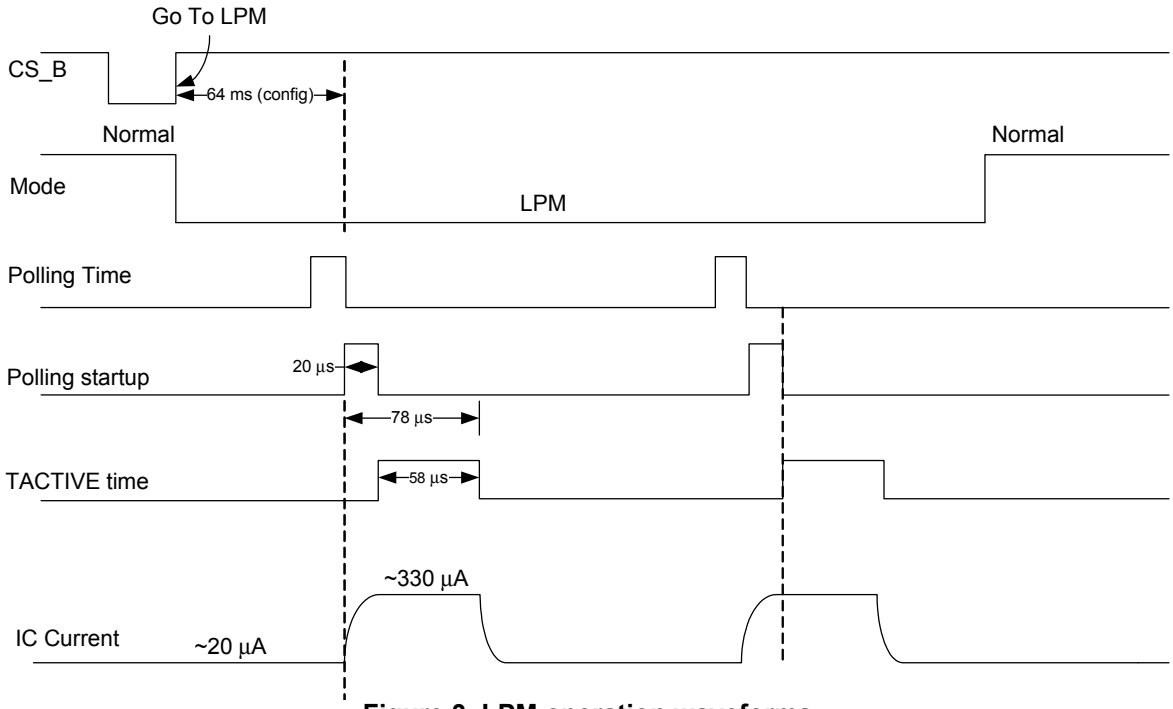

Figure 3. LPM operation waveforms

If a change of state is detected during the LPM operation, the device returns to the normal mode and triggers an interrupt to inform it has awakened and action is needed by the MCU. The MC33978 may wake-up from LPM and enter Normal mode when any of the following events occur:

- Input switch change of state (when enabled)
- Interrupt timer expire
- Falling edge of WAKE_B (as set by the device configuration register)
- Falling edge of INT_B (with VDDQ = 5.0 V)
- Falling edge of CS_B (with VDDQ = 5.0 V)
- Power-ON Reset (POR)

The V_{DDQ} supply may be removed from the device during LPM, however removing V_{DDQ} from the device disables a wake-up from the falling edge of INT_B and CS_B. The IC checks the status of V_{DDQ} after a falling edge of WAKE_B (as selected in the device configuration register), INT_B, and CS_B. If V_{DDQ} is low, the IC returns to LPM and does not report a Wake event. If the V_{DDQ} is high, the IC wakes up and reports the Wake event.

In cases where CS_B is used to wake the device, the first MISO data message is not valid.

In cases of a low VBATP, the polling pauses and waits until the V_{BATP} rises out of UV or a POR occurs. The pause of the polling ensures all of the internal rails, currents, and thresholds are up at the required levels to accurately detect open or closed switches. The chip does not wake-up in this condition and simply waits for the V_{BATP} voltage to rise or cause a POR.

There are many configurations affecting the Low-power mode operation on the MC33978. The following features can be modified to provide flexibility during the Low-power mode:

- Polling rate
- Slow polling
- Interrupt Timer
- Wake-up enable
- Polling Current level
- Comparator Only
- LPM voltage threshold configuration
- Wake-up debounce

3.1 Polling rate and slow polling

The Polling Rate Register is used to set the frequency of the polling pulse during the LPM. The polling rate can be programmed from 3.0 ms to 128 ms, as described in Table 1.

Table 1. Polling rate configuration bits

Polling rate configuration [LPM configuration register 0x1E / 0x1F]				
Bit	**Functions**	**Default Value**	**Description**	
3 - 0	poll[3-0]	1111	0000 - 3.0 ms 0001 - 6.0 ms 0010 - 12 ms 0011 - 24 ms 0100 - 48 ms 0101 - 68 ms 0110 - 76 ms 0111 - 128 ms	1000 - 32 ms 1001 - 36 ms 1010 - 40 ms 1011 - 44 ms 1100 - 52 ms 1101 - 56 ms 1110 - 60 ms 1111 - 64 ms (default)

In addition, a slow polling rate operation is selectable for each individual channel. By setting the corresponding bit on the slow polling register (0x30/31 and 0x32/33), the polling frequency is four times slower.

The selection of the proper polling rate and slow polling option must be made, considering the latency and power consumption allowed in the system. Reducing the polling rate, increments the latency time for switch detection but it reduces the power consumption during the LPM. therefore, proper analysis must be made to find the best balance between power consumption and switch detection latency for each specific application, as shown in Figure 4.

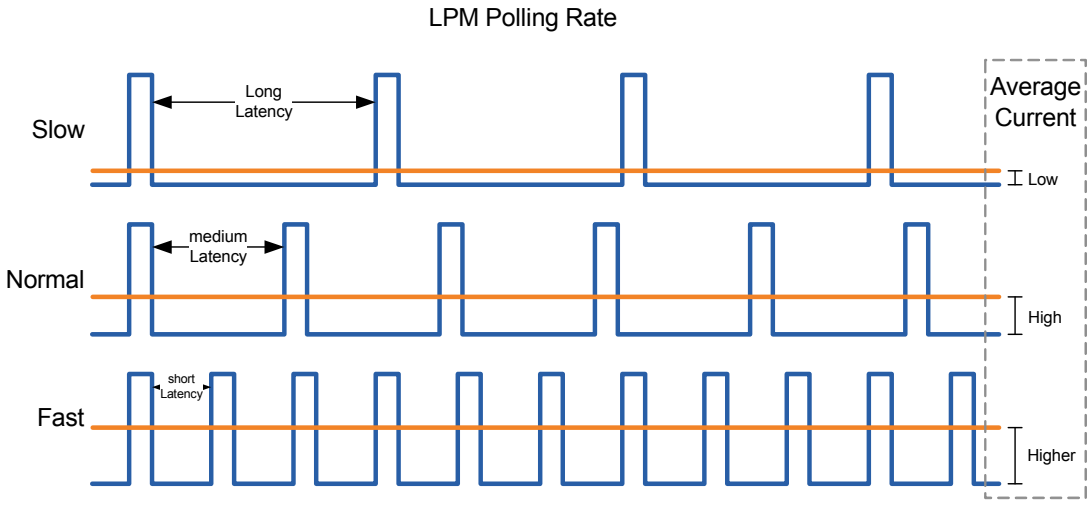

Figure 4. Polling current vs. switch detection latency

3.2 Interrupt timer

With the interrupt timer set, the IC wakes up after the selected timer expires and triggers an interrupt. This is useful in applications requiring a constant monitoring of the MC33978 switch status register or the configuration registers to ensure proper configuration at all times. This register can be selected to be OFF if this feature is not required by the application.

Table 2. Interrupt timer bits

Interrupt timer [LPM configuration register 0x1E / 0x1F]				
Bit	**Functions**	**Default value**	**Description**	
7 - 4	int[3-0]	0000	• 0000 - OFF • 0001 - 6.0 ms • 0010 - 12 ms • 0011 - 24 ms • 0100 - 48 ms • 0101 - 96 ms • 0110 - 192 ms • 0111 - 394 ms	• 1000 - 4.0 ms • 1001 - 8.0 ms • 1010 - 16 ms • 1011 - 32 ms • 1100 - 64 ms • 1101 - 128 ms • 1110 - 256 ms • 1111 - 512 ms

3.3 Wake-up enable

The MC33978 can disable each one of the channels from waking up during LPM operation by writing a 0 on the wake-up enable bits. By disabling the Wake-up function, the corresponding SG/SB circuit is not powered and is removed from the polling cycle, and thus not contributing to the total polling current. If a switch change occurs on disabled channels, the device does not detect it and remains in LPM.

If all channels are wake-up disabled, the polling circuit is turned off, and the quiescent current of the device during LPM operation is the lowest current possible. Beware that no switch detection is possible during LPM when all Wake-up channels are turned off. However, the device can still be awakened, by all the wake-up mechanisms described above.

3.4 Low-power mode current level

When a switch is closed during the Low-power mode, by default the MC33978 provides a polling current of 1.0 mA on SG channels and 2.2 mA on SB channels for the duration of the polling pulse. By setting the corresponding bit on the Polling current configuration registers to [1], the corresponding channels poll at the wetting current level set during the normal mode operation for the respective channels.

3.5 Comparator only

The Comparator Only register allows the input comparators to be active during LPM operation with no polling current. When the bits on the Comparator Only register are set to [1], the corresponding input uses a switch detection threshold of $V_{ICTH2P5}$ = 2.5 V, instead of the 4.0 V detection threshold. In this Operating mode, the input is planned to receive a digital logic level signal and wake-up on a change of state.

3.6 Low-power mode voltage threshold

The MC33978 is able to use different voltage thresholds to wake-up from LPM operation. On SG channels, a Logic [0] means the input uses the LPM delta voltage threshold (VICTHRLPM = 200 mV typically) to determine the state of the switch. A Logic [1] means the input uses the Normal threshold (VICTHR = 4.0 V) to determine the state of the switch.

SB channels only uses the 4.0 V threshold regardless the status of the LPM voltage threshold bit. The user must ensure the correct current level is set to allow the crossing of the normal mode threshold on an SB channel.

3.7 Low-power mode wake-up debounce

The IC is able to extend the time the active polling takes place to ensure a true change of state has occurred in LPM operation and reduced the chance noise has impacted the measurement. If this bit is [0], the IC uses only the Delta-V technique to determine if a switch has changed sate. If this bit is set to [1], the IC debounces the measurement by continuing to source the LPM polling current for an additional 1.2 ms and take the measurement based on the final voltage level. This helps to ensure the switch is detected correctly in noisy systems. Figure 5 through Figure 8 show the waveforms for switch detection with and without the Debounce feature for both SG and SB channels.

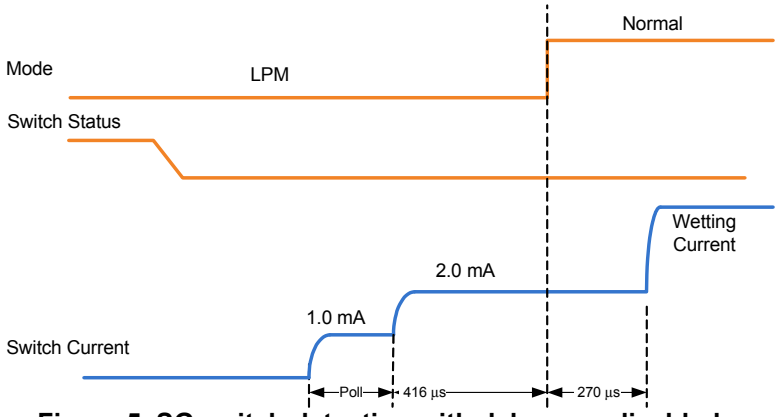

Figure 5. SG switch detection with debounce disabled

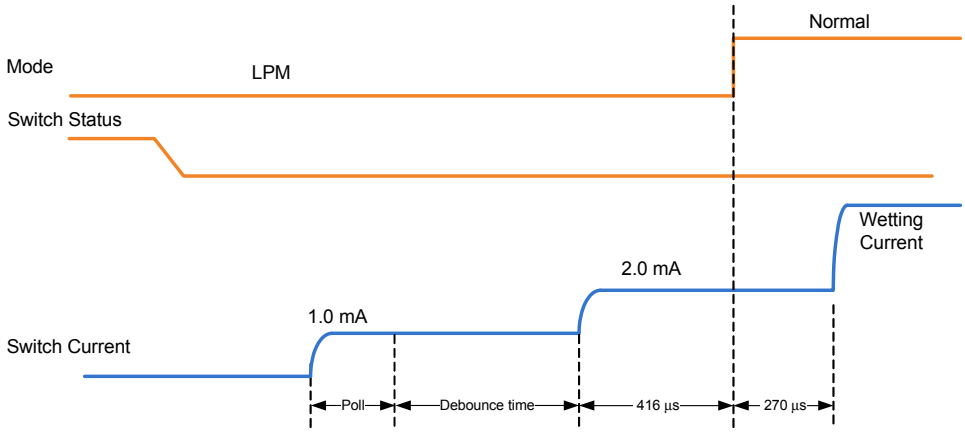

Figure 6. SG switch detection with debounce enabled

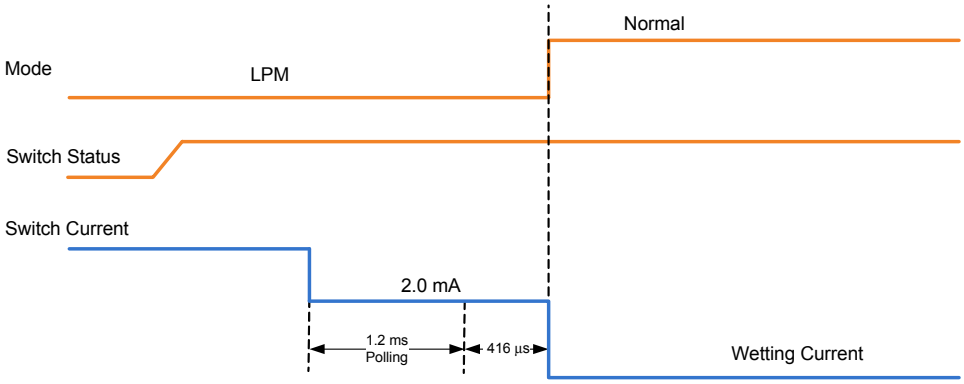

Figure 7. SB switch detection with debounce disabled

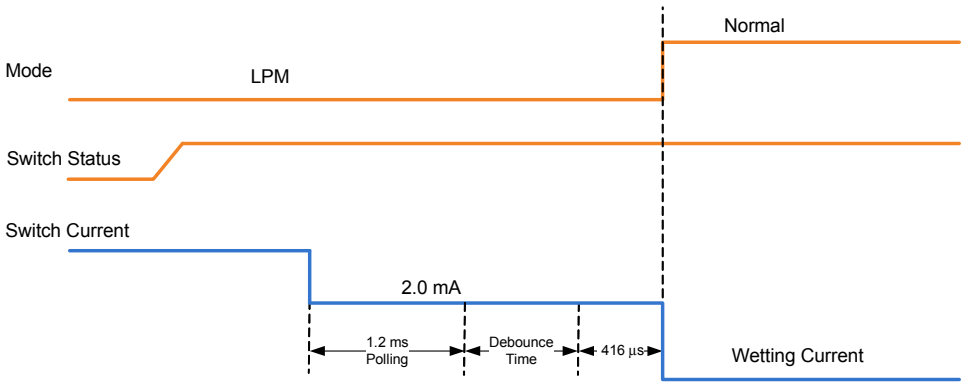

Figure 8. SB switch detection with debounce enabled

4 Switch detection in low-power mode

In the LPM operation, a switch change of status is detected only during the next available polling cycle after the switch change has occurred. Therefore, the latency of a switch detection is directly dependent on the Polling rate programmed in the MC33978.

A “Delta-V” detection mechanism is implemented on SG channels to monitor if the switch is closed or open, and the internal logic takes this information to decide whether there has been a change of state or not, and act accordingly. When the polling pulse starts, the MC33978 measures and latches the initial voltage on the input pin while the Polling current is forced to flow through the input pin; at this point, it performs an early check, comparing against the 4.0 V detection threshold. If the input is determined to meet the open condition (when entering LPM), and remains open on the polling event, the chip terminates the polling event earlier for that input(s) to lower current in the chip. If the signal does not meet the open condition during the early check, it continues with the polling pulse. At the end of the polling period, the MC33978 measures the final voltage at the input pin and compares whether the Differential Voltage (ΔV) is higher or lower than the LPM switch detection threshold (typ 0.2 V), as shown in Figure 9.

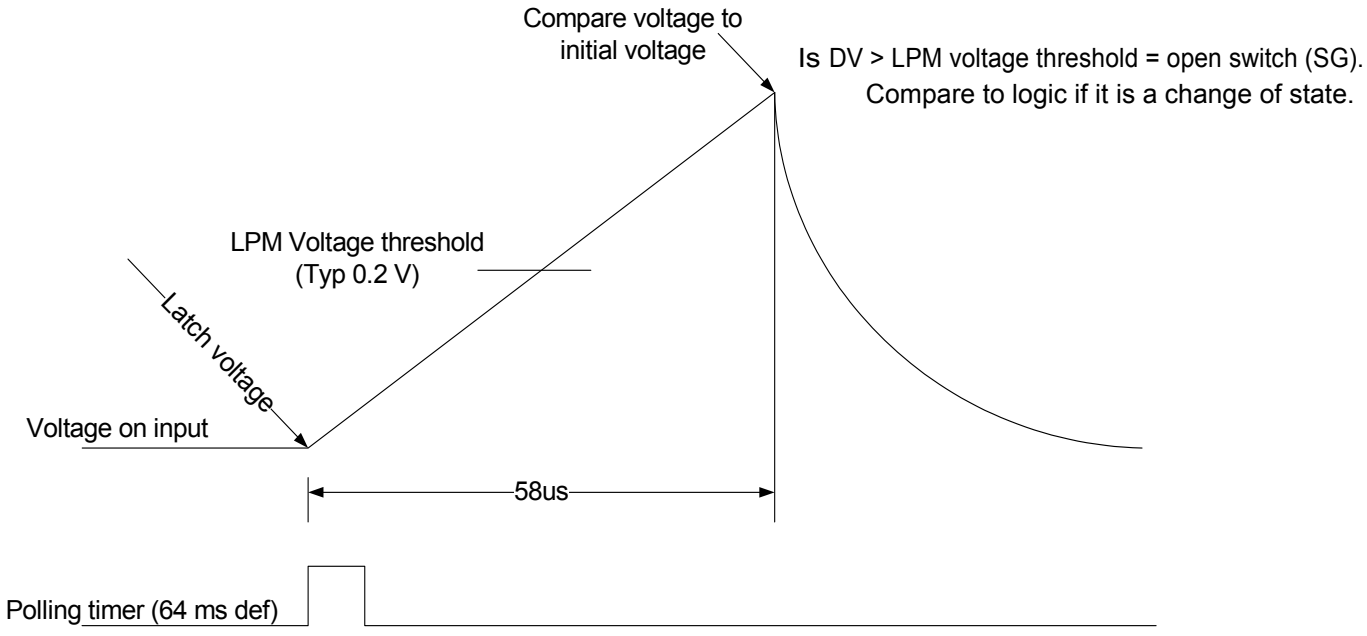

Figure 9. Delta-V detection mechanism

Table 3 shows the logical process to identify a close/open switch on SG channels.

Table 3. Switch status detection method

Channel type	Switch status	Initial voltage	Final voltage	ΔV	Input capacitor	Comments
SG	Close	GND	GND	~0 V	Does not Charge	When the switch is closed to ground, polling current goes straight to ground and the input capacitor does not get charged. There is no Delta-V and the device detects a closed condition.
	Open	≥ 0 V	~8.0 V	≥ 0.2 V	Charged to the current source voltage (~8.0 V)	When the switch is open, the input pin is floating to the voltage held by the input capacitor. During the Low-power mode, the capacitor is discharged to a certain level, and when the polling current is activated, it charges the capacitor back to ~8.0 V level and detects an open condition. If the capacitor does not discharge below the 4.0 V threshold, the device detects the open condition during the early check, and terminates the polling pulse early to reduce current consumption.

The MC33978 only provides the 4.0 V detection threshold to compare the voltage on the input pin for SB channels. When the Switch is closed to Battery, the input capacitor is charged to battery voltage, and detected as a closed circuit, as long as the input pin is higher than 4.0 V. When the Switch is open, the internal pull-down force the voltage to go to GND. When the input pin crosses the 4.0 V, the MC33978 detects an open switch and acts accordingly.

The SB channels, by default, use a polling timer of 1.2 ms. During the LPM operation, the device has this time to allow the input capacitor to charge or discharge and cross the 4.0 V detection threshold and detect the change of state. From a close to open state, the device needs to pull down the voltage stored on the input capacitor when the current source is activated on the polling cycle. Since the input capacitor could charge as high as 36 V, it requires enough time to be depleted and be able to cross the 4.0 V detection threshold.

By using the 1.2 ms timer, the power consumption is higher than it would usually be for an SG channels. If the system is required to operate with lower power consumption, the MC33978 provides the ability to change the SB polling timer from 1.2 ms to 58 μs to reduce the power consumption, but increasing the risk of not being able to detect fast switch changes. The SB polling timer is controlled by the SBPOLL_TIME bit in the Device Configuration register.

As the MC33978 detects a change of status in any of the input channels, the device starts a wake-up timer (416 us ±15%) during which, the source current is increased to 2.0 mA (sustain current). This time is required to charge the node in preparation for a transition from the Delta-V detection mechanism to the 4.0 V detection threshold in Normal mode. At the end of the wake-up timer, the MC33978 returns to the Normal mode to inform the system that a change of state has occurred.

When the device wakes up from the LPM operation, if the change of state was from an open to a closed condition, the current source keeps a 2.0 mA current flowing during 270 μs before it starts forcing the wetting current to the programmed level. This mechanism helps prevent inrush current in the case more than one switch is closed during the wake-up event. See Figure 10 for an example of the switch detection mechanism on an SG channel.

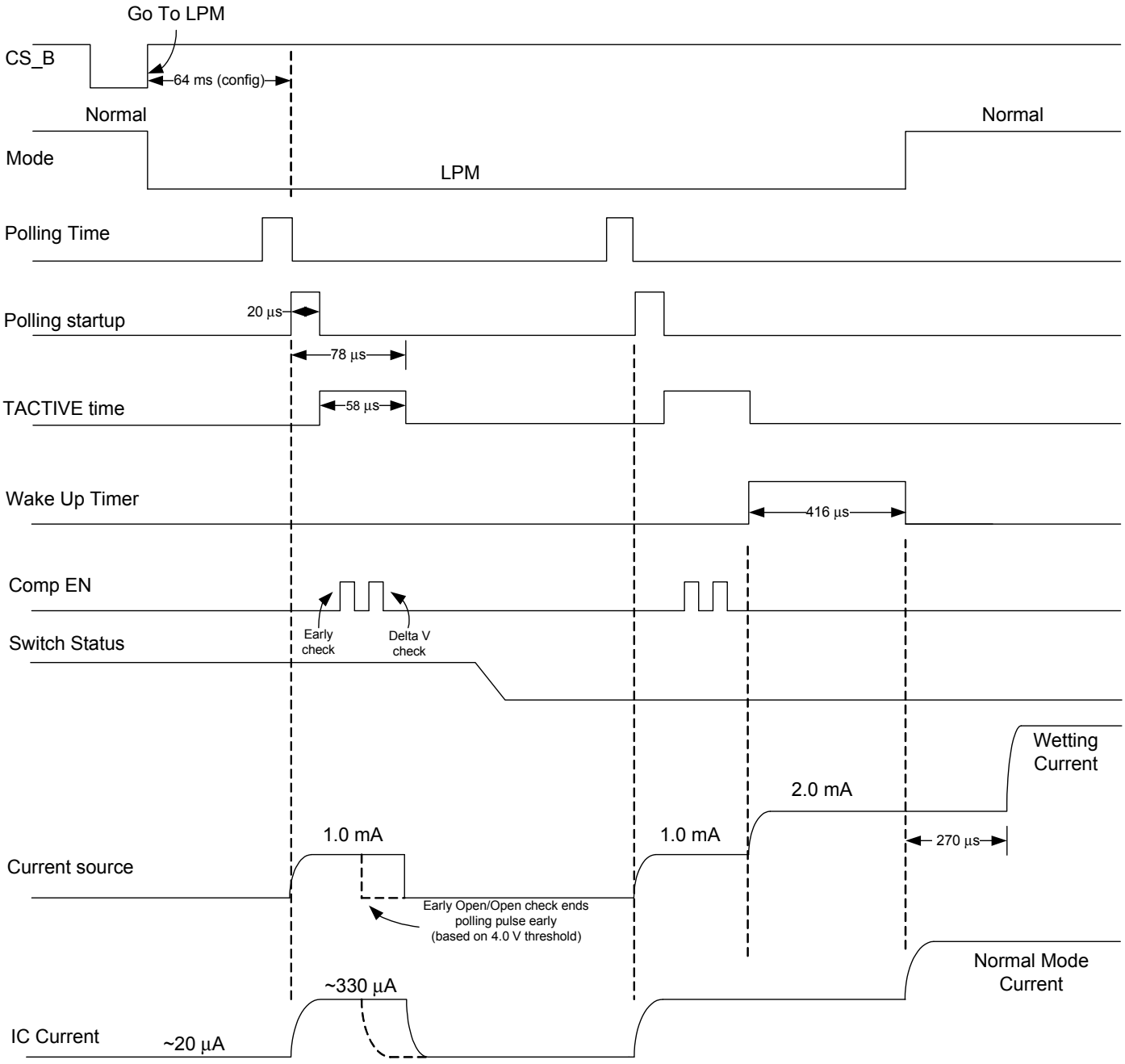

Figure 10. Switch status change detection on an SG channel

5 Conclusion

The MC33978 provides a flexible solution for switch monitoring applications with a high energy efficiency, compared to other solutions. By utilizing the features provided in the Low-power mode operation, the MC33978 is able to fit in a wide variety of applications, allowing designers to do flexible trade-off, such as reduced power consumption, switch detection latency, noise robustness, among others.

The MC33978 provide full featured switch status monitoring in both normal and LPM operation through a single SPI interface, reducing design time and resource utilization by simplifying the software required compared to the implementation of intelligent switch monitoring with standard discrete techniques, which in turn lead to a more compact, robust, and cost effective solution for system with high count of input switches and low-voltage analog signals to be monitored.

6 References

Following are URLs where you can obtain information on related NXP products and application solutions:

Document number and description		URL
MC33978	Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/MC33978.pdf
KIT33978UG	User Guide	http://www.nxp.com/files/analog/doc/user_guide/KT33978UG.pdf
Support Pages		**URL**
MC33978	Product Summary Page	http://www.nxp.com/products/analog-power-management/interface/22-i-o-msdi-programmable-current-analog-mux:MC33978
Power Management Home Page		http://www.nxp.com/PMIC
Analog Home Page		http://www.nxp.com/analog

7 Revision history

Revision	Date	Description
1.0	09/2015	• Initial release
	7/2016	• Updated to NXP document form and style

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