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APPLICATION NOTE

DEMOBOARD FOR BGA2003

- **Description of product**

BGA2003: RF transistor with internal bias circuit. Benefit is lower component count, internal compensation for temperature and diffusion spread.

- **Application Area**

Low noise amplifiers for CDMA, DECT, GSM, PCS with low component count.

- **Presented Application**

The application presents a low noise amplifier for CDMA at 1930-1990 MHz. Supply voltage is 3V and supply current 10 mA. Only output matching is needed.

- **Main results**

An amplifier has been designed and tested with >12.3 dB gain, IP3in=5 dBm, $VSWR_{in,out}$<1:2, and <2 dB Noise Figure at 1930-1990 MHz. 3 Volt, 10 mA supply.

Abstract

Philips' double poly fifth generation technology makes it possible to design high performance MMICs (Microwave Monolithic Integrated Circuits). The advantage of such MMICs is a higher functionality and a lower component count for high frequency applications.

This application note describes a design made with the BGA2003. The BGA2003 is a high frequency transistor with integrated bias and control input.
The application described here is specially intended as CDMA LNA (Low Noise Amplifier) for the 1930-1990 MHz frequency region. The design was intended to show the following performance: Gain > 12dB, NF < 2 dB, IP3in > +2 dBm, $VSWR_{in,out}$ < 1:2, Vsupply = 3V.

The following appendices can be found next:

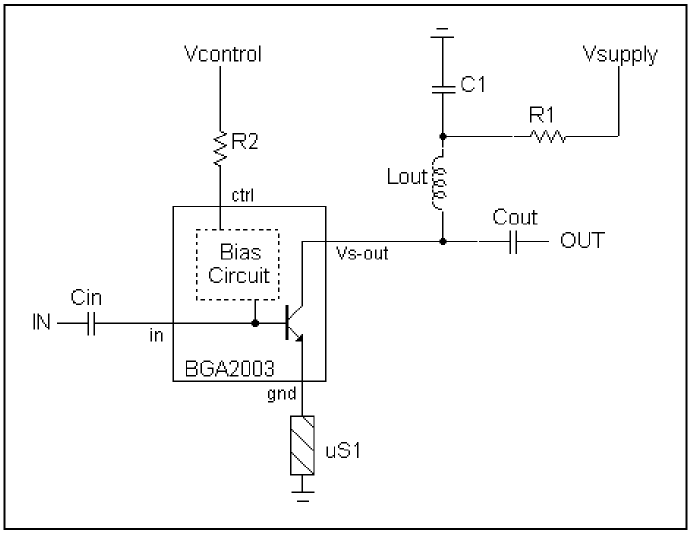
-Circuit diagram and layout drawing

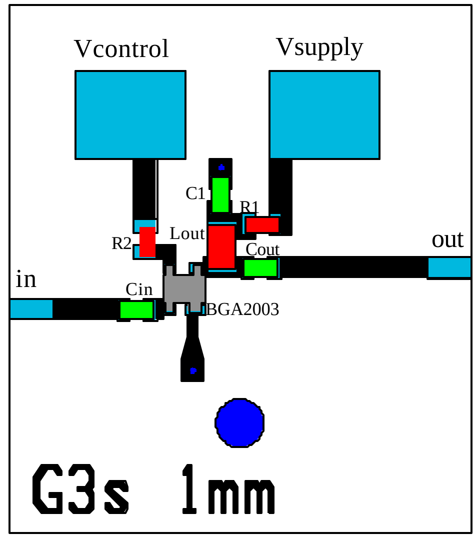
-Component values

-Measured results

-Conclusions and recomendations

Circuit diagram and Layout drawing:

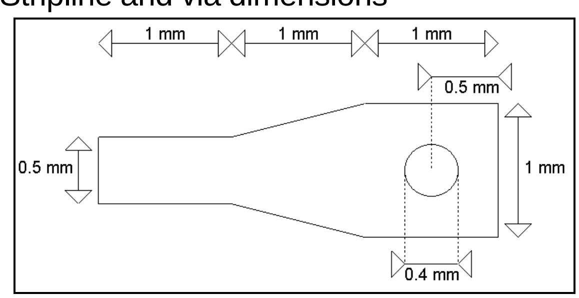




Component Values

Component	Value	Type	Comment
R1	22	0603 Philips	Supply decoupling
R2	2200	0603 Philips	Current setting
C1	8.2pF	0603 Philips	RF-short to ground
Cin	8.2pF	0603 Philips	Input match, DC-decoupling
Lout	3.9nH	0603 TDK MLG1608	Output match
Cout	1.0pF	0603 Philips	Output match
uS1	-	PCB-stripline 50Ω, via	see figure below
MMIC	BGA2003	Philips SOT343R2	
PCB	-	FR4	e_R ~ 4.6, H = 0.5 mm

Stripline and via dimensions



Measured values:

Vsupply = 3V, Vcontrol = 3V, Isupply = 9.4 mA, Icontrol = 0.84 mA

	@ 1930 MHz	@ 1990 MHz	remark:
$VSWR_{in}$	1.85	1.81	
$VSWR_{out}$	1.53	1.85	
S21	12.6 dB	12.2 dB	
S12	-17.5 dB	-17.1 dB	
IP3in	+5	+5.3	Pin=-25 dBm, Δf=1 MHz
NF	2 dB	1.9 dB	

Conclusions and recomendations:

From the measured results it can be found that the desired performance can be delivered. The IP3 is even a lot higher than required. Therefore one could try to lower the current in order to have a less power consuming application. Because the gain would go down and matching components on the input would be necessary to compensate for this, that approach was not used in this design.

When evaluating the demoboard, one might find that the LNA is oscillating when both input and output are open, and when all DC voltages are applied. Under normal operating conditions ($VSWR_{in,out}$< 1:7) there is however no problem.