Overlaying MPC823 Graphics on a Remote Video Source

Application Note

Version 0.6

Date 27/11/98

Rodney Watt

Imaging and Entertainment Solutions

Europe.

Tel : +49 89 92103 138

Email : R26005@email.mot.com

freescale™ semiconductor

Revision History

Revision	Date	Author	Description
0.1	11/09/98	Rodney Watt	Initial Document
0.2	21/09/98	Rodney Watt	State M/C simplified by changing MPC823 Video Control
0.3	23/10/98	Rodney Watt	Information added - Connection to FADS - Signal Descriptions
0.4	06/11/98	Rodney Watt	Added test results from completed circuit
0.5	20/11/98	Rodney Watt	Document title changed Update after testing complete
0.6	27/11/98	Rodney Watt	Bug fix

Table of Contents

Table of Tables

Table of Figures

1. Introduction

1.1. Background

The MPC823 is a very powerful and flexible embedded microprocessor. This part compasses a PowerPC core, a communications processor module and a system integration unit. A video controller forms part of this system integration unit.

The flexibility of the part allows the MPC823 to be used in numerous applications. One such application is in web access equipment. Web browser boxes allow the user to access the web while using his television as the display medium.

Most web access boxes work on the principle that one TV channel will be dedicated to view web pages. This works well but has the limitation that the user needs to change channel when he wants to switch between TV and the web.

Imagine the situation where the user is a football fan and wants to keep up to date with the latest scores. Instead of having to keep switching between channels from watching TV to checking the latest web page, it would be much better if the web page (or at least part of it) appeared at the bottom of the TV screen, overlaid on the normal TV picture.

This applications note details the hardware required to support such a feature.

1.2. Overlaying Video Signals

In order to overlay two video signals, they must be locked in time. This means their synchronisation signals, i.e. Horizontal SYNC and Vertical SYNC must be “in step”. Also, they must be driven from the same clock and also, they must have the correct colour reference lock.

The incoming TV signal contains all the relevant timing, brightness and colour information. Since the analogue TV signal is fixed and can not be altered, it is the digitally generated signal which must be manipulated.

This process is known as “Genlock”. Genlocking simply means that the local sync generator locks on to and synchronises itself with a separate incoming signal.

Normally this is achieved by stripping the timing information from the incoming TV signal and using this to drive the graphics controller on the secondary source.

However, on the MPC823, the VSYNC and HSYNC signals can only be driven by the internal video controller. These signals can not be driven by an external source. The only signal that can be driven into the MPC823's video controller is the pixel clock.

This application note shows how the MPC823 generated graphics can by synchronised with an external video signal by controlling the pixel clock which is feed into the MPC823’s video controller.

1.3. The MPC823's Video Controller

Before examining how the 823's video controller can be overlaid onto a remote TV signal, a basic knowledge of the controller is required.

The MPC823's video controller supports PAL and NTSC displays, (as well as digital TFT LCD panels). The MPC823 provides all the necessary digital signals for the display. An external video encoder is required for the digital to analogue conversion.

The video controller uses a frame buffer, also called a display buffer, which is stored in system memory. The data in the display buffer represents pixel components (bytes), whether it is RGB or YCrCb . The user is responsible for preprocessing data as it is stored in the display buffer. The video controller uses a dedicated DMA channel to read the data from the display buffer and drive it to the video interface. This memory is accessed via the MPC823's System Interface Unit. The display data is loaded into the video controller's FIFO's using direct memory access, (DMA), transactions.

The video controller also generates the required timing and control signals (horizontal sync, vertical sync, field, and blanking).

The diagram below shows a basic system using the MPC823's video controller.

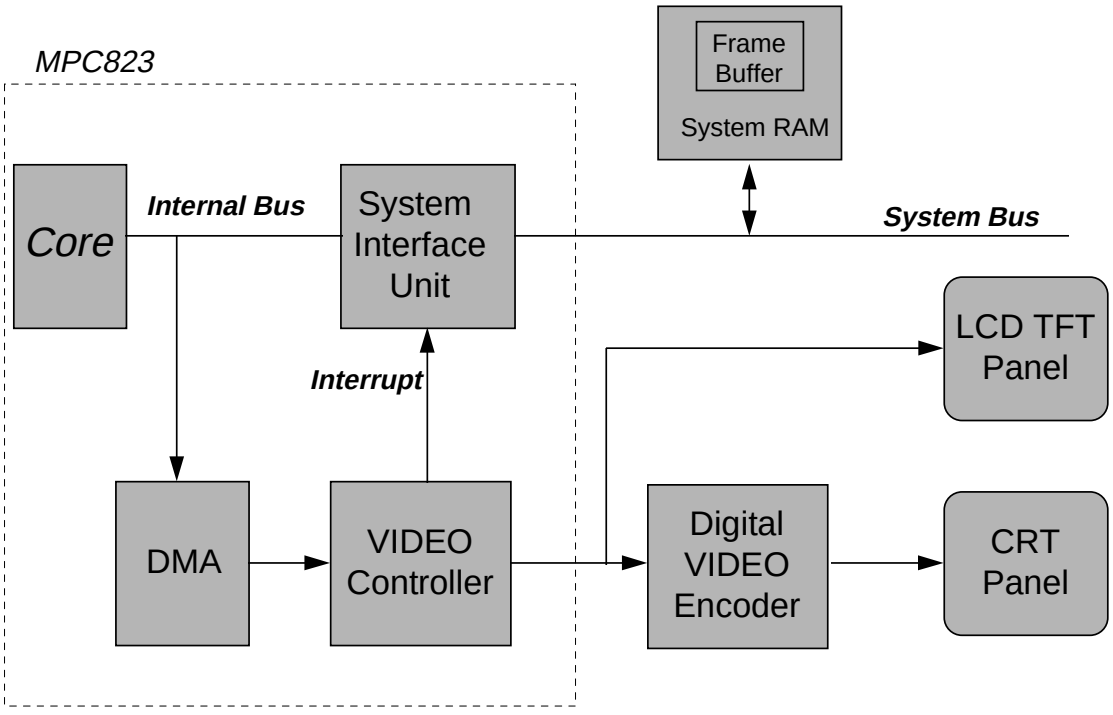


Figure 1 Video System using the MPC823's Video Controller

The video controller consists of a register set, DMA controller with FIFOs, and a video control RAM array, as shown below. The video controller RAM array provides the proper sequencing and control signal generation needed to synchronise the data stream through the FIFOs. The video controller, a standalone module, is programmed using a set of configuration registers. Once the registers have been configured and the video controller is enabled, the DMA controller initiates burst read cycles to display memory.

The video controller connects gluelessly to most video encoders. The basic connection being via a eight bit data bus, (CCIR-656 Compatible), and associated control signals. The control signals, (Horizontal Sync, Vertical Sync, Field and Blanking), are software programmable. Their state being programmed using a “Video Control RAM” area inside the MPC823.

The video controller master clock source can either be generated internally by the system interface unit, or it can be driven into the MPC823’s video controller by an external source.

In simple video applications, the pixel clock will be generated internally by the MPC823’s clock circuitry. However, in more complex systems where it is required to synchronise the video controller with another video source, the pixel clock should be provided externally.

The diagram below shows the internals of the video controller.

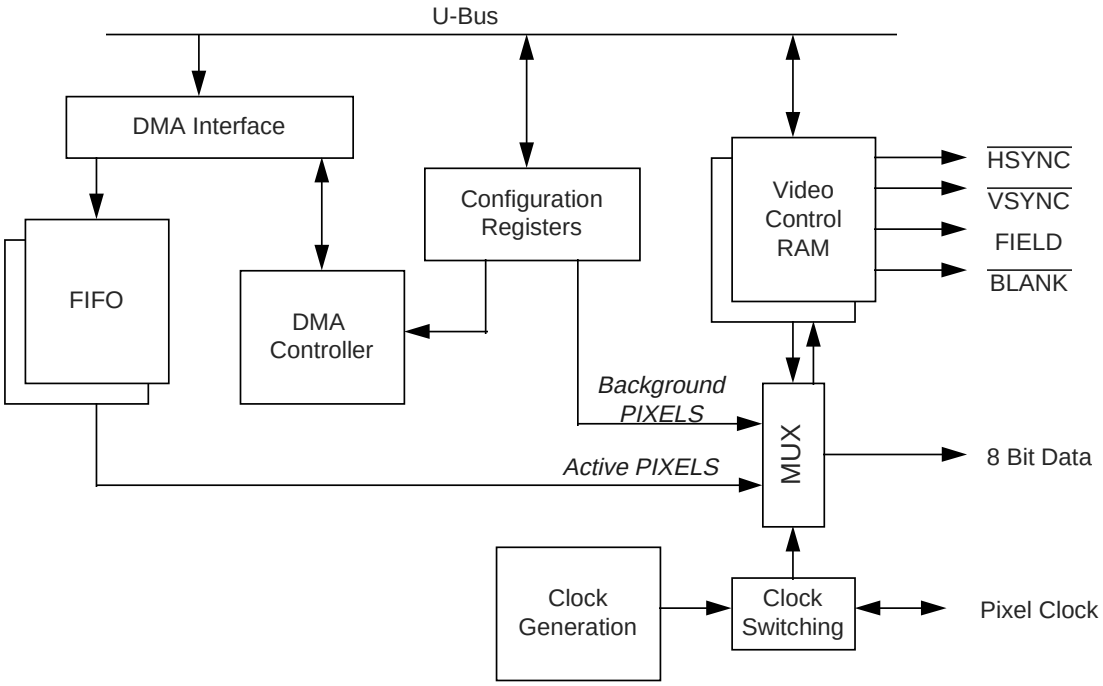


Figure 2 Video Controller Block Diagram

2. Circuit Description

The circuit diagram below shows how graphic overlay may be achieved.

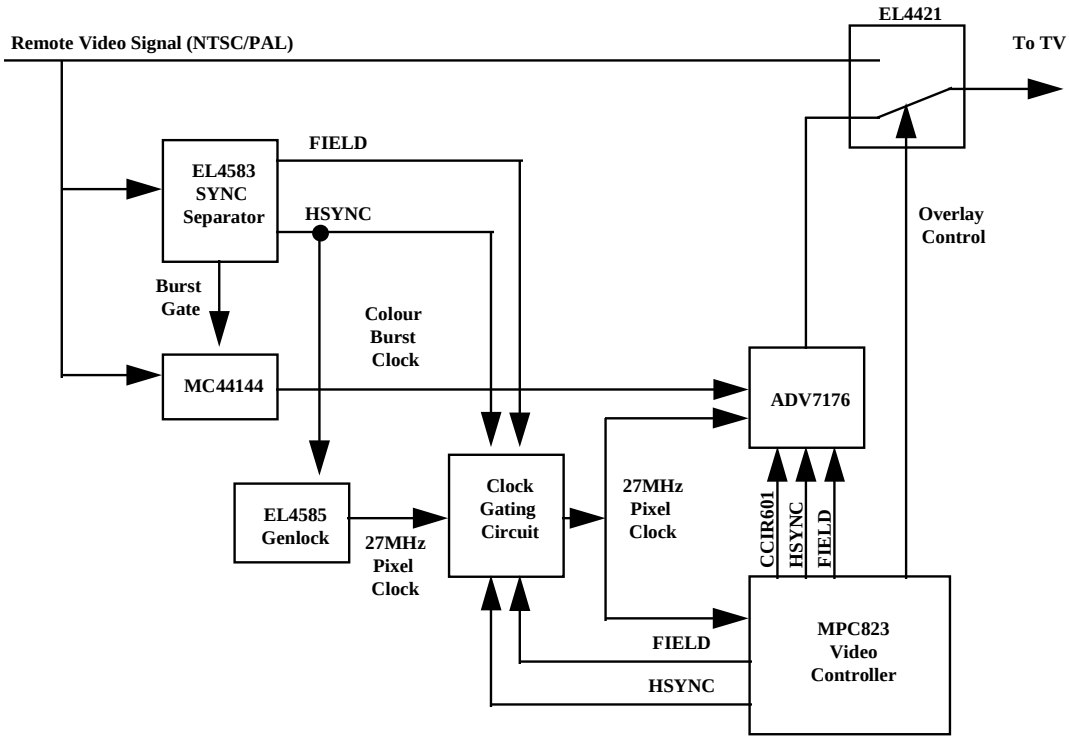


Figure 3 System Block Diagram

2.1. SYNC Separation

Firstly the timing synchronisation pulses, FIELD and HSYNC, must be extracted from the incoming video signal. This is achieved by the EL4583 Sync Separator. As well as the HSYNC and VSYNC timing information, the EL4583 also produces a “Burst Gate” signal which is required to synchronise the colours.

2.2. Synchronising Colour Information

Colour information within the video signal is all contained in a single frequency, 3.58MHz for NTSC and 4.43MHz for PAL. The colour is defined by the phase difference between the colour signal at any point on the line of video an a “colour burst” reference at the beginning of each line. To ensure that any overlaid video appears the correct colour, it must be generated with respect to the correct reference. The video encoder must be supplied with this colour reference. The MC44144 is a PLL chip that produces a continuous colour burst reference. It is supplied with the TV analogue video and a “Burst Gate” pulse from the EL4583. The loop locks when the original burst reference is present and coast for the rest of the time.

2.3. Pixel Clock Generation

The timing for all the digital parts of the system must also be locked to the incoming analogue video. The system clock, usually 27MHz must be locked to the HSYNC to ensure exactly the same number of pixels on each line. This locked pixel clock is produced using the EL4585 which takes the analogue HSYNC and produces a locked 27MHz clock. It is generated by multiplying the horizontal line frequency by the number of pixel clocks per scan line by using a phase lock loop. This clock is used to drive the MPC823 video controller and the video encoder.

2.4. Video Encoder

In this example, an Analogue Devices Video Encoder is used, ADV7176. This is the video encoder used on the MPC823FADS board. The timing information, (pixel clock, HSYNC and FIELD), is all extracted from the remote video signal. It is only the data information that is provided by the MPC823's video controller.

2.5. Video Muxing

The video overlay is achieved by switching between the incoming video source, (Remote Source), and the MPC823 source, (Local Source). An EL4421 multiplexed-input video amplifier is used to switch between the two video sources. This switching is controlled by the "Overlay Enable" signal which is driven by the MPC823's video controller.

2.6. MPC823 Video Controller

The MPC823 video controller is driven by the pixel clock which is extracted from the remote video source. The video controller provides the data to the video encoder. The MPC823's video timing signals, (e.g. VSYNC, HSYNC, BLANK, FIELD), are not used to drive the video encoder. The timing information for the video encoder is provided by the remote video source. Some of these timing signals are however used by the clock gating circuit to synchronise the MPC823's video date with the remote video data.

2.7. Clock Gating Circuit

Usually four signals are used to control a video source. These are detailed in the table below.

Signal	Description	Use
VSYNC	Vertical Synchronisation Pulse	Asserted at the start and the middle of the frame
HSYNC	Horizontal Synchronous Pulse	Asserted at the start of each line
FIELD	Odd/even field indicator	Indicates odd/even field in interlaced system
BLANK	Video Banking Signal	To blank the display

Table 1 Video Control Signals

Both video sources, (i.e. the incoming video picture and the 823 generated graphics) will be controlled using these signals. As the incoming video picture is fixed and can not be altered, the MPC823's video information will be modified to keep both video sources in sync.

The MPC823's video controller is configured in such a way that the locally generated data will always be "ahead" of the remote video. The MPC823' s video controller will then "wait" till the remote video "catches up".

2.7.1. State Machine

The state machine for the clock gating circuit is shown below.

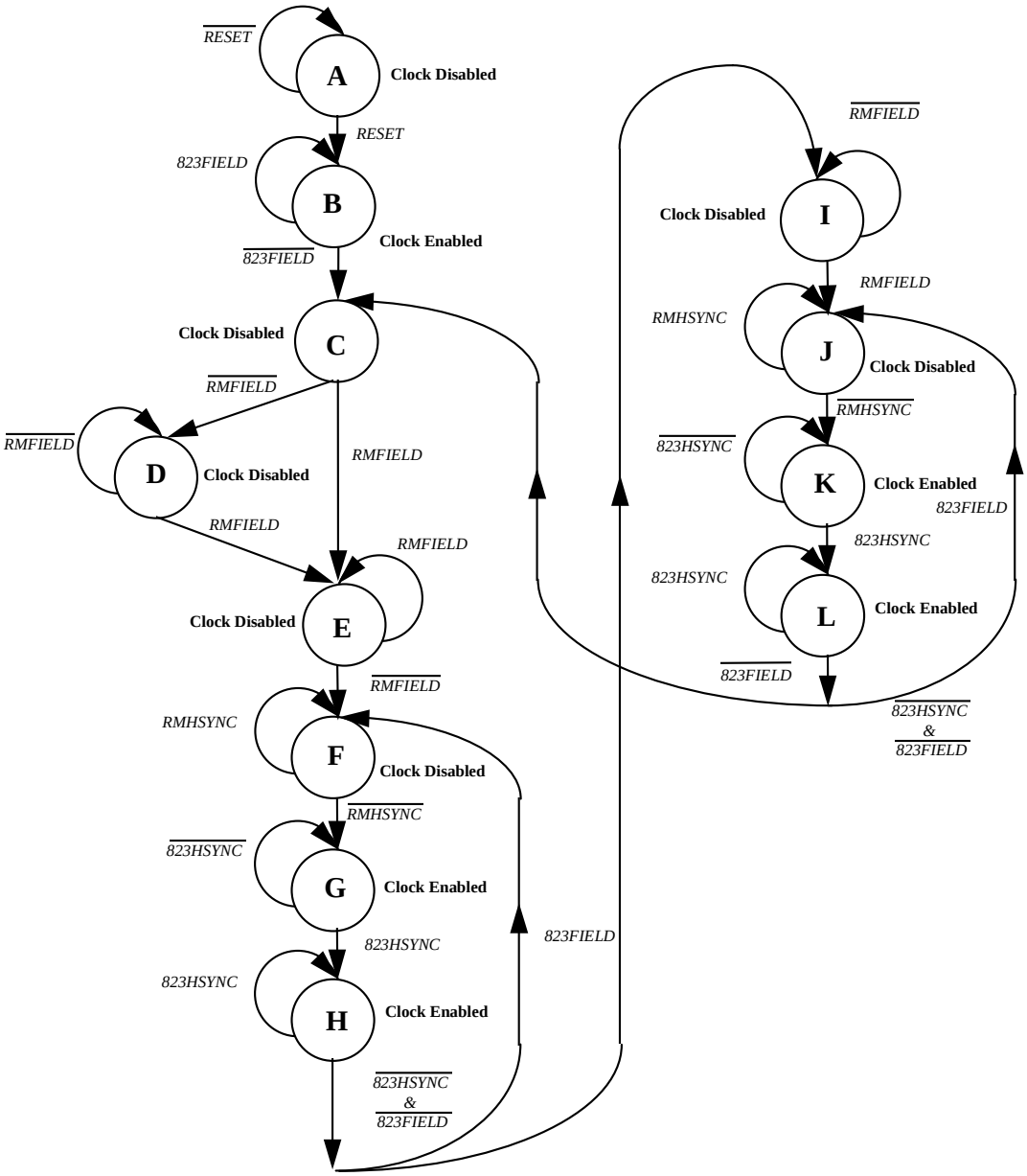


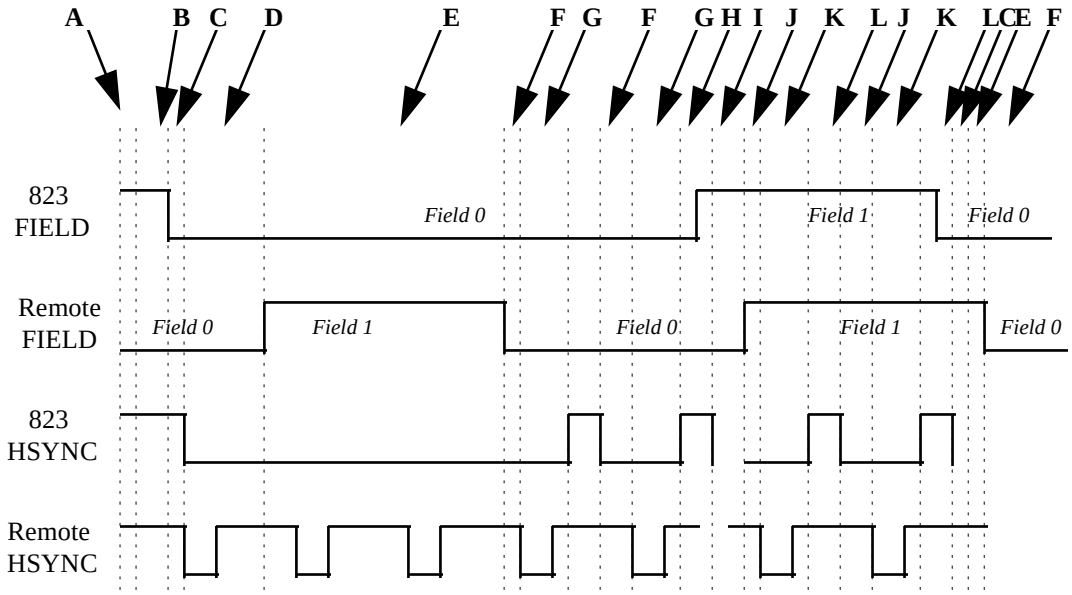
Figure 4 State Machine

2.7.2. Timing Diagrams

The operation of the clock gating circuit can be better seen from the timing diagram below.

State	Meaning	Clock Status
A	Circuit in reset	Disabled
B	Waiting for MPC823 Field 0	Enabled
C	Check for value of Remote Video Field	Disabled
D	Waiting for Remote Video Field 1	Disabled
E	Waiting for Remote Video Field 0	Disabled
F	Waiting for Remote HSYNC	Disabled
G	Waiting for MPC823 HSYNC to go high	Enabled
H	Check for MPC823 HSYNC or MPC823 Field 1	Enabled
I	Waiting for Remote Video Field 1	Disabled
J	Waiting for Remote HSYNC	Disabled
K	Waiting for MPC823 HSYNC to go high	Enabled
L	Check for MPC823 HSYNC or MPC823 Field 0	Enabled

Table 2 Remote Video and 823 in Sync.



Note : The diagram above is not to scale.

2.7.3. State Machine Logic Equations

```
Name            statemc;
Partno          XXXXXX;
Date            10/11/98;
Revision        0.1;
Designer        Rod Watt;
Company         Freescale;
Assembly        App Note;
Location        Ux;
Device          p22v10;

/*****************************************************************/
/* Clock Gating State Machine                                    */
/*                                                               */
/* This state machine is used to gate the pixel clock which goes */
/* to the MPC823's video controller.                             */
/* The state machine monitors the timing signals of the Remote   */
/* Video and the MPC823's video. The pixel clock is turned on and */
/* off which halts the MPC823's video data. This is used to keep */
/* both video sources in sync.                                   */
/*****************************************************************/


/**  Inputs  **/

Pin 1           = clock;              /* System Clock              */
Pin 2           = RMFIELD;            /* Remote Video's FIELD      */
Pin 3           = 823FIELD;           /* 823's FIELD Signal        */
Pin 4           = RMHSYNC;            /* Remote HSYNC Signal       */
Pin 5           = 823HSYNC;           /* 823's HSYNC Signal        */
Pin 8           = Reset;              /* System Reset              */
Pin 9           = pixelclk;           /* Pixel Clock               */


/**  Outputs  **/

Pin 14          = clkout;             /* O/P clock for 823         */
Pin [15..18]  = [state3..0];          /* State Machine             */

/** Declarations and Intermediate Variable Definitions **/

field state     =[state3..0];         /*State Machine Field        */

$define         false   'b'0
$define         true    'b'1

$define         State_A         'b'0000
$define         State_B         'b'0001
$define         State_C         'b'0010
$define         State_D         'b'0011
$define         State_E         'b'0100
$define         State_F         'b'0101
$define         State_G         'b'0110
$define         State_H         'b'0111
$define         State_I         'b'1000
$define         State_J         'b'1001
$define         State_K         'b'1010
$define         State_L         'b'1011


/**  Logic Equations  **/

       state.ar       =       !Reset;
```

```
/* State Sequence */

        SEQUENCE state {
                PRESENT State_A
                IF Reset NEXT State_B;
                DEFAULT NEXT State_A;

                PRESENT State_B
                IF !823FIELD NEXT State_C;
                DEFAULT NEXT State_B;

                PRESENT State_C
                IF !RMFIELD NEXT State_D;
                IF RMFIELD NEXT State_E;

                PRESENT State_D
                IF RMFIELD NEXT State_E;
                DEFAULT NEXT State_D;

                PRESENT State_E
                IF !RMFIELD NEXT State_F;
                DEFAULT NEXT State_E;

                PRESENT State_F
                IF  !RMHSYNC NEXT State_G;
                DEFAULT NEXT State_F;

                PRESENT State_G
                IF 823HSYNC NEXT State_H;
                DEFAULT NEXT State_G;

                PRESENT State_H
                IF (!823HSYNC & !823FIELD) NEXT State_F;
                IF 823FIELD NEXT State_I;
                DEFAULT NEXT State_H;

                PRESENT State_I
                IF RMFIELD NEXT State_J;
                DEFAULT NEXT State_I;

                PRESENT State_J
                IF !RMHSYNC NEXT State_K;
                DEFAULT NEXT State_J;

                PRESENT State_K
                IF 823HSYNC NEXT State_L;
                DEFAULT NEXT State_K;

                PRESENT State_L
                IF (!823HSYNC & 823FIELD) NEXT State_J;
                IF !823FIELD NEXT State_C;
                DEFAULT NEXT State_L;


                }

/** Outputs for State Machine **/

        clkout =  pixelclk & state:[0] & false
                #  pixelclk & state:[1] & true
                #  pixelclk & state:[2] & false
                #  pixelclk & state:[3] & false
                #  pixelclk & state:[4] & false
                #  pixelclk & state:[5] & false
                #  pixelclk & state:[6] & true
                #  pixelclk & state:[7] & true
                #  pixelclk & state:[8] & false
                #  pixelclk & state:[9] & false
                #  pixelclk & state:[A] & true
                #  pixelclk & state:[B] & true;
```

2.8. MPC823 Video Controller

The MPC823's video controller is extremely flexible. The operation of the video controller is determined by programming the configuration registers and the video RAM.

2.8.1. Configuration Registers

The configuration registers determine how the video controller is initialised.

Register Name	Description	Used For
VCCR	Video Controller Configuration Register	Configure Video Controller - data timing, data polarity, - byte order, address type, clock
VSR[1]	Video Status Register	Report Events to the core - BERR, underrun, EOF
VCMR	Video Command Register	Control Display Format - Select active set, blank display
VBCB	Video Background Colour Buffer Register	Background Video - i.e. inactive part of the screen
VFCR0	Video Frame Configuration Register (SET 0)	Configure SET 0 - No. of lines for a field
VFAA0	Video Frame Buffer A Start Address Register (SET 0)	Start address of SET 0 odd field
VFBA0	Video Frame Buffer B Start Address Register (SET 0)	Start address of SET 0 even field
VFCR1[2]	Video Frame Configuration Register (SET 1)	Configure SET 1 - No. of lines for a field
VFAA1[2]	Video Frame Buffer A Start Address Register (SET 1)	Start address of SET 1 odd field
VFBA1[2]	Video Frame Buffer B Start Address Register (SET 1)	Start address of SET 1 even field

Table 3 MPC823's Video Configuration Registers

Note : [1] This is a status register, it does not need to be initialised by the user.
[2] Only Set 0 is used, these registers which control Set 1 are left in the default state

The table below details how these registers should be configured in this application

Register Name	Setting	Meaning
VCCR	0x2042	Drive data on clock rising edge Data is active high Background video is set for YCrCb format End of Frame Interrupt is disabled Underrun/bus error interrupt is disabled Interrupt request level is set to 0 (Not applicable) Byte Order is set to Big or little Endian Address type is set to 0 The external clock is set as the clock source The video controller is turned on
VCMR	0x00	RAM Set 0 and FIFO Set 0 is selected Image from the frame buffer is displayed
VBCB	0x80108010	The background colour is set to black (YCrCb format)
VFCR0	0x0780505A	Frame B is valid (Video is interlaced) Vertical pixel count is 240 lines The gap between lines is set to 90 Number of burst per line is 90
VFAA0	0xXXXXXX	This register points to the external memory and hence is specific to the hardware. For instance, on the MPC823FADS board, this register could be set to 0x00300000
VFBA0	0xXXXXXX	This register points to the external memory and hence is specific to the hardware. For instance, on the MPC823FADS board, this register could be set to 0x003005a0

Table 4 MPC823's Video Configuration Registers Initialisation

2.8.2. Video RAM

The operation of the MPC823's video control signals are determined by the video controller RAM array. The video RAM consist of two RAM arrays, RAM_0 and RAM_1, that contain 64 32-bit entries. At any given time, one RAM array actively drives the panel and controls video controller operation, while the other is inactive but modifiable.

The video RAM array block diagram is shown below.

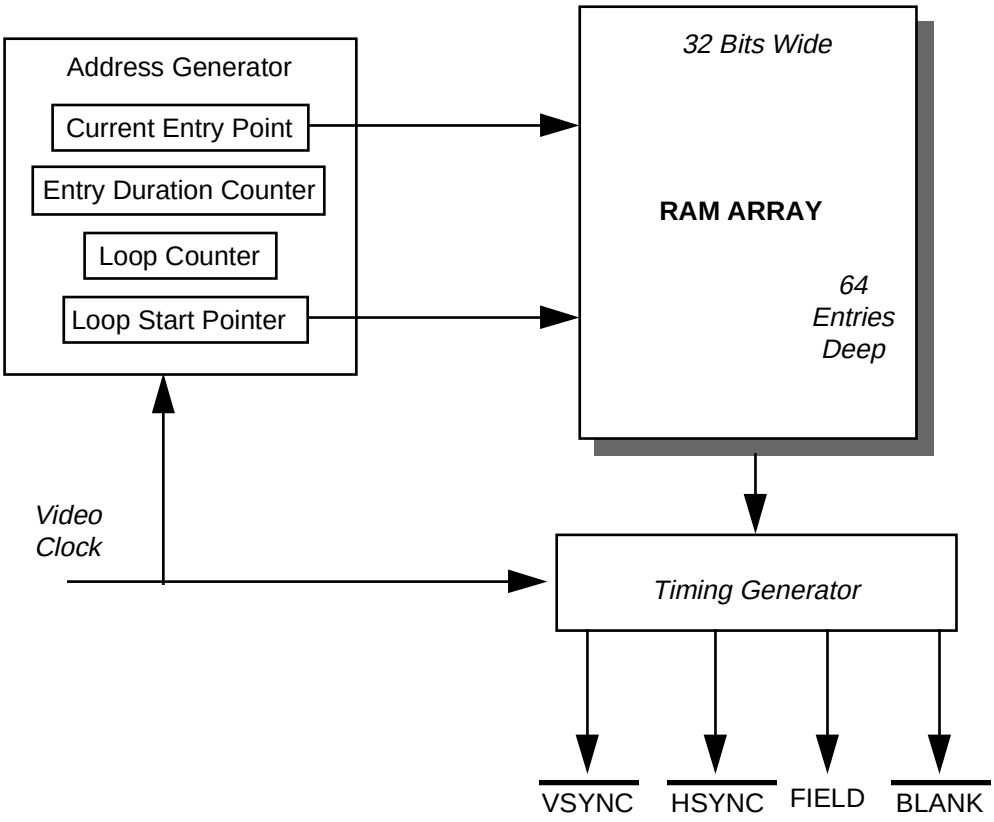


Figure 5 Video RAM Array Block Diagram

Details of the video RAM word are given in the MPC823 data book.

2.8.2.1. Programming.

The 823's video control signal are used for two purposes in this design.

- They provide synchronisation information to the clock gating circuit
- They provide the "Overlay Enable" signal to the video mixer. The 823's FIELD signal provides the "Overlay Enable" signal.

Note : On the MPC823FADS board, the MPC823's VSYNC signal provides the FIELD timing information to the video encoder. Therefore, the VSYNC must be programmed as a FIELD signal.

Ram Entry	RAM Word Field									Line Description
	Hx [1]	Vx [2]	Fx [2]	Bx	VDS	INT	LCYC	LP	LST	
0	00	00	11	00	01	0	200	1	0	Lines 0 - 200
1	00	00	11	00	01	0	235	0	0	Odd Field active area
2	11	00	11	11	01	0	8	0	0	Remote Video Selected
3	11	00	11	11	00	0	1440	0	0	Horizontal line repeated
4	11	00	11	00	01	0	31 [4]	1	0	200 times
5	00	00	11	00	01	0	40	1	0	Lines 201 - 240
6	00	00	11	00	01	0	235	0	0	Odd Field active area
7	11	00	11	11	01	0	8	0	0	MPC823 Video Selected
8	11	00	00	11	00	0	1440	0	0	Horizontal line repeated
9	11	00	11	00	01	0	31 [4]	1	0	40 times
10	00	11	11	00	01	0	200	1	0	Lines 241 - 440
11	00	11	11	00	01	0	235	0	0	Odd Field active area
12	11	11	11	11	01	0	8	0	0	Remote Video Selected
13	11	11	11	11	00	0	1440	0	0	Horizontal line repeated
14	11	11	11	00	01	0	31 [4]	1	0	200 times
15	00	11	11	00	01	0	40	1	0	Lines 441 - 480
16	00	11	11	00	01	0	235	0	0	Odd Field active area
17	11	11	11	11	01	0	8	0	0	MPC823 Video Selected
18	11	11	00	11	00	0	1440	0	0	Horizontal line repeated
19	11	11	11	00	01	0	31 [4]	1	0	40 times

Table 5 NTSC Programming Example

Note : [1] The timing of the HSYNC signal is different to that given in the MPC823UM. The duration of the HSYNC pulse has been increased.

Note : [2] The Vx signals are used to control the video encoders FIELD values

Note : [3] When Fx = 11, the remote video source is selected
When Fx = 00, the MPC823's video date is selected

Note : [3] The 823 video is only sent to the TV during its "active data time".

Note : [4] The line length is reduced by one clock to ensure the 823 is "always in front" of the remote video.

3. Hardware

3.1. Circuit Schematics

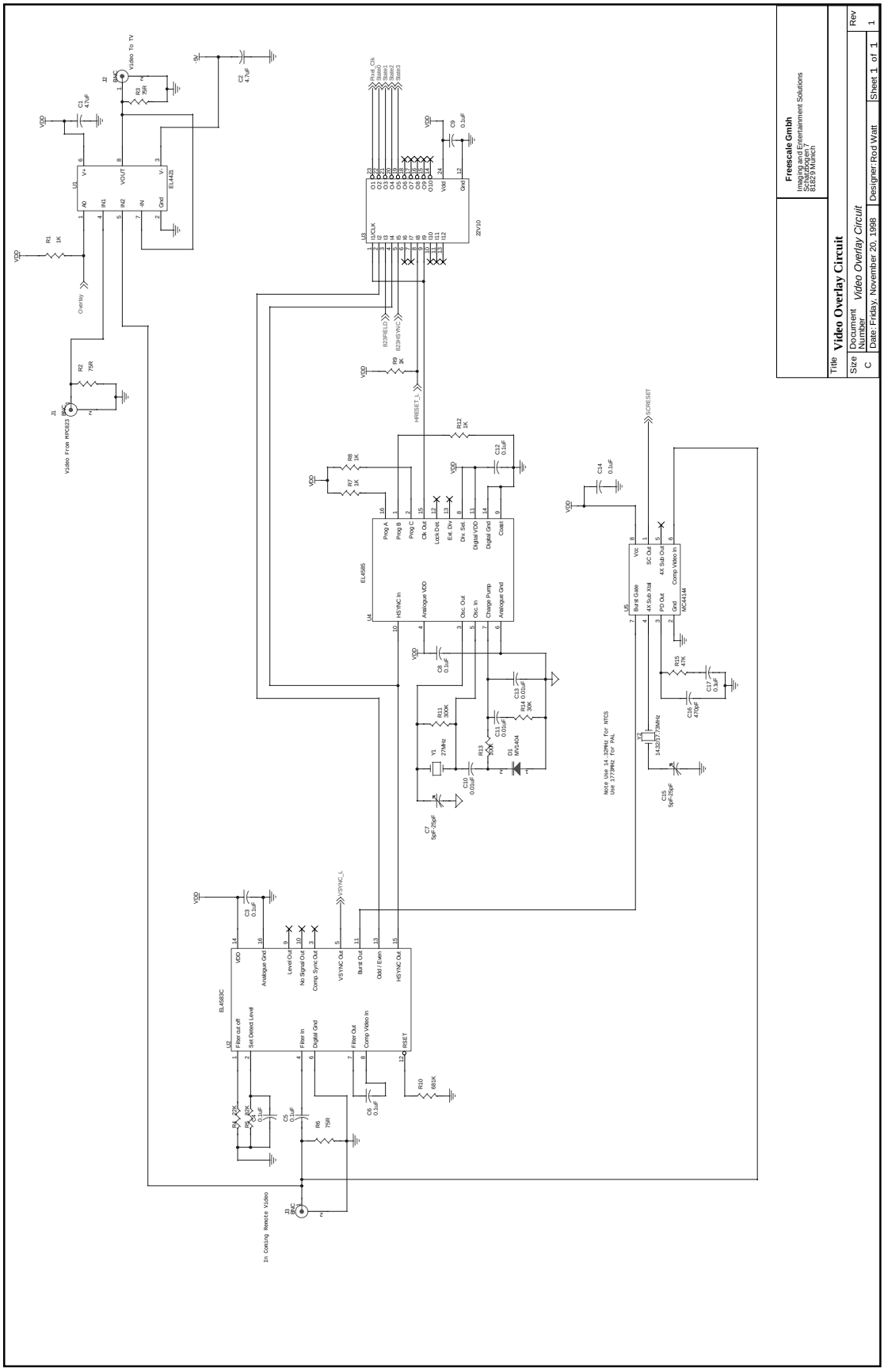
The following page shows the circuit schematics. The table below details the signals used.

Signal	Input/Output	Description
Remote Video	Input	Incoming remote TV signal
823 Video	Input	823 generated graphics
Overlay	Input	Switches between remote and 823 video signals. Generated by the MPC823's video controller
823FIELD	Input	FIELD signal from MPC823's video controller
823HSYNC	Input	HSYNC signal from MPC823's video controller
TV Video	Output	Mixed video signal to TV
SCRESET	Output	Colour phase signal to ADV7176 video encoder
Pixel Clock	Output	Pixel Clock to MPC823's video controller and ADV7176 video encoder
State[0:3]	Output	State machine bits reflecting current state
HRESET	Input	Hard Reset signal from MPC823

Table 6 Input/Output Signals

Note : The Input/Output is stated with respect to the video overlay circuit.

Overlaying MPC823 Graphics on an Analogue TV Picture



3.2. Parts List

Reference Designator	Description	No. Off.
C1,C2	4.7uF Capacitor	2
C3,C4,C5,C6,C8,C9,C12, C14,C17	0.1uF Capacitor	9
C7, C15	5pF-30pF Variable Capacitor	1
C10,C11, C13	0.01uF Capacitor	3
C16	470pF Capacitor	1
D1	Freescale MV1404 Varactor	1
J1,J2,J3	BNC Connector	3
R2,R3,R6	75R Resistor	3
R4	22K Resistor	1
R5	82K Resistor	1
R1,R7,R8,R9, R12	1K Resistor	5
R10	681K Resistor	1
R11	300K Resistor	1
R13	100K Resistor	1
R14	30K Resistor	1
R15	47K Resistor	1
U1	Elantec EL4421 Muxed I/P Video Amplifier	1
U2	Elantec EL4583C Sync. Separator	1
U3	PAL22V10 PAL	1
U4	Elantec EL4585 Horizontal Genlock	1
U5	Freescale MC44144 Subcarrier Phase Lock Loop	1
Y1	27MHz Crystal	1
Y2[1]	14.32/17.73MHz Crystal	1

Table 7 Parts List

Note : [1] Use 14.32 MHz for NTSC
Use 17.73 MHz for PAL

4. Test

The following section describes how the video overlay board may be tested. This involves connecting the board up to the MPC823FADS board and also a description of the signals that should be seen.

4.1. Connection to the FADS

In order to evaluate this circuit, it can be connected to an MPC823FADS board. The diagram below shows how the circuit should be connected up in a system.

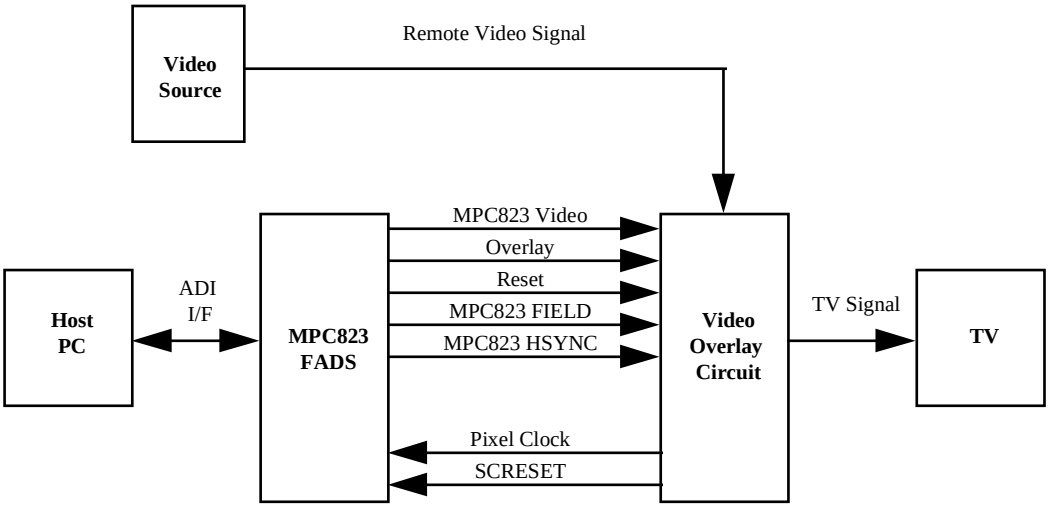


Figure 6 Graphics Overlay System

The MPC823FADS system is used to generate the MPC823 graphics. The FADS system is connected to a host PC via the ADI (Application Development Interface) cable. The PC is running a single line debugger, MPC8Bug. This provides a means for downloading the MPC823's graphics onto the FADS board.

A video source, such as a VCR, provides the remote video information. This is feed to the video overlay circuit via a simple phono socket.

The video overlay circuit takes in the video from the FADS board and from the remote video source. Apart from synchronising the two video sources, it is responsible for mixing the video information which is sent to the TV.

The following table details how the video overlay circuitry should be connected to the MPC823FADS board.

Signal	I/O (wrt FADS)	Description	Connection	Notes
MPC823 Video	O/P	Video from MPC823	P11 on MPC823FADSDB	_
Overlay	O/P	Overlay enable signal to video mux	P7, Pin 13 on MPC823FADSDB	MPC823's FIELD signal provides overlay information
Reset	O/P	Reset	P8, Pin C22 on MPC8xxFADS	MPC823's HRESET Signal
MPC823 FIELD	O/P	VSYNC from MPC823	P7, Pin 9 on MPC823FADSDB	MPC823's VSYNC provides the FIELD information
MPC823 HSYNC	O/P	HSYNC from MPC823	P7, Pin 7 on MPC823FADSDB	_
Pixel Clock	I/P	Video clock to MPC823 video controller	P7, Pin 1 on MPC823FADSDB	The on board video clock must be disabled by writing a '0' to bit VDOEXCKEN in the BCSR4 Register on the FADS
SCRESET	I/P	Subcarrier reset for ADV7176	U10, Pin 35	Pin must be disconnected from PCB

Table 8 Connection to the FADS Board

4.2. Test Results

The diagram below shows the main signals of concern in the design. These signals will be discussed in turn.

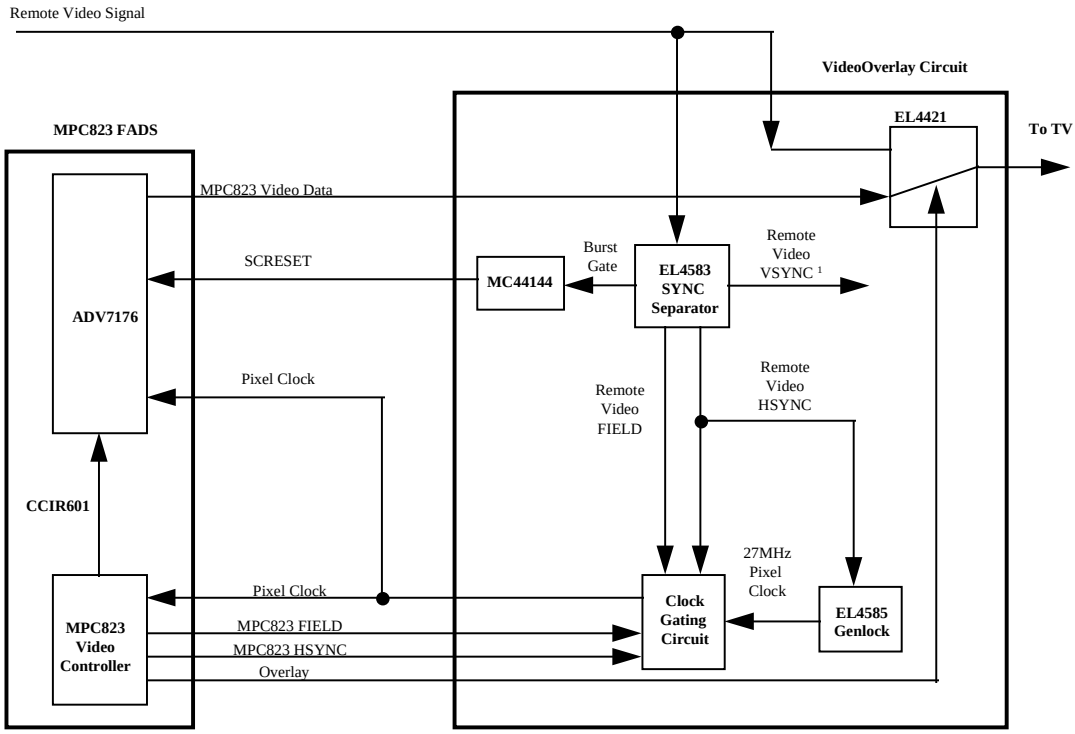


Figure 7 Main Signals

Note : [1] The remote video's VSYNC signal is not used in the circuit. It is shown for the sake of completeness.

4.2.1. Remote TV Signal

The remote TV signal is transmitted as composite video. This means that the single signal contains colour video and timing information. The signal is made up of various "components"; i.e. active video, horizontal sync, horizontal blanking, vertical sync, vertical blanking and colour burst.

4.2.2. Burst Gate

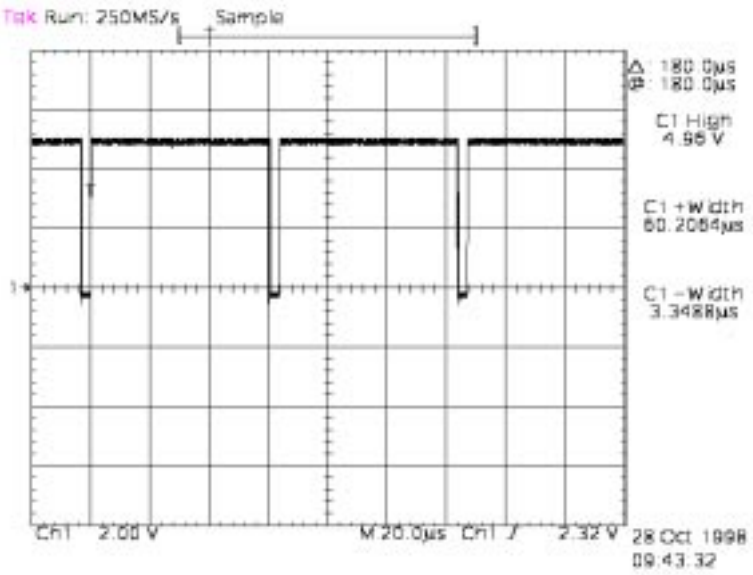


Figure 8 Burst Gate Signal

The Elantec EL4585 produces a “Burst Gate” pulse which is feed to the Freescale MC44144 PLL. This pulse is triggered by the trailing edge of the HSYNC pulse. Its duration being produced by an internal timer.

4.2.3. SCReset

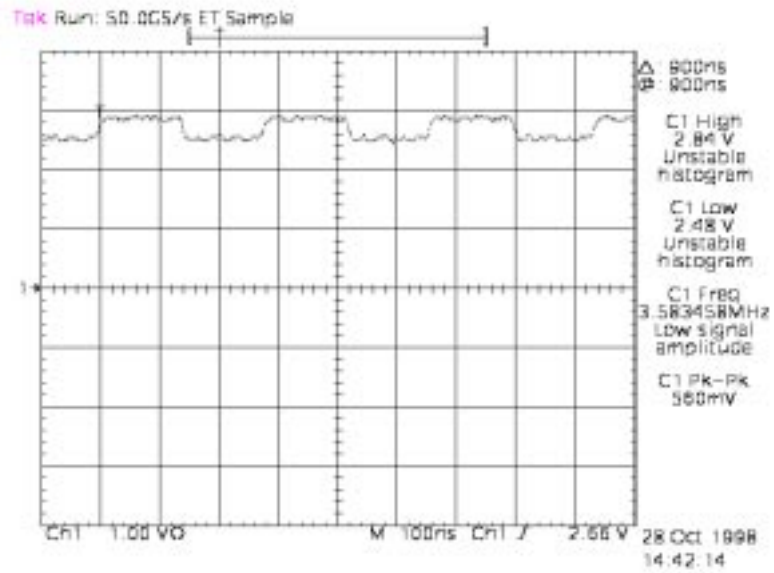


Figure 9 SCReset

The SCReset signal is feed to the video encoder, (ADV7176), to restore the colour information.

For NTSC, the colour information is carried on a 3.58MHz signal.

4.2.4. Remote Video FIELD

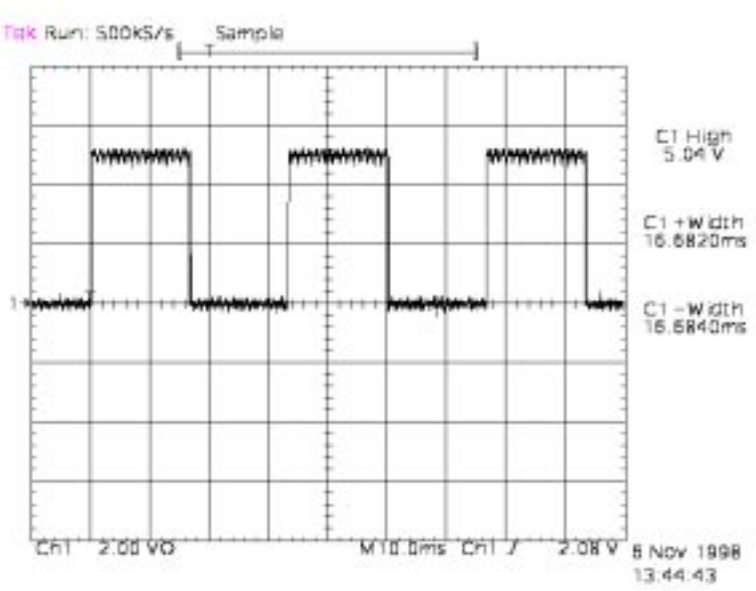


Figure 10 Remote Video FIELD

The FIELD signal indicates if the Odd or Even lines are being driven on an Interlaced picture.

When FIELD = 0, the Even lines are being shown

When FIELD = 1, the Odd lines are being shown

FIELD is asserted (either high or low) for 16.68 mS.

The time between subsequent HSYNC pulses = 58.8828 + 4.6722 = 63.555uS
(see next page)

Therefore each FIELD signal "covers" $(16.68 \times 10^{-3}) / (63.555 \times 10^{-6}) = 262.5$ lines

Each complete NTSC picture is made up of two fields. i.e. an Odd field and an Even field.

This results in a total picture of (2 x 262.5) = 525 lines

4.2.5. Remote Video HSYNC

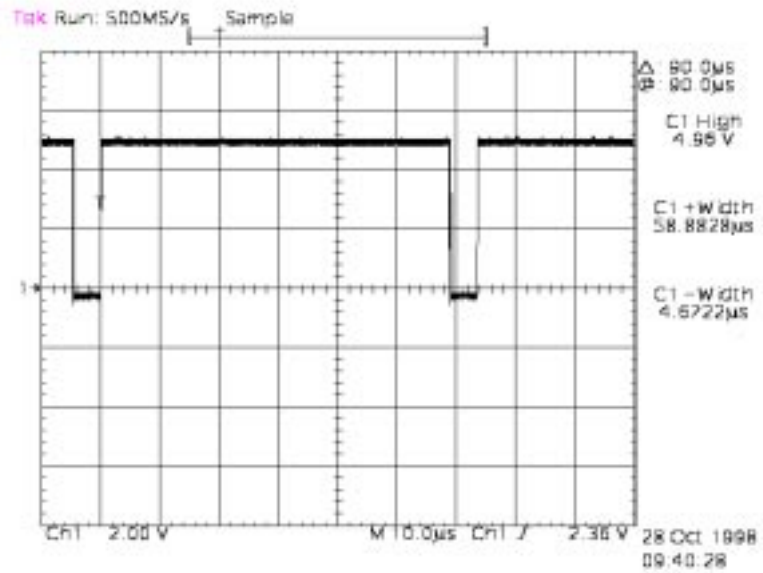


Figure 11 Remote Video HSYNC

The start of each line is marked by the assertion of HSYNC.

Time between subsequent HSYNC pulses = 58.8828 + 4.6722 = 63.555uS

1 pixel clock = $1/(27 \times 10^{6})$ S

Therefore, each line = $63.555 \times 10^{-6} / (1/(27 \times 10^{6})) = 1716$ clock cycles

4.2.6. Pixel Clock

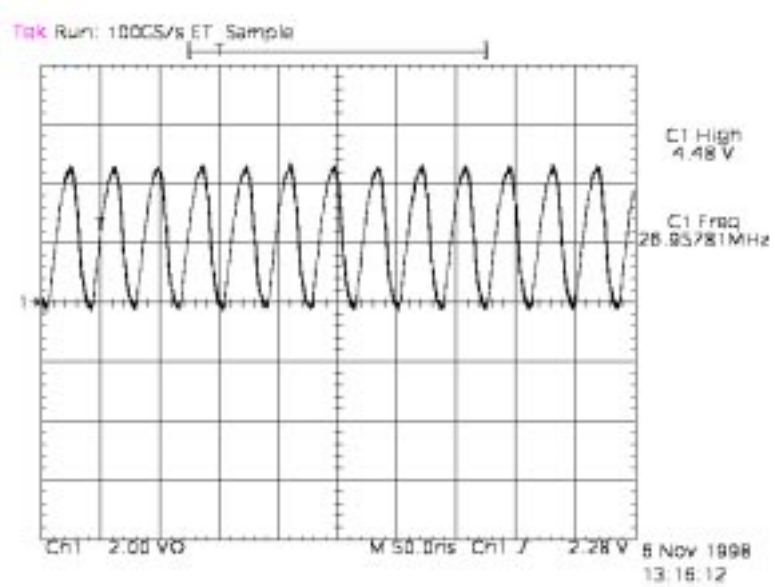


Figure 12 Pixel Clock

The diagram above shows the pixel clock that has been generated from the incoming video source. The clock information is actually generated by dividing the time between subsequent HSYNC pulses. The clock is nominally 27MHz but its exact frequency can be altered by three programmable bits on the EL4585C Horizontal Genlock chip.

A	B	C	Div. Value	Freq. (MHz)	Used For
0	0	0	1702	26.602	PAL - 6Fsc
0	0	1	1728	27.0	PAL - CCIR 601
0	1	0	1888	29.5	PAL - Square
0	1	1	2270	35.468	PAL - 8Fsc
1	0	0	1364	21.476	NTSC - 6Fsc
1	0	1	1716	27.0	NTSC - CCIR 601
1	1	0	1560	24.546	NTSC - Square
1	1	1	1820	28.636	NTSC - 8Fsc

Table 9 Pixel Clock Frequencies

Note : In this example used, a divisor factor of 1716 was used. i.e. each line is made up of 1716 pixel clocks.

Refer to the EL4585C Horizontal Genlock specification for additional information.

4.2.7. Remote Video VSYNC

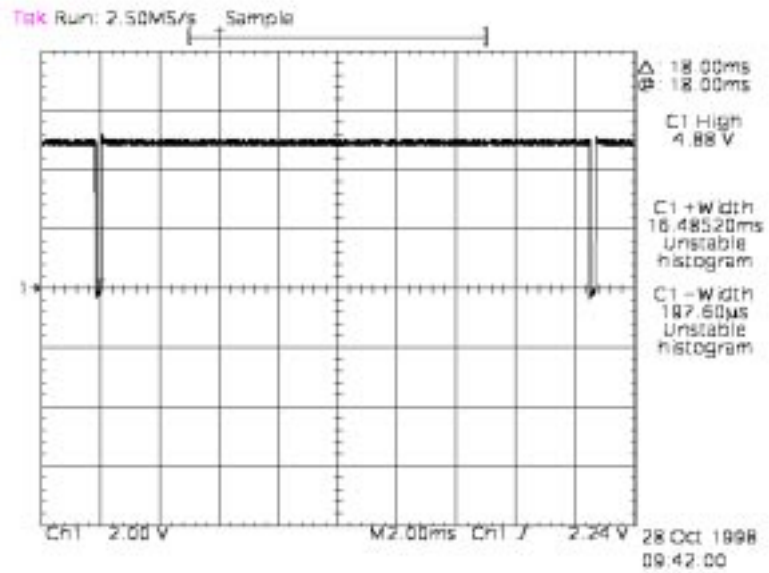


Figure 13 Remote Video VSYNC

Although the remote video's VSYNC signal is not used in the design, it is shown here for completeness.

Time between subsequent VSYNC pulses = 16.48520 mS + 197.60 uS = 16.6828 mS

Each pixel clock = $1/(27 \times 10^6)$ S

Therefore, number of pixel clocks between subsequent VSYNC pulses is

$$16.6828 \times 10^{-3} / (1/(27 \times 10^6)) = 450436 \text{ clocks}$$

Each line contains 1716 clocks

Therefore, number of lines between subsequent VSYNC pulses is

$$450436 / 1716 = 262.5 \text{ lines}$$

i.e. A VSYNC pulse is asserted at the start of each field

4.2.8. MPC823 FIELD

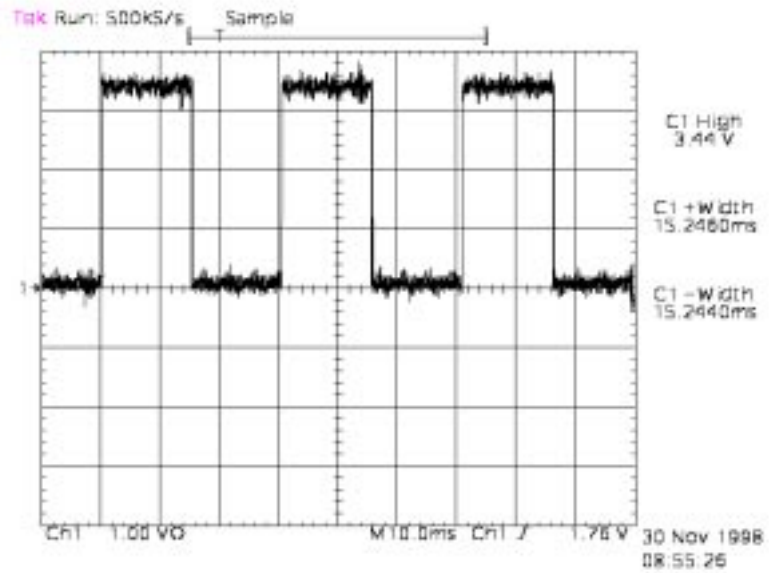


Figure 14 MPC823 Field

The FIELD signal indicates if the Odd or Even lines are being driven on an Interlaced picture.

When FIELD = 0, the Even lines are being shown

When FIELD = 1, the Odd lines are being shown

The value of the FIELD is programmable in the MPC823's VRAM.

Here, each field is 15.24mS.

The time between subsequent HSYNC pulses = 54.7776 + 8.74 = 63.5176uS
(see next page)

Therefore each FIELD signal "covers" $(15.24 \times 10^{-3}) / (63.5176 \times 10^{-6}) = 240$ lines

Each complete NTSC picture is made up of two fields. i.e. an Odd field and an Even field.

This results in a total picture of (2 x 240) = 480 lines

This is because the 823 video data is only driven during the active data area.

4.2.9. MPC823 HSYNC_L

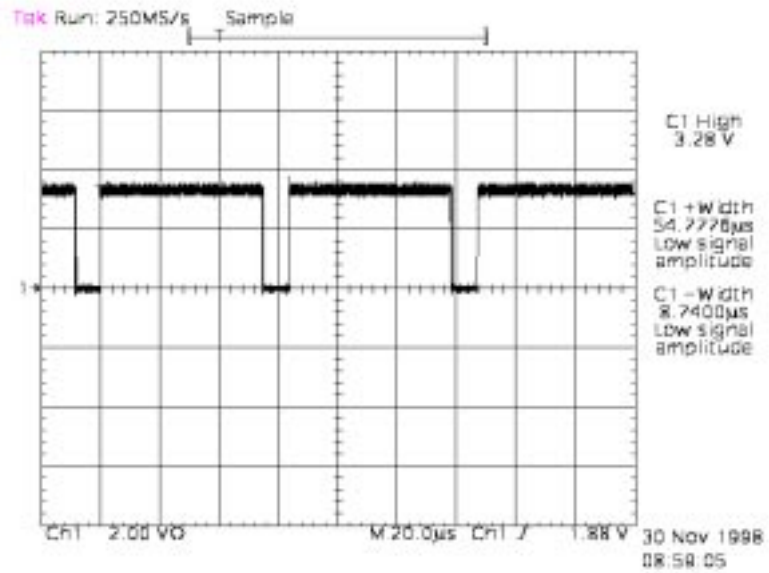


Figure 15 MPC823 HSYNC_L

The MPC823's HSYNC pulse indicates that the 823 is starting a new line of graphics. Again, this signal may be controlled by programming the video controllers VRAM.

Time between subsequent HSYNC pulses = 54.7776 + 8.74 = 63.5176uS

1 pixel clock = $1/(27 \times 10^{6})$ S

Therefore, each line = $63.5176 \times 10^{-6} / (1/(27 \times 10^{6})) = 1715$ clock cycles

"Normal" NTSC is 1716 clocks long. Here, the MPC823's video is reduced by 1 clock to ensure it is always ahead of the remote video.

4.2.10. Overlay

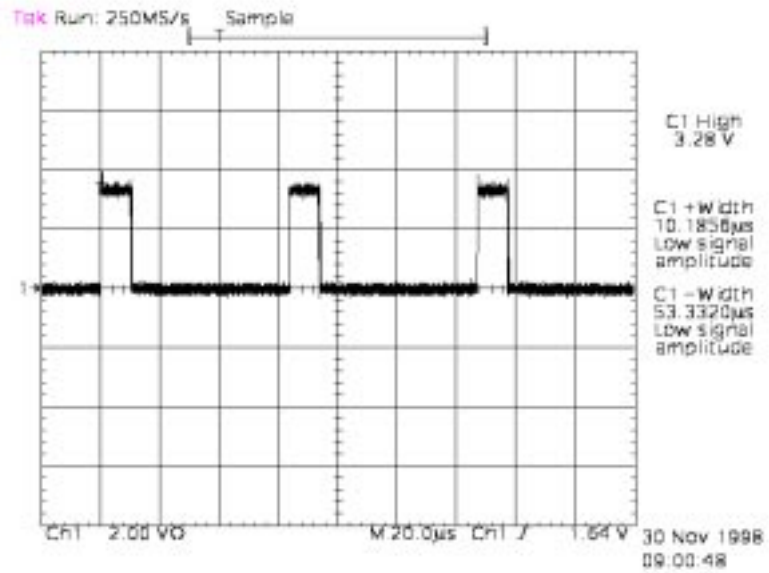


Figure 16 Overlay

The MPC823's FIELD signal is used to generate the overlay signal. This signal is used to switch between the two incoming video signals, (i.e. remote and MPC823), on the video multiplexer.

When overlay = 0, the video from the MPC823 is selected. When overlay = 1, the remote video source is selected.

In the example shown above, the signal "low" time is 53.332uS.

1 pixel clock = $1/(27 \times 10^{6})$ S

Therefore, the overlay signal is low for $(53.332 \times 10^{-6}) / (1/(27 \times 10^{6})) = 1440$ clocks.

The signal "high" time is 10.1856uS

i.e. Therefore, the overlay signal is high for $(10.1856 \times 10^{-6}) / (1/(27 \times 10^{6})) = 275$ clocks.

i.e. For each line of MPC823 data which lasts 1715 clocks, only the "active data" which is shown for 1440 clocks is shown on the TV screen.

5. Acronyms and Abbreviations

ADI	Application Development Interface
BDM	Background Debug Mode
CD	Clock Disabled
CRT	Cathode Ray Tube
DMA	Direct memory Access
FADS	MPC823 Family Application Development System
FIFO	First In First Out
HSYNC	Horizontal Synchronising Pulse signal
LCD	Liquid Crystal Display
MOF	Middle of Frame
MPC8Bug	MPC823 BDM Interface Software
NTSC	National Television Standards Committee
PAL	Phase Alternation Line
PCB	Printed Circuit Board
RAM	Random Access Memory
RGB	Red Green Blue
RM	Remote Video Source
SOF	Start of Frame
TFT	Thin Film Technology
VCR	Video Cassette Recorder
VSYNC	Vertical Synchronising Pulse signal
YCrCb	Luminance/Colour Difference Specification (ITU-R BT601)

6. References

PowerPC™ MPC823 Users Manual - MPC823UM/D
MPC823FADS Users Manual
MC44144 Data Sheet - MC44144/D
Analog Devices ADV7175/ADV7176 Data Sheet
Elantec EL4583C Data Sheet
Elantec EL4585 Data Sheet
Elantec EL4421 Data Sheet