An internal RISC-based packet-processing engine supports multiple networking protocols to guarantee reliable data transport over packet networks while significantly offloading such processing from the DSP cores. The MSC8144 embeds the industry's largest internal memory and supports a variety of advanced interface types, including high-speed Ethernet and UTOPIA for network communications, DDR controller for high-speed, industry-standard memory interface, multi-channel TDM interfaces for connectivity to the PSTN networks and Serial RapidIO and PCI interfaces for connectivity to other devices mounted on the same rack or circuit board. The highly flexible, fully programmable MSC8144 multimedia DSP offers tremendous processing power while maintaining a competitive price and power per channel. Figure 3 shows a block diagram of the MSC8144.

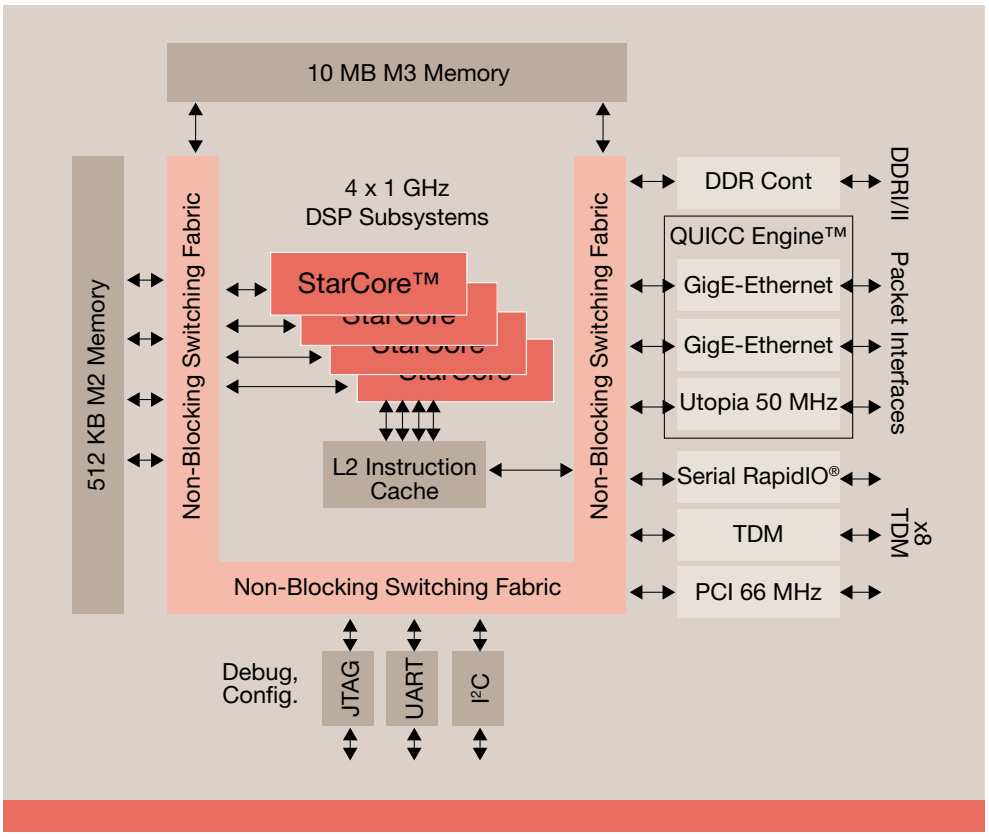
Application Development System (ADS)

Freescale will provide an ADS board as a reference platform and programming development environment for the MSC8144 DSP. The ADS combines a single MSC8144 DSP optionally controlled from a PowerQUICC III MPC8560 communications processor via PCI bus or Gigabit Ethernet switch.

A PT3MC expansion connector provides flexible connectivity options for TDM, UTOPIA, Ethernet and PCI. The ADS is a triple-AMC form factor and can operate as part of an AdvancedTCA® system or stand alone.

From the MSC8144 perspective, all the key I/O interconnects and external memory (if required) are provided. Flexible Ethernet connectivity is provided as well, including SGMII (SERDES) via the main AMC connector or RGMII via RJ45. RMII/SMII is also available via the expansion connector. The Serial RapidIO port is also connected via the main AMC connector and multiple TDM options are available, including E1/T1 Framer, DS3 Framer or expansion connector.

Figure 3: MSC8144 Block Diagram



Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Design Alliance Program, which includes third-party protocol and signaling stack suppliers, real-time operating systems support and a variety of applications software support. All of this builds upon the existing support for previous generations of the StarCore DSP family.

Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set and cycle accurate simulators and debugger for the SC3400 DSP core based on StarCore technology.

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

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Application Summary

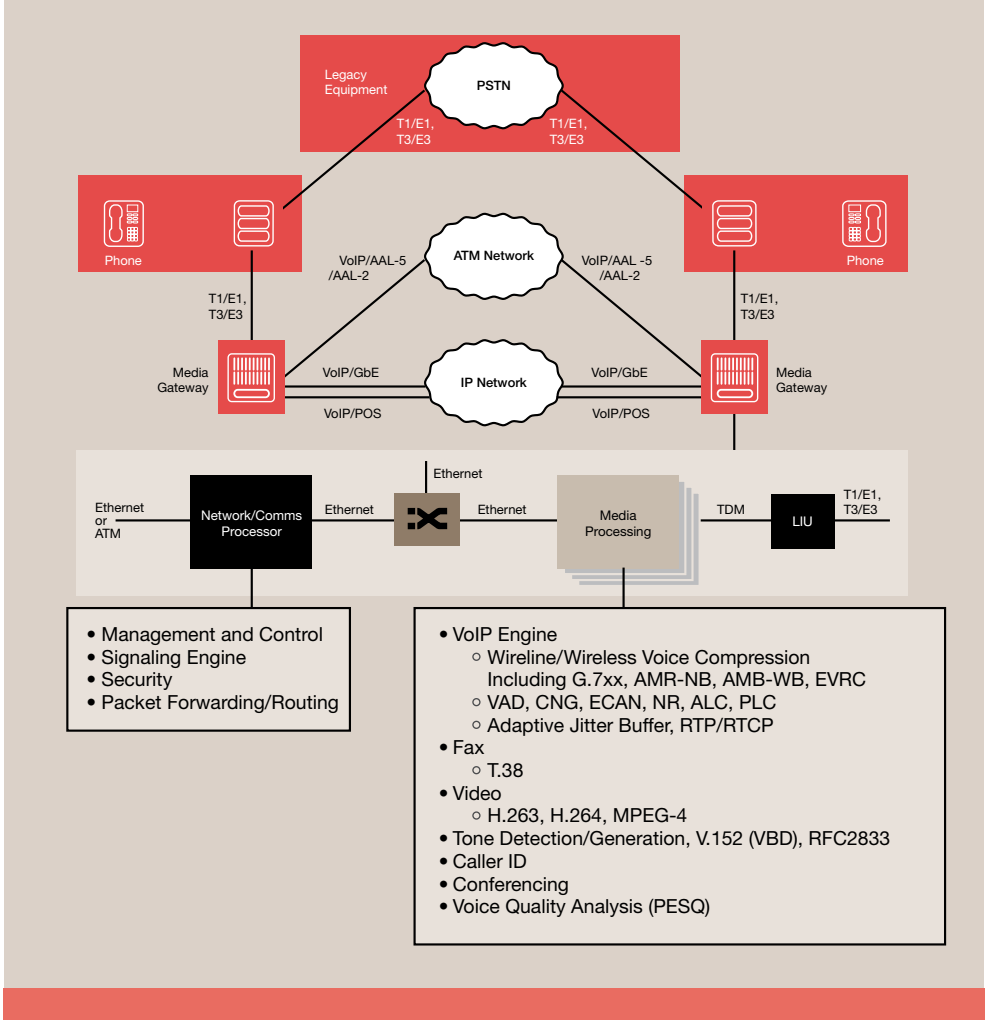
Media Gateway Solution Based on Freescale's High-Performance Processors

The recent increase of data traffic on the network is driving major changes in communications; part of this growth has been brought about by the convergence of voice and video traffic onto public networks. These changes have prompted Internet Protocol (IP)-based networking to evolve at a rapid pace—answering the demand to deliver voice- and video-over-IP (V2IP) and beginning to deliver on the promise of multimedia services over a unified all-IP network, such as an IP multimedia subsystem (IMS)—blurring the boundaries between fixed and wireless telephony networks.

The goal of every telecoms operator is to offer the "triple play" of voice, video and data streaming on a single IP packet network, thus generating new sources of revenue. Adding mobile telephony makes a "quad play" that brings fixed-mobile convergence into the mix. IP, and specifically IMS, are expected to be universal in deployment in the near future and are key enablers of these services and revenue opportunities.

The reality for today and the foreseeable future is that media gateways, media servers and switches supporting the interworking of V2IP on legacy circuit-switched time-division mutiplexing (TDM) and ATM networks, will continue to be the technological forces that drive the delivery of multimedia services. See Figure 1.

Figure 1: Example of a Typical Media Gateway Environment



Under IMS, fixed access (cable, DSL, LAN), mobile access (W-CDMA, CDMA2000, GSM, GPRS) and wireless access (WLAN, WiMAX) are all supported; other phone systems, such as POTS, H.323 and non-IMS VoIP, are only supported through media gateways.

The result is that gateways and servers will still be present even in an all-IMS world. While the protocol and interconnect may change, many of the challenges of interoperability remain the same.

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Design Challenges

Until "IMS everywhere" becomes a reality, equipment has to operate not only between circuit- and packet-switched networks, but between fixed and wireless networks while maintaining compatibility with many standards and protocols. Even in IMS networks, the various standards and protocols used in the multiple access domains mean that transcoding functions are still required.

The media gateway is a classic example of the requirement to interoperate between different networks and standards due to the wide variety of technologies that make up existing networks. These include the circuit-switched PSTN, ATM, frame relay-based public data networks and IP packet networks—all of which may be carried over the same synchronous optical network (SONET).

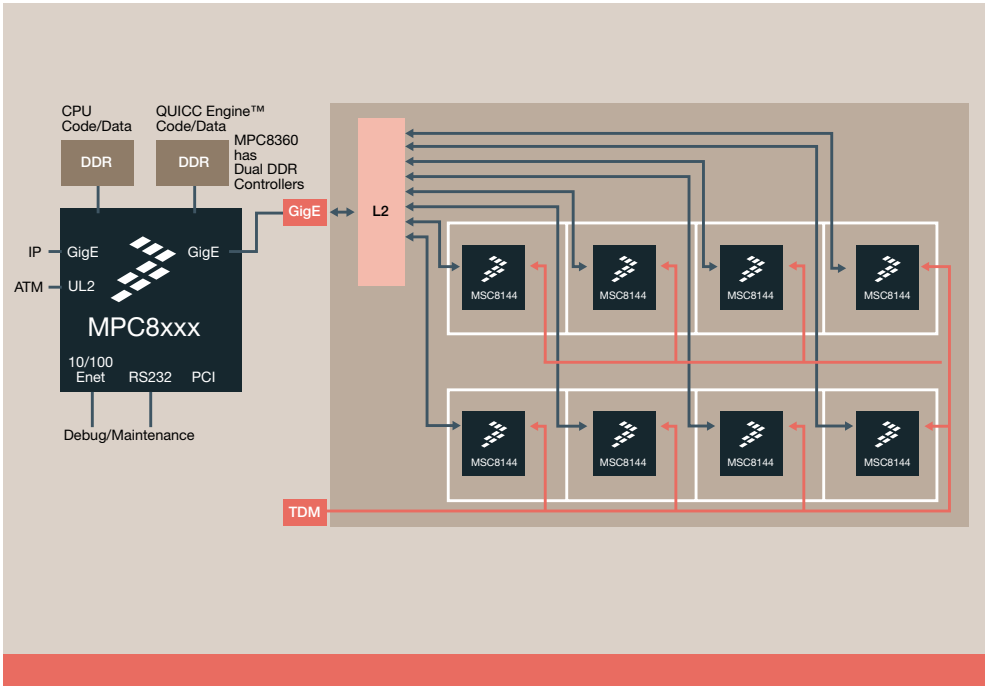
Functions required of media gateways typically include the conversion and compression TDM voice circuits onto ATM networks using a variety of adaptation protocols (AAL0, AAL1, AAL2 and AAL5) or onto packet-based networks using IP (including RTP) frame relay or extensions of both. Voice switches that support the switching of voice circuits among the various network interfaces may require interworking between different protocols.

Specific design challenges for media gateways include:

- Accommodating increasing numbers of voice, video or data (fax/modem) channels per slot within a specific networking device
- Supporting the increasing number of different network interfaces and speeds required, ranging from channelized T1/E1 lines through OC-12 SONET and Gigabit Ethernet interfaces
- Adapting to the number of different protocols used (ATM, AAL2/AAL5, IP/RTP, packet-over-SONET/PPP, MPLS) even as the protocol standards evolve and improve
- Providing the flexibility to add new features and functions through software as future market demands dictate
- Achieving all of this with lower power consumption and a smaller board footprint

One of the biggest challenges facing manufacturers today is minimizing time to market while maintaining and building key product differentiation. Overcoming these challenges requires a careful selection of components to produce a competitive solution that meets the demands of service providers. Not only is the hardware choice important, manufacturers must also consider the ecosystem surrounding the products that enable them to take their system to market quickly with minimal effort. This includes the supporting software, the tool chain and the available reference designs. An example of Freescale's hardware solution is shown in Figure 2.

Figure 2: Example of Freescale's Hardware Solution

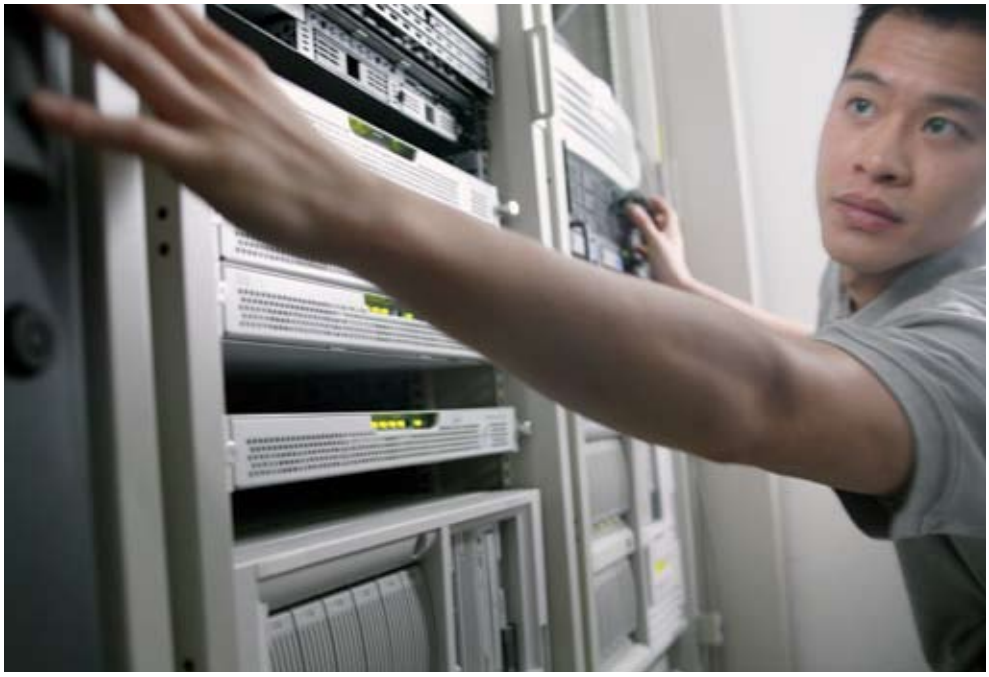


Application Example

Taking a high-level view, a media gateway system operates on traditional TDM voice data, converting it to and from the desired packet format. The format depends on the network protocol and could be either IP or ATM based. With IP, the voice packet is formatted into a specific VoIP protocol (such as RTP), possibly tagged as part of a MPLS session and forwarded to an IP-based network (over Ethernet or SONET), where Quality of Service (QoS) may be guaranteed through the use of various protocols, including DiffServ. ATM is suitable for carrying voice because of its native QoS features. Options for ATM processing in media gateways might include VoIP AAL5, where voice packets from the DSPs are formatted into a specific VoIP protocol (such as RTP), which are then converted into AAL5 PDUs and segmented into ATM cells. Alternatively, voice packets may be formatted into ATM AAL2 "mini-packets," one or more of which are encapsulated into ATM cells.

The conversion between packet and TDM involves voice encoding or decoding using standard ITU codecs such as G.711, to provide toll-quality voice. One of the other codecs (for example, G.723.1, G.726 or G.729) can provide near-toll-quality voice by compressing the data, allowing more efficient network bandwidth use. Echo cancellation is employed to remove near-end echo that can be introduced by mismatches between hybrid impedances and low-cost end user equipment. Packet networks can also introduce an array of problems, such as lost packets, packet errors or even delayed and out of order delivery. These can all effect the QoS in a voice system. QoS can be maintained in these systems through effective jitter buffers that can overcome these problems. The voice coding and echo cancellation is most suited to a DSP, which is coupled with a TDM interface to provide a connection to the PSTN network.

A high-performance communications processor with the appropriate protocol interfaces is required to provide the conduit to the packet network, performing uplink aggregation, downlink routing and, if required, the protocol interworking between ATM and IP.



Freescale Semiconductor offers complete solutions for all aspects of media gateway, server and switch implementations. These include Freescale's DSPs based on StarCore™ technology, which convert and compress TDM voice circuits into packet- or cell-based flows, the PowerQUICC™ communications processors required to terminate or switch the packet- or cell-based circuits and, if required, host processors built on Power Architecture™ technology to implement the control functions that manage each voice connection.

The Quad-Core MSC8144 DSP Based on StarCore Technology

The MSC8144 offers the performance and flexibility required for current and future packet telephony, wireless and video transcoding applications and is carefully optimized for minimal cost, power and area per channel.

The MSC8144 includes four high-performance SC3400 StarCore DSP subsystems and is binary compatible with the SC140 core used in the MSC812x DSP family and SC1400 core used in the MSC711x DSP family. Each SC3400 core connects to both a 16 KB 8-way Level 1 instruction cache (I-Cache) and a 32 KB 8-way Level 1 data cache (D-Cache). Each DSP core has four ALUs and performs 3200/4000 16 x 16-bit DSP MMACS at 800 MHz/1 GHz yielding up to a maximum of 12800/16000 MMACS per device. Video applications that use 8 x 8-bit MAC instructions can achieve 25600/32000 8 x 8-bit MMACS per device.

Key Features

- 512 KB of M2 shared memory
- 10 MB of M3 shared memory
- L1 instruction and data caches optimized for packet telephony
- 128K of shared L2 I-cache
- DDR memory controller
- Serial RapidIO® interface
- Dual Ethernet Controller 10/100/1000 Mbps supporting RGMII, SMII, MII, RMII, SMII
- ATM controller supporting various ATM adaptation layers
- Eight 512-channel (256 receive and 256 transmit TDM interfaces)
- 16-channel DMA controller
- 32-bit PCI interface running at 66/33 MHz
- UART and I^2C interface