

# RF LDMOS Wideband Integrated Power Amplifiers

The MD71C2250N wideband integrated circuit is designed with on-chip matching that makes it usable from 2000 to 2200 MHz. This multi-stage structure is rated for 24 to 32 Volt operation and covers all typical cellular base station modulation formats.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1(A+B)} = 80$  mA,  $I_{DQ2(A+B)} = 520$  mA,  $P_{out} = 5.3$  Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	PAE (%)	ACPR (dBc)
2110 MHz	31.2	17.0	-48.3
2140 MHz	31.1	16.8	-49.3
2170 MHz	31.1	16.8	-50.1

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2140 MHz, 63 Watts CW Output Power (3 dB Input Overdrive from Rated  $P_{out}$ )
- Typical  $P_{out}$  @ 1 dB Compression Point  $\approx 54$  Watts CW

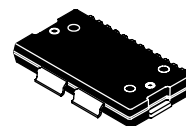
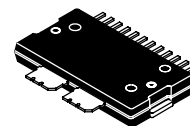
### Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

**MD71C2250NR1**  
**MD71C2250GNR1**  
**MD71C2250NBR1**

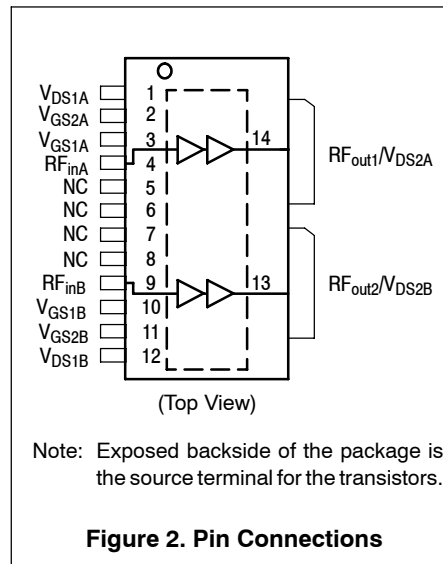
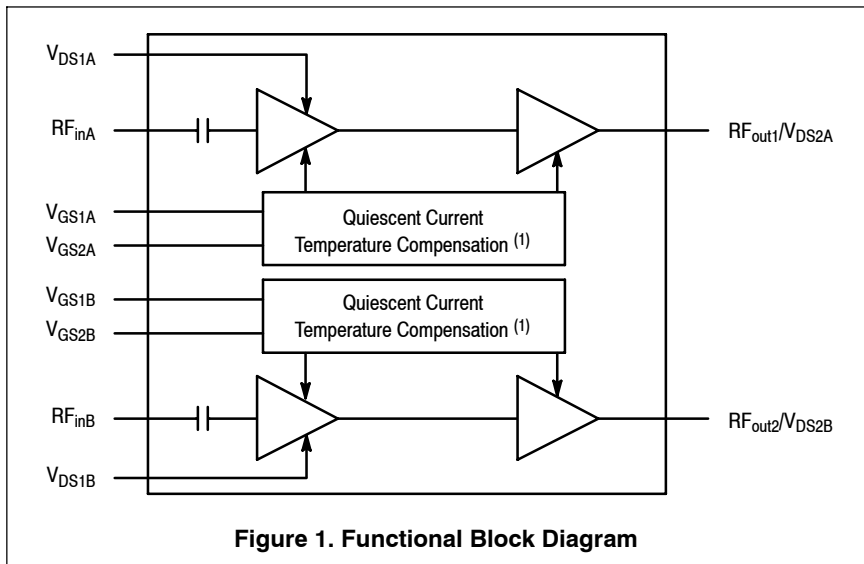
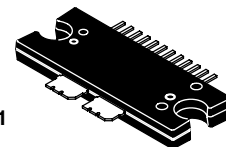
**2110-2170 MHz, 5.3 W AVG., 28 V**  
**SINGLE W-CDMA**  
**RF LDMOS WIDEBAND**  
**INTEGRATED POWER AMPLIFIERS**

**CASE 1618-02**  
**TO-270 WB-14**  
**PLASTIC**  
**MD71C2250NR1**



**CASE 1621-02**  
**TO-270 WB-14 GULL**  
**PLASTIC**  
**MD71C2250GNR1**

**CASE 1617-02**  
**TO-272 WB-14**  
**PLASTIC**  
**MD71C2250NBR1**



1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C
Input Power	$P_{in}$	28	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 5.3 W CW, 2170 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)} = 80$ mA Stage 2, 28 Vdc, $I_{DQ2(A+B)} = 520$ mA Case Temperature 80°C, 50 W CW, 2170 MHz Stage 1, 28 Vdc, $I_{DQ1(A+B)} = 80$ mA Stage 2, 28 Vdc, $I_{DQ2(A+B)} = 520$ mA	$R_{\theta JC}$	5.3 1.1 5.0 0.95	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	II (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 1 - Off Characteristics (4)</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$
<b>Stage 1 - On Characteristics</b>					
Gate Threshold Voltage (4) ( $V_{DS} = 10$ Vdc, $I_D = 23$ $\mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28$ Vdc, $I_{DQ1(A+B)} = 80$ mA)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_{DQ1(A+B)} = 80$ mA, Measured in Functional Test)	$V_{GG(Q)}$	6.0	7.0	8.0	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 2 - Off Characteristics</b> (1)					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 2 - On Characteristics**

Gate Threshold Voltage (1) ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 150\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2(A+B)} = 520\text{ mA}$ )	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2(A+B)} = 520\text{ mA}$ , Measured in Functional Test)	$V_{GG(Q)}$	5.5	6.3	7.5	Vdc
Drain-Source On-Voltage (1) ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.24	1.2	Vdc

**Functional Tests** (2,3) (In Freescale Wideband 2110–2170 Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1(A+B)} = 80\text{ mA}$ ,  $I_{DQ2(A+B)} = 520\text{ mA}$ ,  $P_{out} = 5.3\text{ W Avg.}$ ,  $f = 2170\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	30.0	31.1	34.0	dB
Power Added Efficiency	PAE	15.0	16.8	—	%
Adjacent Channel Power Ratio	ACPR	—	-50.1	-47.0	dBc
Input Return Loss	IRL	—	-14	-9	dB

**Typical Broadband Performance** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1(A+B)} = 80\text{ mA}$ ,  $I_{DQ2(A+B)} = 520\text{ mA}$ ,  $P_{out} = 5.3\text{ W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Frequency	$G_{ps}$ (dB)	PAE (%)	ACPR (dBc)	IRL (dB)
2110 MHz	31.2	17.0	-48.3	-9
2140 MHz	31.1	16.8	-49.3	-11
2170 MHz	31.1	16.8	-50.1	-14

- Each side of device measured separately.
- Part internally matched both on input and output.
- Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performance</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1(A+B)} = 80\text{ mA}$ , $I_{DQ2(A+B)} = 520\text{ mA}$ , 2110–2170 MHz Bandwidth					
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	54	—	W
IMD Symmetry @ 50 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD <sub>sym</sub>	—	16	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	70	—	MHz
Quiescent Current Accuracy over Temperature (1,2) with 4.7 k $\Omega$ Gate Feed Resistors (-30 to 85°C)	$\Delta I_{QT}$	—	1.5	—	%
		—	5.0	—	
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 5.3\text{ W Avg.}$	$G_F$	—	0.1	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.028	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1\text{dB}$	—	0.028	—	dB/°C

1. Each side of device measured separately.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf.Select Documentation/Application Notes - AN1977 or AN1987>.

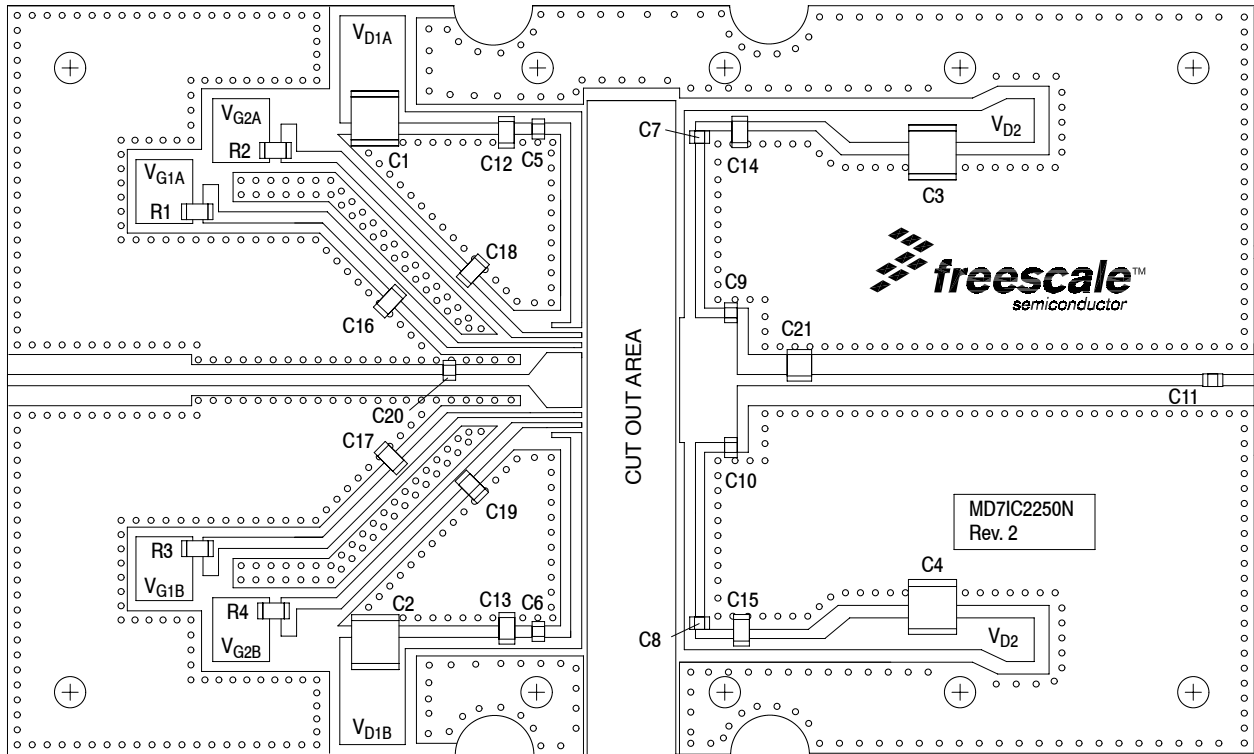


Figure 3. MD7IC2250NR1(GNR1)(NBR1) Test Circuit Component Layout

Table 6. MD7IC2250NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	10 $\mu$ F Chip Capacitors	GRM55DR61H106KA88L	Murata
C5, C6, C7, C8	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C9, C10	2.0 pF Chip Capacitors	ATC600F2R0BT250XT	ATC
C11	33 pF Chip Capacitor	ATC600F330JT250XT	ATC
C12, C13	1.0 $\mu$ F Chip Capacitors	GRM31MR71H105KA88L	Murata
C14, C15, C16, C17, C18, C19	4.7 $\mu$ F Chip Capacitors	GRM31CR71H475KA12L	Murata
C20	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C21	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
R1, R2, R3, R4	4.7 k $\Omega$ Chip Resistors	CRCW12064K70FKEA	Vishay
PCB	0.020", $\epsilon_r = 3.5$	RF35A2	Taconic

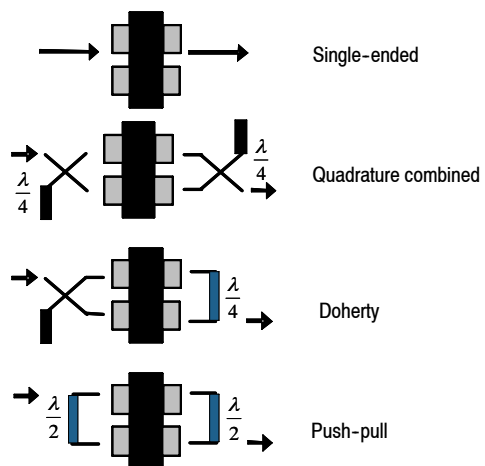
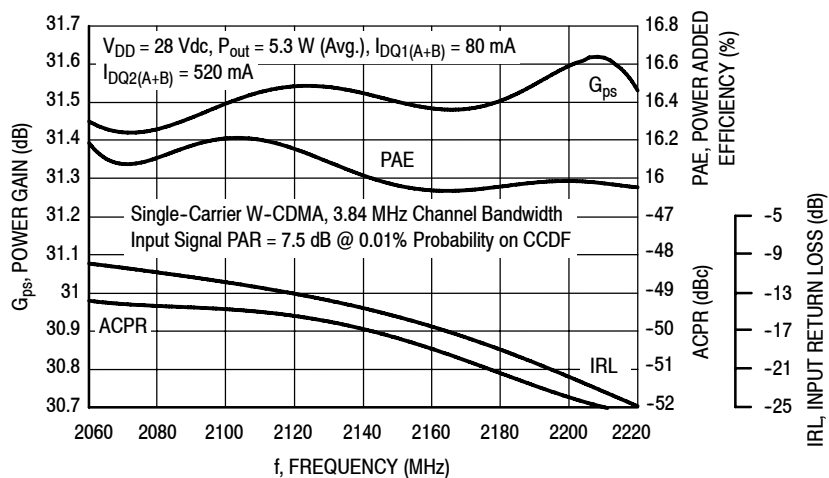
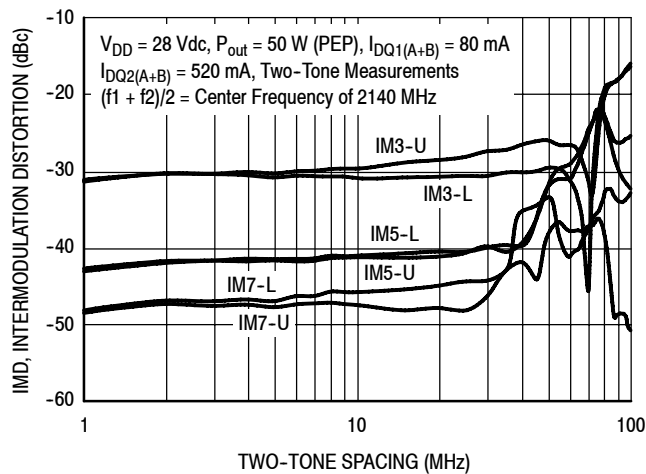


Figure 4. Possible Circuit Topologies

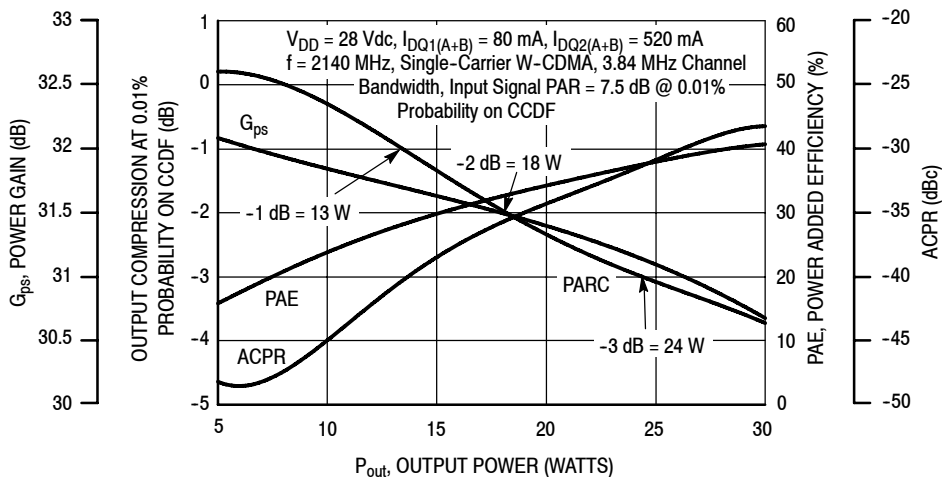
### TYPICAL CHARACTERISTICS



**Figure 5. Power Gain, Power Added Efficiency, IRL and ACPR Broadband Performance @  $P_{out} = 5.3$  Watts Avg.**

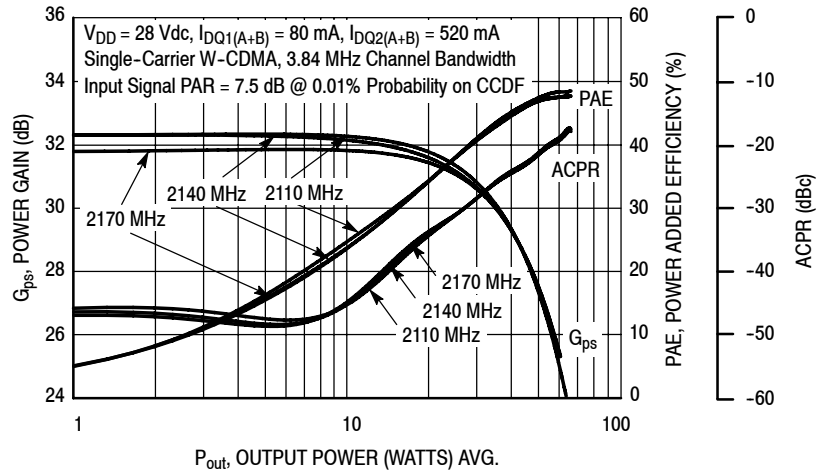


**Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing**

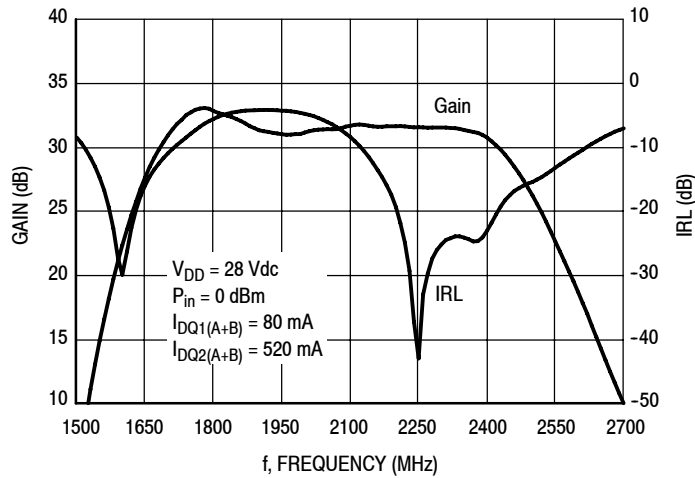


**Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS



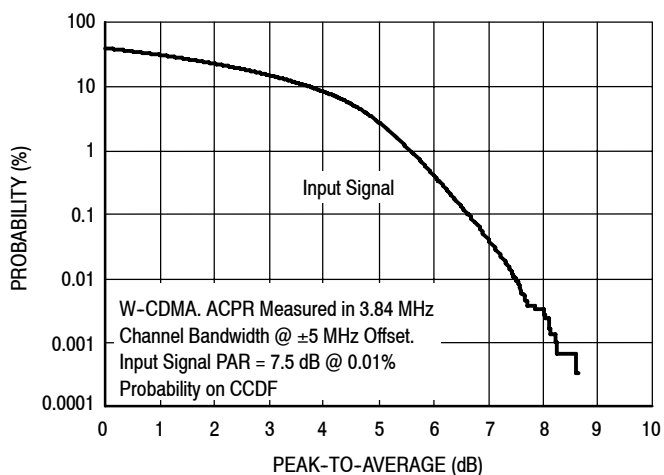
**Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**



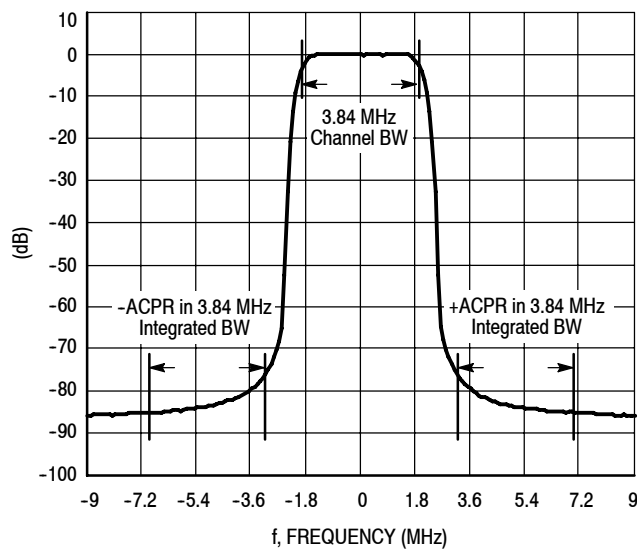
**Figure 9. Broadband Frequency Response**



### W-CDMA TEST SIGNAL



**Figure 10. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**



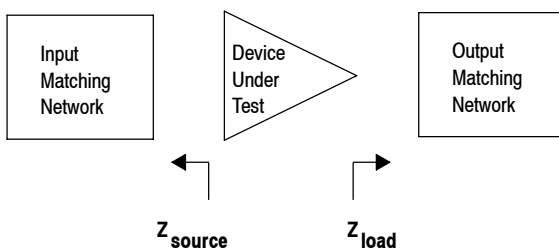
**Figure 11. Single-Carrier W-CDMA Spectrum**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1(A+B)} = 80 \text{ mA}$ ,  $I_{DQ2(A+B)} = 520 \text{ mA}$ ,  $P_{out} = 5.3 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2060	$17.0 + j4.49$	$5.12 - j3.98$
2080	$17.2 + j4.94$	$5.07 - j4.10$
2100	$17.4 + j5.41$	$5.00 - j4.23$
2120	$17.7 + j5.88$	$4.90 - j4.36$
2140	$17.9 + j6.36$	$4.76 - j4.88$
2160	$18.2 + j6.84$	$4.59 - j4.60$
2180	$18.4 + j7.33$	$4.38 - j4.69$
2200	$18.7 + j7.84$	$4.15 - j4.77$
2220	$19.0 + j8.35$	$3.91 - j4.82$

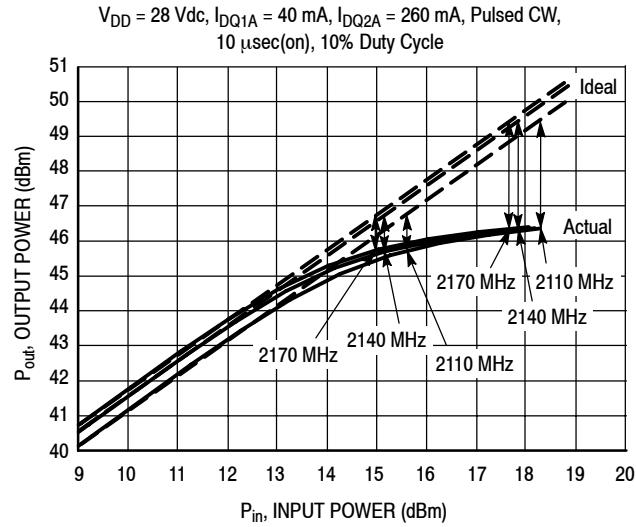
$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.



**Figure 12. Series Equivalent Source and Load Impedance**

## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
2110	38	45.8	44	46.4
2140	37	45.7	44	46.4
2170	37	45.7	44	46.4

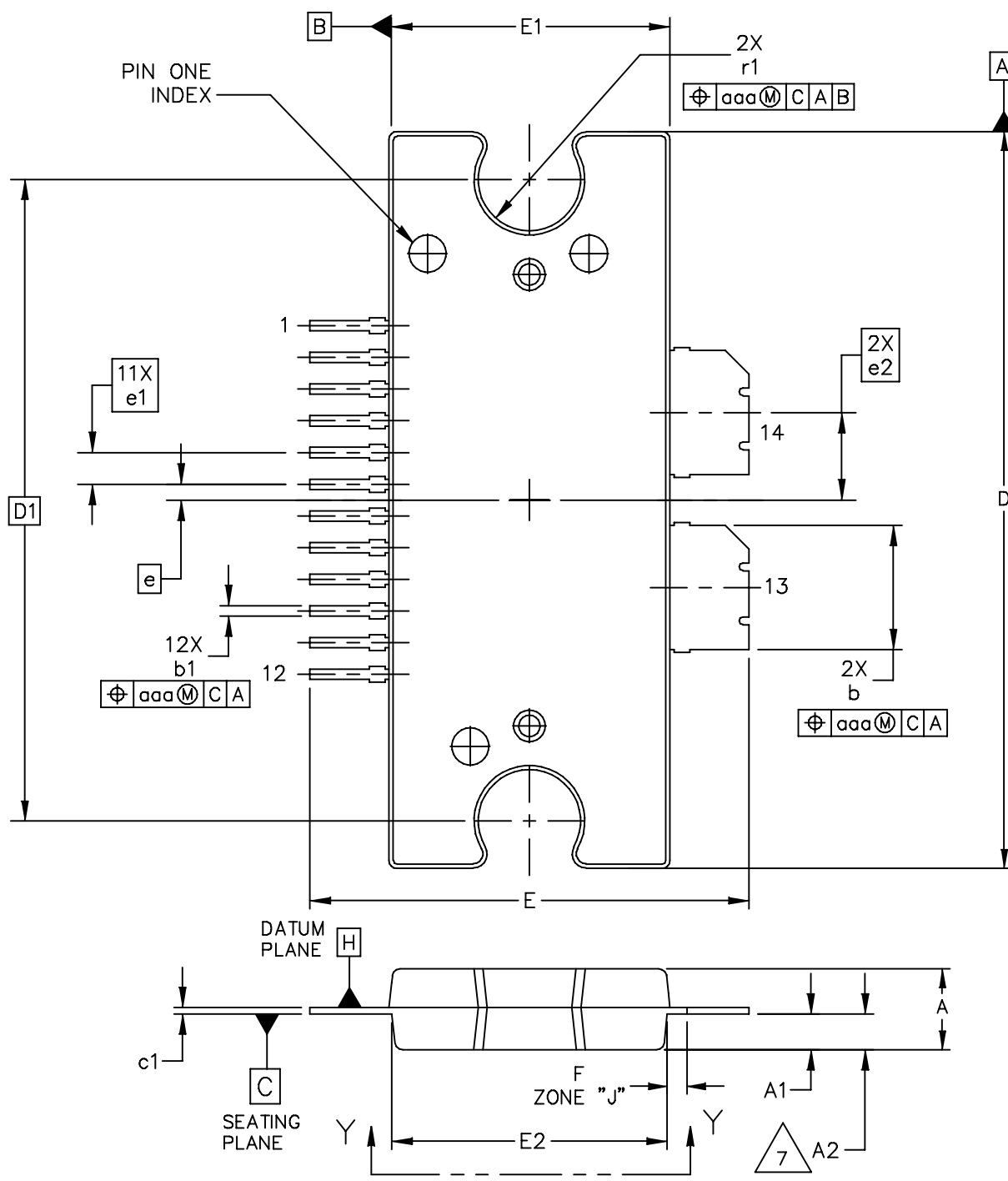
Test Impedances per Compression Level

f (MHz)		$Z_{\text{source}}$ $\Omega$	$Z_{\text{load}}$ $\Omega$
2110	P1dB	65.6 + j43.6	7.09 - j14.1
2140	P1dB	58.7 + j39.7	6.88 - j14.0
2170	P1dB	52.4 + j32.5	6.99 - j14.5

**Figure 13. Pulsed CW Output Power versus Input Power @ 28 V**

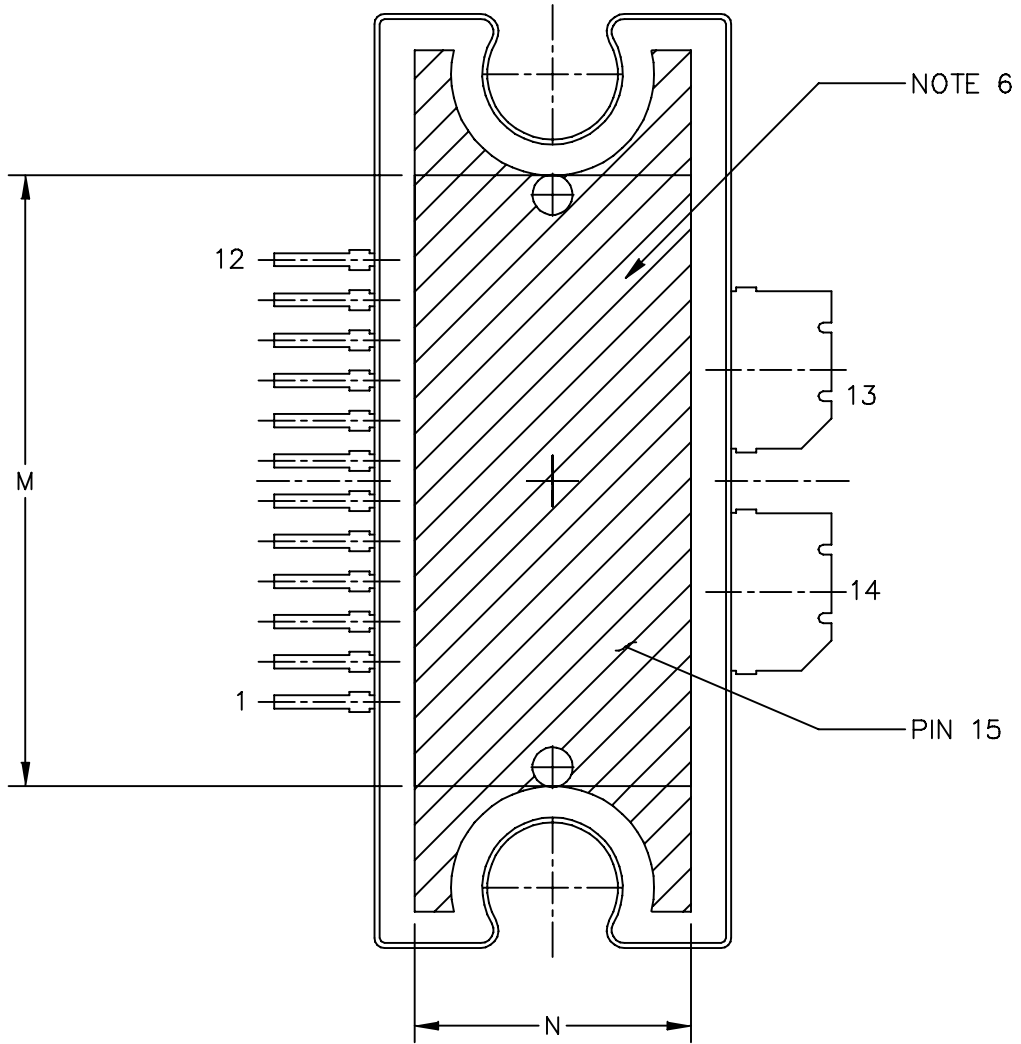
Note: Measurement made on a single path of the device under Class AB conditions.

### PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D	REV: A
	CASE NUMBER: 1617-02	27 JUN 2007
	STANDARD: NON-JEDEC	

MD71C2250NR1 MD71C2250GNR1 MD71C2250NBR1



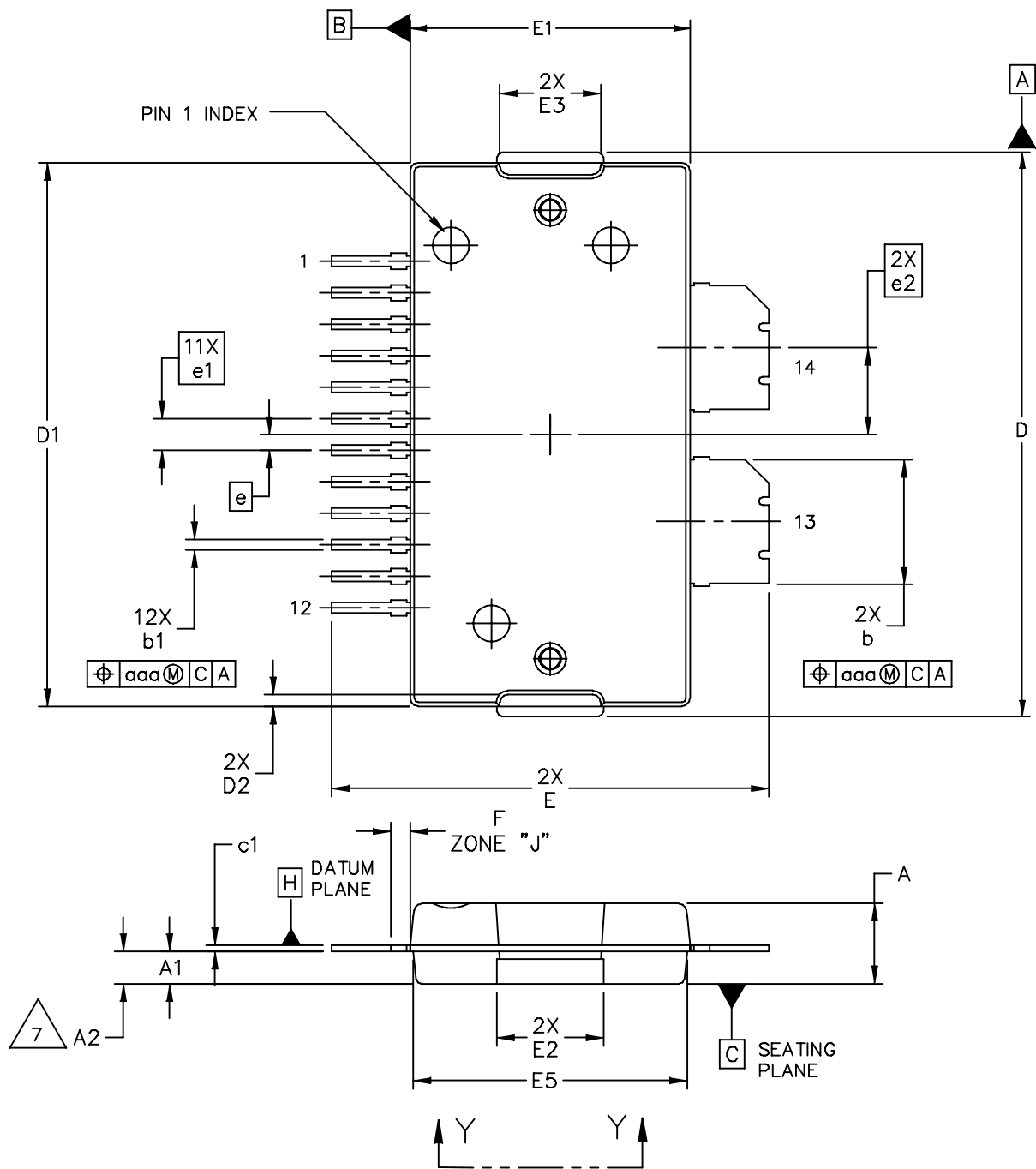
VIEW Y-Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D	REV: A	
	CASE NUMBER: 1617-02	27 JUN 2007	
	STANDARD: NON-JEDEC		

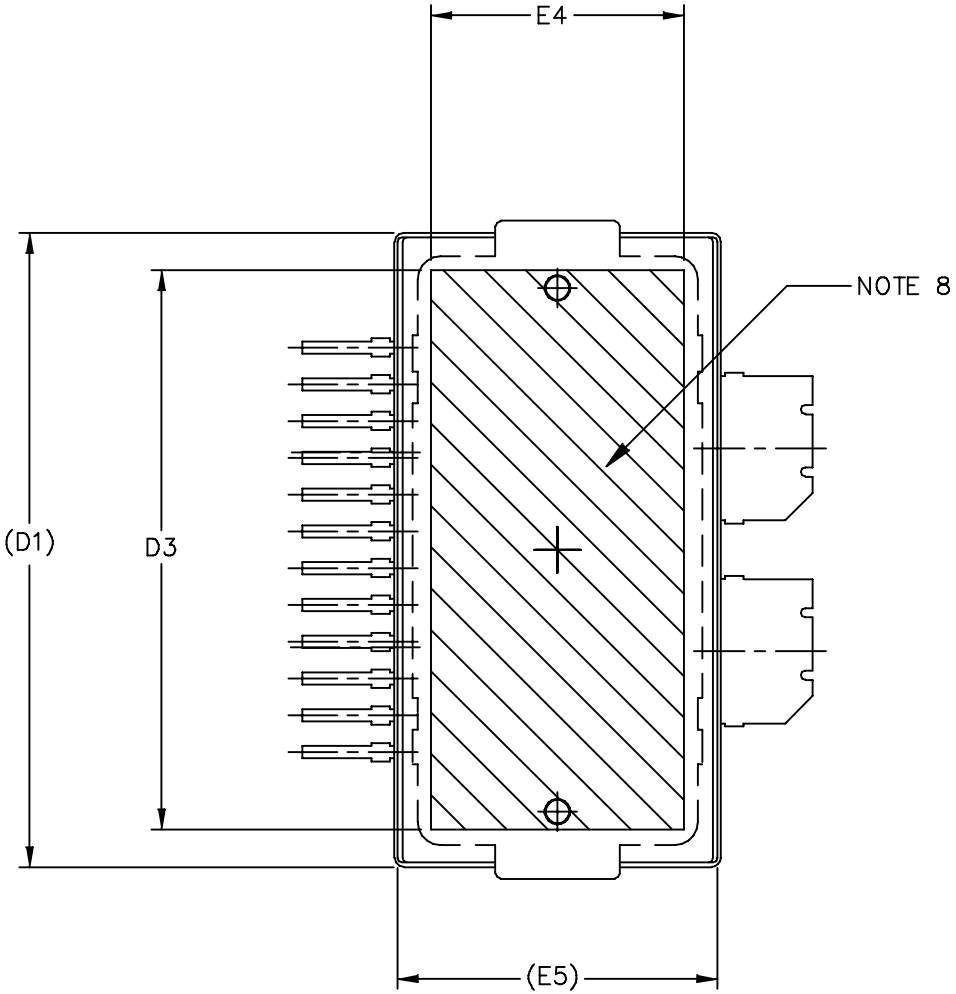
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.154	.160	3.91	4.06
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.810 BSC		20.57 BSC		e1	.040 BSC		1.02 BSC	
E	.551	.559	14.00	14.20	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	r1	.063	.068	1.6	1.73
E2	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----					
N	.270	----	6.86	----					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE:  TO-272 WIDE BODY 14 LEAD					DOCUMENT NO: 98ASA10649D			REV: A	
					CASE NUMBER: 1617-02			27 JUN 2007	
					STANDARD: NON-JEDEC				



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: A	
	CASE NUMBER: 1618-02	19 JUN 2007	
	STANDARD: NON-JEDEC		



VIEW Y-Y

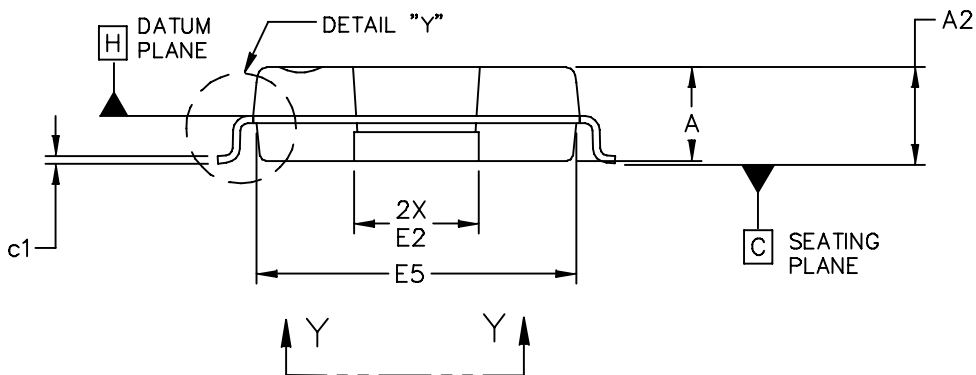
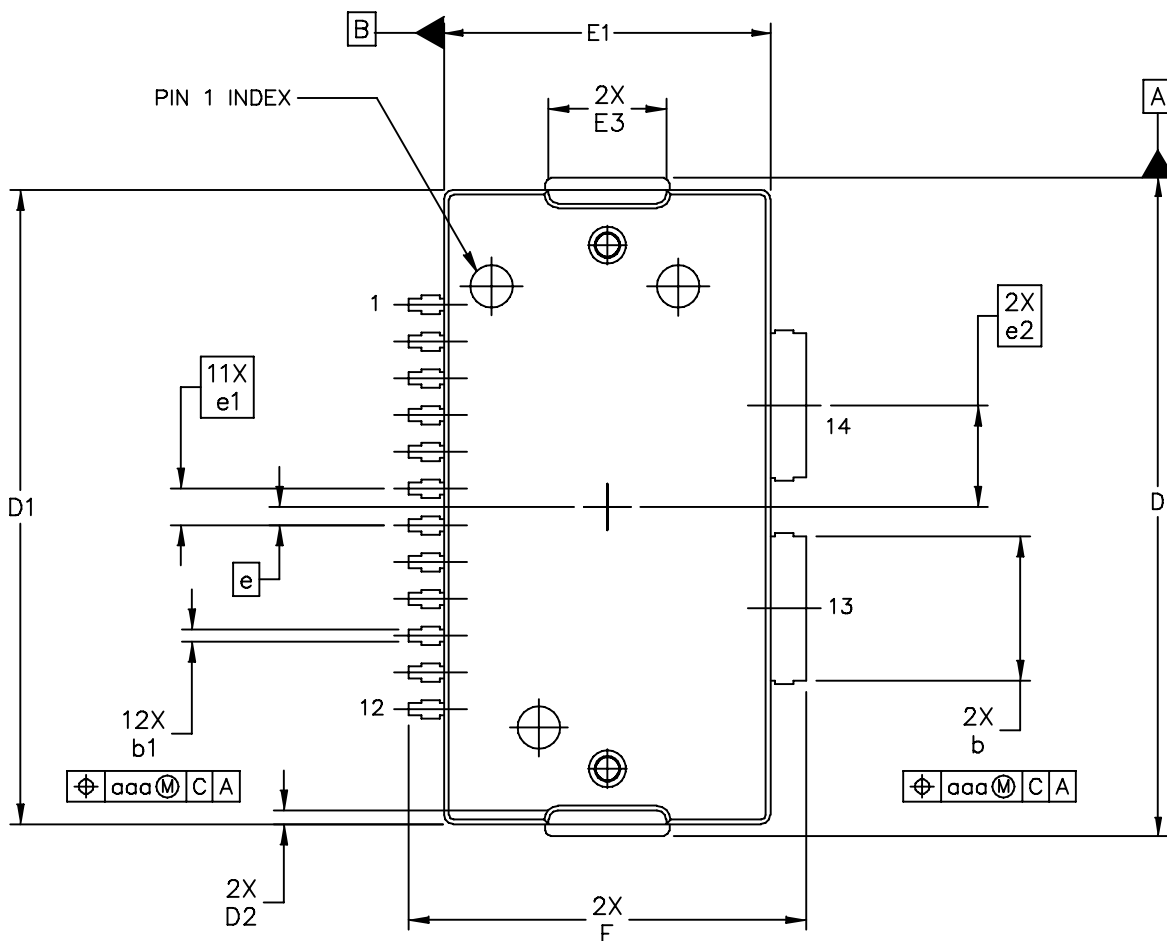
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD		DOCUMENT NO: 98ASA10650D	REV: A
		CASE NUMBER: 1618-02	19 JUN 2007
		STANDARD: NON-JEDEC	



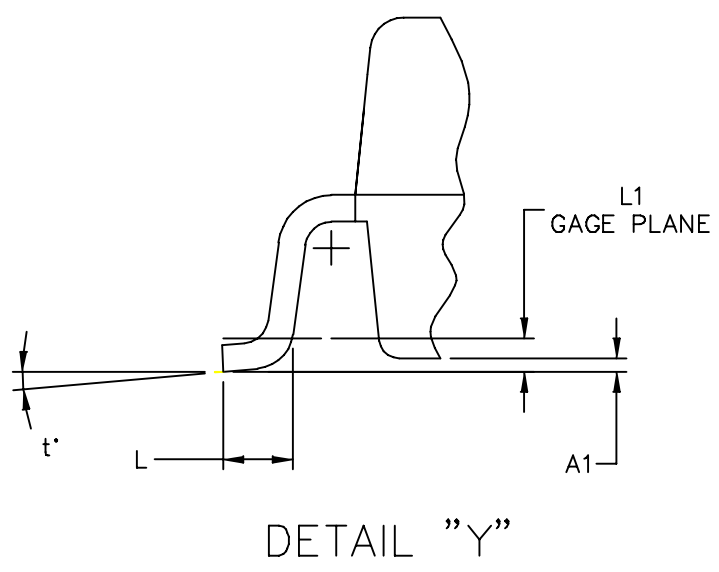
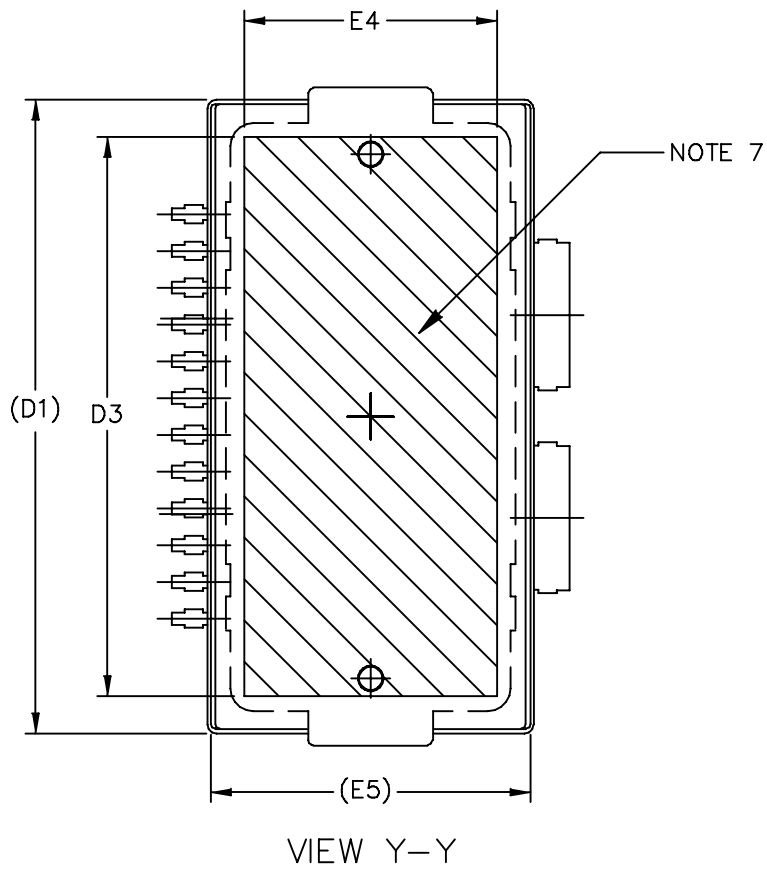
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: TO-270 WIDE BODY 14 LEAD					DOCUMENT NO: 98ASA10650D			REV: A	
					CASE NUMBER: 1618-02			19 JUN 2007	
					STANDARD: NON-JEDEC				



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD GULL WING	DOCUMENT NO: 98ASA10653D	REV: A	
	CASE NUMBER: 1621-02	19 JUN 2007	
	STANDARD: NON-JEDEC		



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 WIDE BODY 14 LEAD GULL WING	DOCUMENT NO: 98ASA10653D	REV: A	
	CASE NUMBER: 1621-02	19 JUN 2007	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2'	8'	2'	8'
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: TO-270 WIDE BODY 14 LEAD GULL WING					DOCUMENT NO: 98ASA10653D			REV: A	
					CASE NUMBER: 1621-02			19 JUN 2007	
					STANDARD: NON-JEDEC				

## PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2010	<ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **Web Support:**

<http://www.freescale.com/support>

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
1-800-441-2447 or +1-303-675-2140  
Fax: +1-303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2010. All rights reserved.