

MOTOROLA

Part: MPC555.K
Mask Set: 01K02A

Transportation Systems Group

Errata Sheet



Customer Errata and Information Sheet

Transportation Systems Group



Part: MPC555.K Mask Set: 01K02A. Report generated 30 March 2000 .

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BBC.CDR1UBUS_03_0	
CMF.192KB_CDR1UBUS_03_0A	
CMF.256KA_CDR1UBUS_03_0A	
DPTRAM.6K_CDR1IMB3_03_0	
JTAG.CDR1_01_0	
L2U.CDR1LBUSUBUS_02_0	
LRAM.10KA_CDR1LBUS_02_0	
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MIOS1.CDR1IMB3_02_0	
PKPADRING.555_CDR1_02_0B	
RCPU.CDR1LBUSIBUS_13_0	
QADC64.CDR1IMB3_02_0B	
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ERRATA AND INFORMATION SUMMARY

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- AR_381 New Features on MPC555 mask revision J76N an later
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- AR_214 Only negate interrupts while the EE bit (MSR) disables interrupts
- AR_478 QADC64: Don't use channel 63 "End Of Queue".
- AR_563 QSM/QSMCM/QADC64 corrupts data after an IACK cycle in CISC parts.
- AR_754 QADC64: Do not use queue1 in external gated mode with queue2 in continuous mode.
- AR_421 QADC64: Don't switch to software triggered continuous scan after completing Q1.
- AR_422 QADC64: Do not rely on set of TOR1 in external gated continuous scan mode
- AR_419 QADC64: False trigger upon configuration (Does NOT apply to ALL parts)

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AR_420 QADC64: Don't change BQ2 with a set of SSE2 without a mode change.
AR_435 QADC64: TOR1 flag operates in both single and continuous external gated modes.
AR_563 QSM/QSMCM/QADC64 corrupts data after an IACK cycle in CISC parts.
AR_584 QSMCM: Do not use link baud and ECK modes
AR_627 TPU: (Microcode) Add neg_mrl with write_mer and end_of_phase
AR_577 TPU3 - TCR2PSCK2 bit does not give TCR2 divide ratios specified.
AR_498 UIMB: Read failures occur for IMB accesses when IMB clock is half speed
AR_582 USIU: Under certain conditions, XFC stuck at 0V on power-on
AR_595 USIU: PLL will not lock on power-on, use limp mode and switch via software
AR_610 Additional current on KAPWR when power is not applied
AR_479 USIU: The MEMC does not support external master burst cycles
AR_679 USIU: In slave mode, do not use write slave accesses
AR_389 Little Endian modes are not supported
AR_442 Avoid loss of clock during HRESET
AR_594 USIU: Changing PLL MF to 1:1 mode can have 180 degree phase shift
AR_687 USIU: Program reserved bits in PDMCR to preserve compatibility
AR_598 USIU: Ensure proper configuration for proper startup

DETAILED ERRATA DESCRIPTIONS

CDR_AR_252	Customer Erratum	MPC555.K
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Censorship has been disabled within the CMF

DESCRIPTION:

The censorship mode for the CMF modules has been disabled. The value of the CMF Censor bits will not provide any protection of the contents of the CMF memory array.

WORKAROUND:

To ensure similar behavior on future revisions with censorship enabled, boot code residing within the CMF flash module should set the ACCESS bit.

CDR_AR_697	Customer Information	MPC555.K
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Revised operating currents

DESCRIPTION:

Characterization of silicon indicates that the operating current specifications must be updated. The total current is not anticipated to change significantly, but will be redistributed amongst VDDL, VDDI, KAPWR, VDDSRAM, VDDSYN, and VDDF.

WORKAROUND:

Refer to electrical specification 3.3 or later for revised values.

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CDR_AR_381	Customer Information	MPC555.K
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New Features on MPC555 mask revision J76N and later

DESCRIPTION:

Several new features were added to the MPC555 starting with mask revision 00J76N and also included in revisions K02A. In the USIU, the DBCT and DBSLR clock control bits were added ("Disable backup clock for timers", "Disable clock switch in loss of lock and reset"). In the USIU, a mode was added to allow the WE pins to also assert on reads, allowing the usage of some SRAMS. An additional "MTS" function has been multiplexed onto the IRQ2/CR/SGPIO2 pin. The MTS pin allows for sharing of additional types of devices in a multi-master system. In addition, the CMF FLASH programming control has changed. The recommended connection of the VSSSYN pin has changed. The recommended connection of the crystal has changed (resistor is now internal).

WORKAROUND:

Consult a revised users manual (15 September 1998 or later) to determine how to use these features. Use the latest version of the FLASH programming tools (version 1.1 or later of CMF_DEMO routines).

CDR_AR_412	Customer Information	MPC555.K
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Avoid instruction fetches from IMB/UIMB memory map

DESCRIPTION:

Instruction fetches on the IMB or to UIMB control registers may result in improper operation, possibly requiring reset to continue.

WORKAROUND:

Avoid instruction fetches from the IMB/UIMB memory map. Program the IMPU to disable instruction accesses to the IMB/UIMB memory map.

CDR_AR_597	Customer Information	MPC555.K
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AC timing changes

DESCRIPTION:

Some of the AC timing specifications have changed. Refer to electrical specification 3.3 or later for new values. See CDR_AR_524 for AC timing specification 30. In addition, the following electrical specifications have changed to the following new values: {sp7, sp7a, sp7b, sp7c, sp7d} 4ns, {sp8a, sp8c, sp8d} 14ns, sp8b 15ns, sp10 14ns, sp11 14ns, sp15 12ns, sp15b 8ns, sp22 9ns, sp28 9ns, sp41 18ns. D(0:31) has been moved from sp7 and sp8 to sp7d and sp8d.

WORKAROUND:

Ensure external devices are matched to these specifications.

CDR_AR_588	Customer Information	MPC555.K
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MASKNUM field in USIU is 0x20

DESCRIPTION:

MASKNUM field in USIU has been changed to 0x20 and will change on future revisions.

WORKAROUND:

Modify software to expect new value (0x20) for the MASKNUM field.

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CDR_AR_636	Customer Erratum	CMF.192KB_CDR1UBUS_03_0A
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CMF: Program at reduced temperature and voltage ranges

DESCRIPTION:

There may be insufficient program margin to be able to correctly read all bits of the array at cold with 3.0Vdd if the part was programmed at hot.

WORKAROUND:

Workarounds in order of effectiveness: First, reduce temperature while programming. Second, reduce Vpp while programming. Third, increase VDD while programming and reading. During programming, limit the maximum ambient temperature to 85C, and Vdd to 3.3V +/- 5%. This allows sufficient margin to read flash cells over the entire specified temperature and voltage ranges. By further restricting Vdd to 3V +/- 5% during all operations (including flash read), the maximum programming temperature may be increased to 90C with sufficient program margin to operate over the entire temperature range.

CDR_AR_730	Customer Information	CMF.192KB_CDR1UBUS_03_0A
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Excessive pulses required for setting censorship.

DESCRIPTION:

Setting the censor bits with the released driver code takes an excessive amount of pulses (100's when it should be 10-15). Root Cause: With the previous release driver code which follows the old published censorship set algorithm, the row addresses to the array varied during high voltage set operations. These row addresses caused some high voltage logic in the array to vary, placing a load on the charge pump whenever the address changed. As a result, the charge pump was overloaded and insufficient voltage was applied to the fuse during the set pulses.

WORKAROUND:

Use the latest driver code (CMF Parallel Driver v2.2 or later) which includes the following fix. For Setting the censor bit, insert program interlock write prior to writing EHV. But if the transition is from 00 to 01 and the ACCESS bit[s] is/are not set and software is running in censored mode, do not perform the interlock write[s], and instead after writing the EHV bit[s] ensure that U-bus addresses 17:25 do not change for the 100ms pulse duration. (Perform a tight loop which lasts > 100ms, do not poll HVS bit[s] during that loop, ensure that the loop and any associated prefetching or operand accesses does not result in addresses which alter A[17:25] on the u-bus.)

CDR_AR_522	Customer Information	CMF.192KB_CDR1UBUS_03_0A
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CMF: PAWS bits always read as 0

DESCRIPTION:

The PAWS bits in the CMFTST register are not readable. They will always read as 0, even if they are in a different state.

WORKAROUND:

Avoid reading the PAWS bits to confirm the proper programming.

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CDR_AR_449	Customer Information	CMF.192KB_CDR1UBUS_03_0A
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Updated Flash Programming Algorithm

DESCRIPTION:

The program/erase pulse algorithm has changed. Consult the latest flash programming algorithm for the number and method of applying pulses. The program pulse width (subject to change) should be 25.6us. The erase pulse width should be 1s (for all revisions of all parts). Longer program or erase pulse widths can result in improper program or erase. Previous revisions (Rev. A, Rev. C) of the part should continue using shorter programming pulses. The programming algorithm and pulse widths are still subject to change.

WORKAROUND:

Update erase pulse widths. Obtain the latest programming algorithm.

CDR_AR_485	Customer Information	DPTRAM.6K_CDR1IMB3_03_0
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Disable of TPU emulation mode while MISC enabled corrupts data in RAM

DESCRIPTION:

If the TPU emulation mode is negated while MISC is enabled, the DPTRAM data may be corrupted.

WORKAROUND:

In test mode / TPU development mode, disable the MISCEN (DPTMCR) before negation of TPEMEM in the TCR. In normal mode, disable MISCEN prior to performing a soft reset of the TPU (TPUMCR2).

CDR_AR_445	Customer Erratum	MIOS1.CDR1IMB3_02_0
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Potential trap state in MIOS MDASM in OPWM mode.

DESCRIPTION:

A trap state is entered when a value of MDASMBR is written in OPWM mode, to a value which is out of the counter bus range. For example, if the modulus value of the MCSM driving the counter bus is \$FF00 and if MDASMBR is written to a value less than \$FF00, then a match is never made on channel B hence a B1 to B2 transfer never occurs. To get out of the trap, the MDASM mode should be reset back to idle.

WORKAROUND:

Ensure that the software never writes MDASMBR (in OPWM mode) to a value which is less than the MCSMMOD value.

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CDR_AR_468	Customer Erratum	MIOS1.CDR1IMB3_02_0
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Configure MIOS/VF/VFLS pins as all MIOS or all VF/VFLS

DESCRIPTION:

The MIOS VF/VFLS multiplexer must not be individually programmed. These pins can be configured either as VF/VFLS or as all MIOS pins. Do not configure bit[0:1] of the MIOS1TPCR register as 2'b01 or 2'b10.

WORKAROUND:

Whenever the user wishes to configure the MIOS/VF/VFLS pins, software should write 2'b11 or 2'b00 to bit[0:1] of the MIOS1TPCR register. This will allow the pins to be either all MIOS functions or all development support functions. The pins should never be configured separately.

CDR_AR_443	Customer Erratum	MIOS1.CDR1IMB3_02_0
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MIOS: Do not write data into the MDASMBR when in an input mode.

DESCRIPTION:

The MDASMBR register can be loaded via a write from the IMB, from the counter bus OR from a transfer from the MDASMAR to the MDASMBR register. The transfer from MDASMAR to MDASMBR only happens in input modes, when the software should not normally write into MDASMBR. However, no hardware exists to prevent a simultaneous transfer from MDASMAR and write to MDASMBR. As a result, during a simultaneous transfer and write, the resulting data in MDASMBR will be undefined. The specification does not define what happens in this case.

WORKAROUND:

When in an input mode, do not write to MDASMBR.

CDR_AR_444	Customer Erratum	MIOS1.CDR1IMB3_02_0
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MIOS: Warning in MDASM OPWM mode when MDASMAR = MDASMBR.

DESCRIPTION:

In OPWM mode when a comparison occurs simultaneously on register A and B (i.e. they have the same value stored), the pin is reset or stays reset. The specification states that the transfer between B1 and B2 should occur when the pin is low. However this is not necessarily the case when a simultaneous A&B compare occurs. If the pin was previously low then the transfer would not happen until after the next compare.

WORKAROUND:

1): Avoid setting MDASMAR = MDASMBR when in OPWM mode. 2): To come out of MDASMAR = MDASMBR when in OPWM mode change the value of MDASMAR first. 3): Be aware that it may take an extra match to update MDASMBR B2 than expected, after a new value is written to MDASMBR B1.

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CDR_AR_446	Customer Erratum	MIOS1.CDR1IMB3_02_0
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MIOS: Avoid 100% pulse in MDASM OPWM mode.

DESCRIPTION:

A two cycle system clock "glitch" (to logic "0") may occur when 100% output state is entered in MDASM OPWM mode. 100% pulse is entered by writing B register bit 15 high when using less than 16 bit resolution. The problem occurs only when B register bit 15 is set while the pin is high; the glitch occurs on the next match on the B register. This glitch is only seen the first time a match on B causes 100% mode to be entered. No glitches will be seen on subsequent matches.

WORKAROUND:

- Use the pads with the slow slew rate. Then at 40 Mhz no glitch will be seen on the output pin.- If B register bit 15 is only set while the pin is low then there will not be any glitch on the pad. The change to 100% will occur 2 cycles after the setting of B register bit 15. Invert the polarity of the output. Then setting A=B will cause a 100% pulse. A glitch free 0% pulse is now no longer possible.

CDR_AR_517	Customer Erratum	MIOS1.CDR1IMB3_02_0
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MIOS: Read MIOS1VNR and MIOS1TCPR registers are undefined

DESCRIPTION:

A read of the MIOS1VNR and MIOS1TCPR registers will produce undefined data. All writes to the MIOS1TCPR will be performed correctly and cause the appropriate actions, but the values read from MIOS1TCPR will be undefined.

WORKAROUND:

Avoid reading the MIOS1VNR and MIOS1TCPR registers.

CDR_AR_624	Customer Erratum	MIOS1.CDR1IMB3_02_0
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MIOS: Use even values in MPWMSMPERR

DESCRIPTION:

In some operating conditions on some parts, the MPWMSM period may be off by one count. The load of the MIOS MPWMSM counter LSB is not guaranteed to function correctly over all conditions. In some cases, the MIOS MPWMSM cannot load a MPWMSM period LSB (Least significant bit of MPWMSMPERR) as a "1" into the MPWMSM counter (MPWMSMCNTR). The counter LSB will be incorrectly loaded as a "0". The period of the PWMSM counter will then be one MPWMSM prescaler clock period less than programmed. There will be no problem if MPWMSM period LSB (MPWMSMPERR_PER0) is a "0". This problem is most likely to occur at lower temperatures and higher voltages, but may occur in other operating conditions. Example of failure: If the MPWMSMPERR is set to %057F, the actual value loaded into the MPWMSMCNTR will be %057E.

WORKAROUND:

Use even values in the MPWMSMPERR.

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CDR_AR_452	Customer Information	MIOS1.CDR1IMB3_02_0
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MIOS: "non-reset" registers are undefined after reset.

DESCRIPTION:

The specification states that many of the MIOS data registers are unaffected by reset. This should really be "undefined" after a reset. Note that after reset all the MIOS submodules are correctly in their idle state with the pads as inputs.

WORKAROUND:

After a reset of the MIOS a full initialization routine should be run, rather than assuming that the same values remain in the MIOS data registers.

CDR_AR_470	Customer Erratum	PKPADRING.555_CDR1_02_0B
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150V MM ESD issues

DESCRIPTION:

Not all ESD specifications are met when tested using machine model (MM) tests. All specifications are met at 100V MM. Vdda pin fails at 150V MM; low level leakage is seen on 5v output pins at 200V MM; 3v pads with keep alive power exhibit low-level leakage at 200V MM. All pads pass Human Body Model (HBM) ESD tests at 3000V and below.

WORKAROUND:

Avoid indicated ESD levels on these pins.

CDR_AR_454	Customer Erratum	PKPADRING.555_CDR1_02_0B
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Use external resistors/drivers when using external reset configuration word

DESCRIPTION:

When asserting RSTCONF to direct the MPC555 to sample the reset configuration word from the external data pins, the weak pulldowns on the data pads may not fully discharge the pins during reset. If the data pins were driven high by the MPC555 just prior to the assertion of reset, the weak pulldowns will not be able to discharge the pins due to contention with the P-channel transistor of the output buffer. This transistor is not fully turned off by the pre-driver stage.

WORKAROUND:

Program the internal flash to provide the reset configuration word. Or, use external resistors/drivers to drive all of the configuration word during reset (including bits set to 0) when providing the reset configuration word from external. An external 10K resistor is sufficient to pull a data pin to 0 during reset.

CDR_AR_524	Customer Erratum	PKPADRING.555_CDR1_02_0B
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TS_B input needs additional input hold time

DESCRIPTION:

The TS_B signal, when an input (spec. 30), requires an input hold time of 5ns.

WORKAROUND:

Keep asserting TS_B for the additional hold time. In a multi-555 system, the TS_B output hold time of one MPC555 is sufficient to meet the TS_B input hold time of another MPC555.

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CDR_AR_680	Customer Information	PKPADRING.555_CDR1_02_0B
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CLKOUT and ENGCLK drive strengths will change

DESCRIPTION:

Beginning with Revision M, the CLKOUT pad driver will be sized to drive loads of 30pf or 90pf, selectable by software. The ENGCLK pad driver will be sized to drive loads of 25pf or 50pf, selectable by software.

WORKAROUND:

Designs with clkout loads between 30pf and 45pf should evaluate setting the clkout driver to the 90pf drive mode. Designs with ENGCLK loads above 25pf should evaluate setting the ENGCLK driver to the 50pf drive mode. Designs with ENGCLK loads above 50pf should reduce the ENGCLK frequency to 10Mhz or below.

CDR_AR_736	Customer Information	PKPADRING.555_CDR1_02_0B
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CLKOUT well tie connected to wrong supply.

DESCRIPTION:

CLKOUT pad's pchannel driver has different supplies connected to the well tie and the source.

WORKAROUND:

Customers need to power up VDD_CLK ahead of VDDi, or at the same time, to prevent parasitic diode from sinking high current into the pin.

CDR_AR_440	Customer Information	RCPU.CDR1LBUSIBUS_13_0
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Execute any IMUL/DIV instruction prior to entering low power modes.

DESCRIPTION:

There is a possibility of higher than desired currents during low power modes. This is caused by a possible contention in the IMULDIV control area. This contention may only exist prior to the execution of any IMULDIV instruction.

WORKAROUND:

Execute mullw instruction prior to entering into low power modes (anytime after reset, and prior to entering the low power mode).

CDR_AR_214	Customer Information	RCPU.CDR1LBUSIBUS_13_0
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Only negate interrupts while the EE bit (MSR) disables interrupts

DESCRIPTION:

An IRQ to the core, which is negated before the core services it, may cause the core to stop fetching until reset.

WORKAROUND:

Interrupt request to the core should only be negated while interrupts are disabled by the EE bit in the MSR. Software should disable interrupts in the CPU core prior to masking or disabling any interrupt which might be currently pending at the CPU core. For external interrupts, it is recommended to use the edge triggered interrupt scheme. After disabling an interrupt, sufficient time should be allowed for the negated signal to propagate to the CPU core, prior to re-enabling interrupts. For an interrupt generated from an IMB module, 6 clocks is sufficient (for IMBCLK in 1:1 mode).

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CDR_AR_478

Customer Erratum

QADC64.CDR1IMB3_02_0B

QADC64: Don't use channel 63 "End Of Queue".

DESCRIPTION:

When operating at 150 C, low voltage, and high frequency a channel 63 written to a CCW does not properly act as an End Of Queue. The appropriate flags will recognize the End Of Queue and be set, but the queue will continue to operate past this point.

WORKAROUND:

Characterization of a small sample of parts indicates that this problem will not be seen if any of the following conditions are met: (1) Vdd must remain above 3.12 volts, or (2) Frequency must remain below 38 MHz, or (3) Temperature of part must remain below 100C, or (4) Channel 63 "End Of Queue" not used.

CDR_AR_563

Customer Erratum

QADC64.CDR1IMB3_02_0B

QSM/QSMCM/QADC64 corrupts data after an IACK cycle in CISC parts.

DESCRIPTION:

This problem does not affect parts that do not run IACK cycles (i.e. RISC CPUs). The Common BIU state machine, used by the QSM/QSMCM/QADC64, mis-tracks an IACK cycle if an interrupt is issued while an IACK cycle for the same level is in progress. In this case, the next access on the IMB3 will be corrupted by the QSM/QSMCM/QADC64. On CPU32 based parts (or CPU32X parts where the FASRAM is not used for the stack), the first access after an IACK cycles is the stacking of the vector offset. The risk to the system by corrupting this stacked value is very low, since it is not used by the processor or most interrupt service routine software. On CPU32X based parts which have the stack located in the FASRAM, however, the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error.

WORKAROUND:

Workarounds exist for both CPU32 and CPU32X based parts. On CPU32 based parts the first access after an IACK cycles is the stacking of the vector offset. The risk to the system by corrupting this stacked value is very low, it is not used by the processor. On CPU32X based parts which have the stack located in the FASRAM the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error. The suggested workarounds for the QSM/QSMCM/QADC64 are listed below. For CPU32 based parts: - assign the QSM/QSMCM/QADC64 it's own interrupt levels separate from any other modules if the corruption of the vector offset in the stack frame is an issue. For CPU32X based parts: (a) assign the QSM/QSMCM/QADC64 its own interrupt levels separate from any other module in the system or (b) move the stack out of the FASRAM.

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CDR_AR_754	Customer Erratum	QADC64.CDR1IMB3_02_0B
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QADC64: Do not use queue1 in external gated mode with queue2 in continuous mode.

DESCRIPTION:

When the gate for queue1 opens when queue2 is converting the last word in its queue, queue1 completion flag will immediately set and no conversions will occur. Queue1 will remain in a hung state for the duration of the gate (no conversions will occur regardless of how long the gate is open). This failure will only occur when the QADC64 is configured with queue1 in external gated mode (continuous or single scan) and queue2 is in continuous mode. The failure mode can be detected if it is known that the gate for queue 1 is shorter than the length of the queue, and the completion flag becomes set. The failure can also be detected as follows: software writes invalid results to the result register (3ff when it is known the input will never go to full scale); after the gate has closed if the invalid result is still in result space 0, then the failure has occurred.

WORKAROUND:

There are 2 workarounds: 1) Do not use queue 2 if queue1 is set for external gated mode. Or, 2) If queue2 is used and queue1 is in external gated mode, set queue2 to single scan mode.

CDR_AR_421	Customer Erratum	QADC64.CDR1IMB3_02_0B
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QADC64: Don't switch to software triggered continuous scan after completing Q1.

DESCRIPTION:

In the case when application software switches Q1 to software triggered continuous scan mode after Q1 completes a single scan where BQ2 provides the end of queue, an indeterminate response results.

WORKAROUND:

Don't select software triggered continuous scan after using Q1.

CDR_AR_422	Customer Erratum	QADC64.CDR1IMB3_02_0B
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QADC64: Do not rely on set of TOR1 in external gated continuous scan mode

DESCRIPTION:

In External Gated Continuous Scan mode: If the external gate is negated during the last conversion (after the ccw has started, but before the result is converted) the TOR1 flag will not set.

WORKAROUND:

Control software needs to reflect the following: In external gated continuous scan mode, setting of TOR1 is guaranteed only if the gate remains open thru the completion of the last conversion in queue1.

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CDR_AR_419	Customer Information	QADC64.CDR1IMB3_02_0B
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QADC64: False trigger upon configuration (Does NOT apply to ALL parts)

DESCRIPTION:

In some implementations, the QADC64 may have a false trigger upon entering an external trigger mode. The potential for a false trigger only exists on QADC64's which are implemented with trigger pin(s) muxed through PortA[3 or 4]. If the triggers have dedicated pins, then no difference exists between the value on the pin and the value between the pad and the module. The false trigger can result when an edge triggered mode is enabled and the logic value at the pin and the previously latched value in the pad are not equal.

WORKAROUND:

A port data register read may be performed prior to entering an external trigger mode to ensure that the latched value between the pad and the module matches the value on the pin. This read ensures that an edge will not be caused by the latch in the pad becoming transparent when the external trigger mode is entered. This issue does not exist on the following parts: MPC555.

CDR_AR_420	Customer Information	QADC64.CDR1IMB3_02_0B
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QADC64: Don't change BQ2 with a set of SSE2 without a mode change.

DESCRIPTION:

Changing BQ2 and setting SSE2 with no mode change will cause Q2 to begin but not recognize the change in BQ2. Further, changes of BQ2 after SSE2 is set, but before Q2 is triggered are also not recognized. All other sequences involving a change in BQ2 are recognized.

WORKAROUND:

Be sure to do mode change when changing BQ2 and setting SSE2. Recommend setting BQ2 first then setting SSE2.

CDR_AR_435	Customer Information	QADC64.CDR1IMB3_02_0B
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QADC64: TOR1 flag operates in both single and continuous external gated modes.

DESCRIPTION:

TOR1 response was added to QADC64 to provide an indication of more than 1 pass through queue1. It was described in the specification as a continuous mode only flag. The flag is however, operating in both single and continuous modes.

WORKAROUND:

None. Simply expect the flag to respond in both single scan and continuous scan modes.

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CDR_AR_563

Customer Erratum

QSMCM.CDR1IMB3_02_0

QSM/QSMCM/QADC64 corrupts data after an IACK cycle in CISC parts.

DESCRIPTION:

This problem does not affect parts that do not run IACK cycles (i.e. RISC CPUs). The Common BIU state machine, used by the QSM/QSMCM/QADC64, mis-tracks an IACK cycle if an interrupt is issued while an IACK cycle for the same level is in progress. In this case, the next access on the IMB3 will be corrupted by the QSM/QSMCM/QADC64. On CPU32 based parts (or CPU32X parts where the FASRAM is not used for the stack), the first access after an IACK cycles is the stacking of the vector offset. The risk to the system by corrupting this stacked value is very low, since it is not used by the processor or most interrupt service routine software. On CPU32X based parts which have the stack located in the FASRAM, however, the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error.

WORKAROUND:

Workarounds exist for both CPU32 and CPU32X based parts. On CPU32 based parts the first access after an IACK cycles is the stacking of the vector offset. The risk to the system by corrupting this stacked value is very low, it is not used by the processor. On CPU32X based parts which have the stack located in the FASRAM the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error. The suggested workarounds for the QSM/QSMCM/QADC64 are listed below. For CPU32 based parts: - assign the QSM/QSMCM/QADC64 it's own interrupt levels separate from any other modules if the corruption of the vector offset in the stack frame is an issue. For CPU32X based parts: (a) assign the QSM/QSMCM/QADC64 its own interrupt levels separate from any other module in the system or (b) move the stack out of the FASRAM.

CDR_AR_584

Customer Erratum

QSMCM.CDR1IMB3_02_0

QSMCM: Do not use link baud and ECK modes

DESCRIPTION:

Reads of the SCI control and status registers do not read correctly when using the link baud or the external clock source feature of the QSMCM. These modes are enabled by the SCCxR0 control register bits 0 and 1 (OTHR and LNKBD). These modes are not fully operational.

WORKAROUND:

Do not use the link baud or external clock modes of the QSMCM. The OTHR bit in the SCCxR0 control register 0 must be set = 0 to use normal mode operation only.

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CDR_AR_627	Customer Information	TPU3.CDR1IMB3_02_2
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TPU: (Microcode) Add neg_mrl with write_mer and end_of_phase

DESCRIPTION:

Wrong generation of 50% d.c. caused when we have the command combination "write_mer, end." If the write_mer is the last instruction together with the end, this may create an additional match using the old content of the match register (which is in the past now and therefore handled as an immediate match)

WORKAROUND:

Add neg_mrl together with the last write_mer and with end-of-phase. The negation of the flag overrides the false match which is enabled by write_mer and postpones the match effect by only u-instruction. In the following u-instruction the NEW MER value is already compared to the selected TCR and no false match is generated. The neg_mrl command has priority over the match event recognition. - Separating the write_mer and the end command. This gives enough time for the new MER to update before the channel transition re-enables match events.

CDR_AR_577	Customer Information	TPU3.CDR1IMB3_02_2
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TPU3 - TCR2PSCK2 bit does not give TCR2 divide ratios specified.

DESCRIPTION:

The TCR2PSCK2 bit was originally specified to cause the TCR2 timebase to be divided by 2. Actually, it causes the TCR2 timebase to be divided as follows: The /16 of external clock and /128 of internal clock are eliminated and /3, /7, /15 of the external clock and /24, /56, /120 of the internal clock are added.

WORKAROUND:

When the TCR2PSCK2 is set, instead of the specified divides of /16, /32, /64, /128, expect the internal clock source to be /8, /24, /56 and /120 for TCR2 Prescaler values of 00, 01, 10 and 11, respectively. Likewise, for the external clock source expect /1, /3, /7, /15 instead of /2, /4, /8, /16.

CDR_AR_498	Customer Erratum	UIMB.CDR1UBUSIMB3_02_0
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UIMB: Read failures occur for IMB accesses when IMB clock is half speed

DESCRIPTION:

When the imb clock is at half speed, a speed path occurs which prevents the proper data in the uimb internal data latches from being observed by the user. Data is transferred from the latches before the latches are updated with data for the current cycle. This failure occurs when the part is heated (80-100C) and the frequency is at 40Mhz.

WORKAROUND:

There are 3 possible workarounds: (1). Since the internal latches are late in being updated with imb data, it takes 2 consecutive reads from the same imb location to observe the proper data from that location. The data from the first access should be disregarded when in half speed mode. (2). When running half speed on the imb, keep the part as close to room temp. (25C) as possible. or (3). Only use full speed imb mode. This workaround only applies to RevC or later.

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CDR_AR_582

Customer Erratum

USIU.CDR1UBUS_05_0

USIU: Under certain conditions, XFC stuck at 0V on power-on

DESCRIPTION:

In some systems, the PLL does not lock on power-up. This issue occurs on some board designs, and not on others. On some boards, the not lock on startup occur if 3V VDD has a DC offset of ~150mV. This also happens when the VDDSYN ramps up much slower than the VDDL/VDDi. This can also be repeated if the XFC pin is temporarily shorted to ground. If the PLL does not lock and limp mode is disabled, the part will never negate HRESET, and CLKOUT will run at the backup clock frequency. If the PLL does not lock and limp mode is enabled, the part will exit reset clocked by the backup clock. For the sensitivities mentioned above, additional assertions of the PORESET pin will not cause the PLL to lock, only cycling the power (and avoiding the condition) will resolve the issue. Observation of the XFC pin (with a high impedance probe), can distinguish that XFC is "stuck" at 0.

WORKAROUND:

First, make sure that the PLL and reset circuitry is correct: see CDR_AR_598. If XFC is at 0V, add a circuit (VDDsyn voltage divider set at 1.1-1.3V over temp/voltage connected to small signal diode connected to XFC) to ensure XFC does not drop below ~0.8V. It has been reported that some boards may be able to avoid this issue by avoiding a DC offset on VDDL and controlling the ramp rate of VDDsyn and KAPWR. Injection into 3V only pins may result in an offset on VDDL -- refer to CDR_AR_595.

CDR_AR_595

Customer Erratum

USIU.CDR1UBUS_05_0

USIU: PLL will not lock on power-on, use limp mode and switch via software

DESCRIPTION:

In some systems, the PLL does not indicate lock on power-up. However, examination of the XFC with a high impedance, low capacitance probe indicates the VCO is at the correct frequency (20MHz XFC typically at ~1.6-1.8V). Additional assertions of the PORESET pin result in the PLL locking. This issue occurs on some board designs, and not on others. The PLL does seem to have some sensitivities related to power supplies. On some boards, the not lock on startup occur if 3V VDD has a DC offset of ~150mV. This also happens when the VDDSYN ramps up much slower than the VDDL/VDDi, or when KAPWR ramps faster. If the PLL does not lock and limp mode is disabled, the part will never negate HRESET, and CLKOUT will run at the backup clock frequency. If the PLL does not lock and limp mode is enabled, the part will exit reset clocked by the backup clock.

WORKAROUND:

Verify proper setup as noted in CDR_AR_598. To avoid system failure, always enable limp mode, allowing the system to boot using the backup clock even though lock is not yet indicated. After booting, switch from backup clock to PLL clock under software control. If EXTCLK is the clock input, use a higher frequency (15MHz or greater) and boot in 1:1 mode with limp mode enabled, or choose MODCK = 010, and overdrive the XTAL input from the oscillator output, and set EXTAL to a voltage of 0.5-0.6V. In this case, the oscillator output should be designed to meet an XTAL Vil of 300mv, with Iil= 1ma. Vih of 0.8v. To reduce fail to indicate lock, reduce the VDDL DC offset below 100mv by use of a discharge resistor. Ensure that current injected into 5V and 3V/5V pads is absorbed by circuitry attached to VDDH. While VDDL is off, avoid injecting current into 3V only pads since the PU3 circuit will cause an increase in VDDL.

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CDR_AR_610	Customer Erratum	USIU.CDR1UBUS_05_0
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Additional current on KAPWR when power is not applied

DESCRIPTION:

There is a leakage path between KAPWR and VDDi/VDDL. This results in additional KAPWR current when VDDi/VDDL is not powered. The amount of current varies, partially based upon the MODCK setting.

WORKAROUND:

Design KAPWR supply to handle additional 15ma of current, if KAPWR is powered while VDDi and VDDL are not powered. For MODCK=011, expect up to 9ma of leakage current, for MODCK=010, expect up to 7ma of leakage current.

CDR_AR_479	Customer Erratum	USIU.CDR1UBUS_05_0
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USIU: The MEMC does not support external master burst cycles

DESCRIPTION:

The MTS function will not work properly to control external devices when an external master initiates a burst.

WORKAROUND:

Use external logic to control devices which can have burst accesses from multiple masters.

CDR_AR_679	Customer Erratum	USIU.CDR1UBUS_05_0
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USIU: In slave mode, do not use write slave accesses

DESCRIPTION:

In slave mode, a write data driven by the Core might be corrupted by the data driven by the external master.

WORKAROUND:

When the device is in SLAVE mode, do not use write accesses from the external master. Alternatively, use peripheral mode if write accesses from the external master are required.

CDR_AR_389	Customer Information	USIU.CDR1UBUS_05_0
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Little Endian modes are not supported

DESCRIPTION:

The little Endian modes are not functional.

WORKAROUND:

Do not activate little endian modes.

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CDR_AR_442	Customer Information	USIU.CDR1UBUS_05_0
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Avoid loss of clock during HRESET

DESCRIPTION:

The chip may fail to switch to backup clock. This mode may occur if the input reference clock fails to toggle during hreset while switching from normal clock to backup clock. This condition may occur while switching from backup clock to normal clock (during hreset) if the PLL is not locked and there is no reference clock. In order to resume operation, the part may require the input reference clock to resume (for 1-2 more clocks) or for PORESET to be asserted.

WORKAROUND:

Avoid loss of the reference clock during hreset; ensure that the PLL is locked before switching to PLL clock. Do not enable reset upon loss of lock if limp mode is enabled, instead enable an change of lock interrupt by setting the COLIE bit (COLIR).

CDR_AR_594	Customer Information	USIU.CDR1UBUS_05_0
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USIU: Changing PLL MF to 1:1 mode can have 180 degree phase shift

DESCRIPTION:

After software changes MF from >1 to MF = 1, a 180 degree skew between EXTCLK and CLKOUT could occur.

WORKAROUND:

If synchronization between EXTCLK and CLKOUT is required, set MODCK to boot in 1:1 mode, and do not alter the MF bits to exit 1:1 mode.

CDR_AR_687	Customer Information	USIU.CDR1UBUS_05_0
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USIU: Program reserved bits in PDMCR to preserve compatibility

DESCRIPTION:

Future revisions of the PDMCR will have additional bits to control enabling and disabling of pad pull-up / pull-down resistors. Software should be written so that it is compatible with these changes. In this revision, PDMCR[8] (TPRDS) does not change the function of the TPU T2CLK pull-up resistors -- the pull-ups remain enabled.

WORKAROUND:

To ensure identical control in future revisions, when programming the PDMCR. PDMCR[8] should remain cleared. PDMCR[9:13] should be programmed to the same value as PRDS (PDMCR[6]). PDMCR[16:17] should be programmed to the same value as SPRDS (PDMCR[7]). The future function of PDMCR[14:15] has not been determined, and should be programmed to 0. For this revision, software should ignore any the read values of PDMCR[8:15].

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CDR_AR_598

Customer Information

USIU.CDR1UBUS_05_0

USIU: Ensure proper configuration for proper startup

DESCRIPTION:

In some systems, the PLL does not lock on power-up, or the system does not properly execute software out of reset. This issue occurs on some board designs, and not on others. Locking may be improved by board design and component selection, and can be resolved by paying attention to the design and setup, and ensuring that the PLL and Oscillator components are correct and as noise free as possible.

WORKAROUND:

First, make sure that the PLL and reset circuitry is correct: ensure that the PLL components are properly selected and that the PLL power (VDDSYN) is not noisy. Refer to appendix E of the users manual, "Clock and Board Guidelines". Verify that the XFC capacitor is connected to VDDSYN. Validate that the TRST_L pin is asserted upon power-up. Do not connect TRST_L to HRESET_L or SRESET_L. Validate that all power supplies are stable and all MODCK pins are at the correct levels in time for the PLL and Oscillator to be stable prior to PORESET_L rising above VIL. Verify that the proper reset configuration word is used. Validate the reset and post reset pin state for each pin controlled by the reset configuration word, and ensure there is not a conflict with an external driver. Preferably use the internal reset configuration word. If using an external reset configuration word, do not rely on the internal pull-downs to operate (refer to CDR_AR_454) and ensure that RSTCONF is asserted until SRESET is negated. After the part exits reset with the system running via the backup clock, validate the clock control registers settings and the PLL status. If the PLL is slow on locking, or the register settings indicate the MODCK pins are incorrect, address the board issues listed above. To avoid risk of system failure for no start, enable limp mode, allowing the system to boot using the backup clock even though lock is not yet indicated. After booting, switch from backup clock to PLL clock under software control after the PLL has gained lock.