Freescale Semiconductor
Advance Information

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MPC7410 RISC Microprocessor Hardware Specifications Addendum for the MPC7410RX*nnn*PC Series

This document describes part number specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7410 Hardware Specifications* (Document No. MPC7410EC).

Specifications provided in this Part Number Specification supersede those in the *MPC7410 Hardware Specifications*, for the part numbers listed in Table A only, specifications not addressed herein are unchanged. This document is frequently updated. Therefore, contact your Freescale sales office for the latest version.

Part numbers addressed in this document are listed in Table A. For more detailed ordering information see Table 17.

Freescale Part Numbers Affected:

XPC7410RX400PC

XPC7410RX450PC

XPC7410RX500PC

XPC7410RX550PC

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Table A. Part Numbers Addressed by this Data Sheet

Freescale Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	Vdd	T_J (°C)	
XPC7410RX400PC	400 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 400Mhz frequency
XPC7410RX450PC	450 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 450Mhz frequency
XPC7410RX500PC	500 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 500Mhz frequency
XPC7410RX550PC	550 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 550Mhz frequency

Notes:
The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

2 Features

There are no changes to the features of the MPC7410 described in the *MPC7410 Hardware Specifications* (MPC7410EC).

4.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7410 part numbers described herein.

Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		Vdd	2.0V±50mV	V
PLL supply voltage		AVdd	2.0V±50mV	V
L2 DLL supply voltage		L2AVdd	2.0V±50mV	V
Processor bus supply voltage	BVSEL = 1 or BVSEL = $\overline{\text{HRESET}}$	OVdd	2.5V±125mV	V
	BVSEL = GND	OVdd	1.8V±90mV	V
L2 bus supply voltage	L2VSEL = 1 or L2VSEL = $\overline{\text{HRESET}}$	L2OVdd	2.5V±125mV	V
	L2VSEL = GND	L2OVdd	1.8V±90mV	V

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit
Input voltage	Processor bus	V_{in}	GND to OVdd	V
	L2 Bus	V_{in}	GND to L2OVdd	V
	JTAG Signals	V_{in}	GND to OVdd	V
Die-junction temperature		T_j	0-65	°C

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 6 provides the power consumption for the MPC7410 part at the frequencies described herein.

Table 6. Power Consumption for MPC7410

	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	500Mhz		
Full-On Mode				
Typical	6	7	W	1, 3,
Maximum	12	14	W	1, 2, 4
Doze Mode				
Maximum	4	5	W	1, 2
Nap Mode				
Maximum	2.0	2.25	W	1, 2
Sleep Mode				
Maximum	2.0	2.25	W	1, 2
Sleep Mode—PLL and DLL Disabled				
Typical	0.5	0.5	W	1, 3

Table 6. Power Consumption for MPC7410 (continued)

	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	400Mhz	500Mhz		
Maximum	2.0	2.0	W	1, 2

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.
2. Maximum power is measured at Vdd = 2.2V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 2.15V, OVdd = L2OVdd = 2.5V in a system while running a codec application that is AltiVec intensive.
4. These values include the use of Altivec. Without Altivec operation, estimate a 25% decrease.

4.2.1 Clock AC Specifications

Table 7 provides the additional clock AC timing specifications described in this Part Number Specification. Refer to the *MPC7410 Hardware Specification* for the remaining frequencies.

Table 7. Clock AC Timing Specifications

At recommended operating conditions (See Table 3)

Characteristic	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	300	400	300	450	300	500	300	550	MHz	
VCO frequency	f_{VCO}	600	800	600	900	600	1000	600	1100	MHz	
SYSCLK frequency	f_{SYSCLK}	33	100	33	100	33	100	33	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	30	10	30	10	30	10	30	ns	
SYSCLK rise and fall time	t_{KR} & t_{KF}	—	1.0	—	1.0	—	1.0	—	1.0	ns	2
		—	0.5	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at OVdd/2	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK jitter		—	±150	—	±150	—	±150	—	±150	ps	5

Table 7. Clock AC Timing Specifications (continued)

At recommended operating conditions (See Table 3)

Characteristic	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Internal PLL relock time		—	100	—	100	—	100	—	100	µs	6

Note:
See general hardware specification.

4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 part described in this Part Number Specification.

Table 8. Processor Bus AC Timing Specifications

At Vdd=AVdd=2.0V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 2.5V±0.125V and OVdd = 1.8V±0.090V, 60X bus at 100MHz

Parameter	Symbol	400, 450, 500, 550 Mhz		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	2,3,4,5
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	2,3,5
Setup Times:				ns	10
Address/Transfer Attribute	t_{AVKH}	1.4	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSVKH}	1.4	—		—
Data/Data Parity	t_{DVKH}	1.4	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARVKH}	1.4	—		—
All Other Inputs	t_{IVKH}	1.4	—		8
Input Hold Times:				ns	11
Address/Transfer Attribute	t_{AXKH}	0	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSXKH}	0	—		—
Data/Data Parity	t_{DXKH}	0	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARXKH}	0	—		—
All Other Inputs	t_{IXKH}	0	—		8
Valid Times:				ns	12
Address/Transfer Attribute	t_{KHAV}	—	3.0		6
$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$	t_{KHTSV}	—	3.0		—
Data	t_{KHDV}	—	3.5		7
Data Parity	t_{KHDPV}	—	3.5		7
ARTRY/SHD0/SHD1	t_{KHARV}	—	2.3		—
All Other Outputs	t_{KHOV}	—	3.0		9

Table 8. Processor Bus AC Timing Specifications (continued)

At Vdd=AVdd=2.0V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 2.5V±0.125V and OVdd = 1.8V±0.090V, 60X bus at 100MHz

Parameter	Symbol	400, 450, 500, 550 Mhz		Unit	Notes
		Min	Max		
Output Hold Times:				ns	13
Address/Transfer Attribute	t_{KHAX}	0.75	—		6
$\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$	t_{KHTSX}	0.75	—		—
Data/Data Parity	t_{KHDX}	0.6	—		7
$\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$	t_{KHARX}	0.75	—		—
All Other Outputs	t_{KHOX}	0.75	—		9
SYSCLK to Output Enable	t_{KHOE}	0.5	—	ns	14
SYSCLK to Output High Impedance (all except $\overline{TS}$, $\overline{ABB}$/AMON(0), $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/DMON(0))	t_{KHOZ}	—	3.5	ns	15
SYSCLK to $\overline{TS}$, $\overline{ABB}$/AMON(0), $\overline{DBB}$/DMON(0) High Impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	4,15, 16,17
Maximum Delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ Precharge	t_{KHARP}	—	1	t_{sysclk}	4,17
SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ High Impedance After Precharge	t_{KHARPZ}	—	2	t_{sysclk}	4,17

Note:
See general hardware specification.

4.2.3 L2 Clock AC Specifications

Table 9 provides the L2CLK Output AC Timing Specifications for the MPC7410 part described in this Part Number Specification

Table 9. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	150	200	150	225	150	250	150	275	MHz	1
L2CLK cycle time	t_{L2CLK}	5	6.67	4.4	6.67	4	6.67	3.6	6.67	ns	
L2CLK duty cycle	t_{CHCL}/ t_{L2CLK}	50		50		50		50		%	2
Internal DLL-relock time		640	—	640	—	640	—	640	—	L2CLK	4

Table 9. L2CLK Output AC Timing Specifications (continued)

At recommended operating conditions (See Table 3)

Parameter	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DLL capture window			±200		±200		±200		±200	ns	5

Note:
See general hardware specification.

4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this Part Number Specification.

Table 10. L2 Bus Interface AC Timing Specifications

At Vdd=AVdd=L2AVdd= 2.05V±50mV; 0 ≤ Tj ≤ 65°C, L2OVdd = 2.5V±0.125V and L2OVdd =1.8V±0.090V

Parameter	Symbol	400 MHz		450 MHz		500 MHz		550 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} & t_{L2CF}	—	1.0	—	1.0	—	1.0	—	1.0	ns	1
Setup Times: Data and parity	t_{DVL2CH}	1.5	—	1.375	—	1.250	—	1.125	—	ns	2
Input Hold Times: Data and parity	t_{DXL2CH}	—	0.0	—	0.0	—	0.0	—	0.0	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOV}	 - - - -	 2.5 TBD TBD TBD	 - - - -	 2.375 TBD TBD TBD	 - - - -	 2.25 TBD TBD TBD	 - - - -	 2.05 TBD TBD TBD	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOX}	 0.6 TBD TBD TBD	 - - - -	 0.55 TBD TBD TBD	 - - - -	 0.5 TBD TBD TBD	 - - - -	 0.45 TBD TBD TBD	 - - - -	ns	3
L2SYNC_IN to high impedance All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOZ}	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	ns	

Note:
See general hardware specification.

9 Document Revision History

Table 16. provides a revision history for this Part Number Specification.

Table 16. Document Revision History

Revision	Date	Substantive Changes
1.1	4/19/2005	Document template update
		Document ID change from MPC7410RXPCPNS for Part Number Specification to MPC7410ECS03AD for Hardware Specification Addendum.
1	9/2002	Minor reformatting
		Section 1.10.1 - added Table 17, Part Marking Nomenclature
0		Initial Release

10 Ordering Information

10.1 Part Numbers Addressed by this Specification

Table 17 provides the ordering information for the MPC7410 part described in this document.

Table 17. Part Marking Nomenclature

MPC 7410 RX *xxx* *x* *x*

Product Code	Part Identifier	Package	Processor Frequency[1]	Application Modifier	Revision Level
XPC	7410	RX = CBGA	450 500 550	P: 2.0 V ± 50 mV 0 to 65 °C	C: 1.2; PVR = 800C 1102

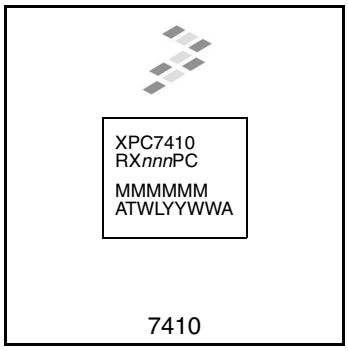
Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.

2. The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

10.3 Part Marking

Parts are marked as the example shown in Figure 26.



Notes:

nnn is the speed grade of the part

MMMMMM is the 6-digit mask number

ATWLYYWWA is the traceability code

CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

Figure 26. Freescale Part Marking for BGA Device

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How to Reach Us:

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Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

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