NX3P191

Logic controlled high-side power switch

Rev. 5 — 14 January 2014 Product data sheet

1. General description

The NX3P191 is a high-side load switch which features a low ON resistance P-channel MOSFET. It has input inrush current reduction that supports more than 500 mA of continuous current. It also has an integrated output discharge resistor to discharge the output capacitance when disabled. Designed for operation from 1.1 V to 3.6 V, it is used in power domain isolation applications to reduce power dissipation and extend battery life. The enable logic includes integrated logic level translation making the device compatible with lower voltage processors and controllers. The NX3P191 is ideal for portable, battery operated applications due to low ground current and ultra-low shutdown current.

2. Features and benefits

- Wide supply voltage range from 1.1 V to 3.6 V
- Very low ON resistance:
  - 95 mΩ (typical) at a supply voltage of 1.8 V
- High noise immunity
- Low-power mode when EN is LOW
- Low ground current (2 μA maximum)
- 1.2 V control logic at a supply voltage of 3.6 V
- High current handling capability (500 mA continuous current)
- Internal output discharge resistor
- Turn-on slew rate limiting
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - CDM AEC-Q100-011 revision B exceeds 500 V
- Specified from −40 °C to +85 °C

3. Applications

- Cell phone
- Digital cameras and audio devices
- Portable and battery-powered equipment

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX3P191UK	−40 °C to +85 °C	WLCSP4	wafer level chip-size package; 4 bumps; body 0.76 × 0.76 × 0.51 mm. (Backside Coating included)	NX3P190/NX3P191

5. Marking

Table 2. Marking codes

Type number	Marking code
NX3P191UK	x1

6. Functional diagram

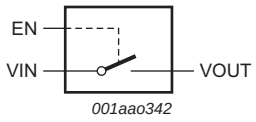


Fig 1. Logic symbol

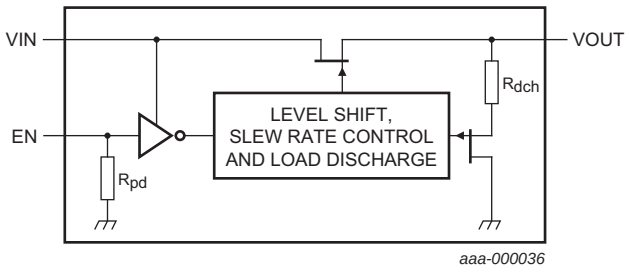


Fig 2. Logic diagram (simplified schematic)

7. Pinning information

7.1 Pinning

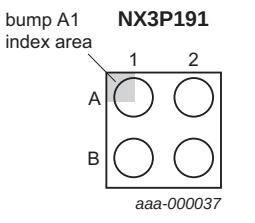


Fig 3. Pin configuration for WLCSP4

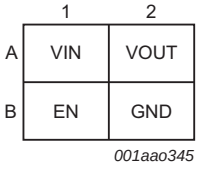


Fig 4. Ball mapping for WLCSP4

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VIN	A1	input voltage
EN	B1	enable input (active HIGH)
VOUT	A2	output voltage
GND	B2	ground (0 V)

8. Functional description

Table 4. Function table[1]

Input EN	Switch
L	switch OFF
H	switch ON

[1] H = HIGH voltage level; L = LOW voltage level.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	input EN	[1]	–0.5	+4.0	V
		input VIN	[2]	–0.5	+4.0	V
V_{SW}	switch voltage	output VOUT	[2]	–0.5	$V_{I(VIN)}$	V
I_{IK}	input clamping current	input EN: $V_{I(EN)} < -0.5$ V		–50	-	mA
I_{SK}	switch clamping current	input VIN: $V_{I(VIN)} < -0.5$ V		–50	-	mA
		output VOUT: $V_{O(VOUT)} < -0.5$ V		–50	-	mA
		output VOUT: $V_{O(VOUT)} > V_{I(VIN)} + 0.5$ V		-	50	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V				
		T_{amb} = 25 °C		-	±1000	mA
		T_{amb} = 85 °C		-	±500	mA
$T_{j(max)}$	maximum junction temperature			–40	+125	°C
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation		[3]	-	300	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 85 °C and the use of a two layer PCB.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		1.1	3.6	V
T_{amb}	ambient temperature		–40	+85	°C

11. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	130	K/W

[1] The overall Rth(j-a) can vary depending on the board layout. To minimize the effective Rth(j-a), all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] Please rely on the measurement data given for a rough estimation of the Rth(j-a) in your application. The actual Rth(j-a) value may vary in applications using different layer stacks and layouts

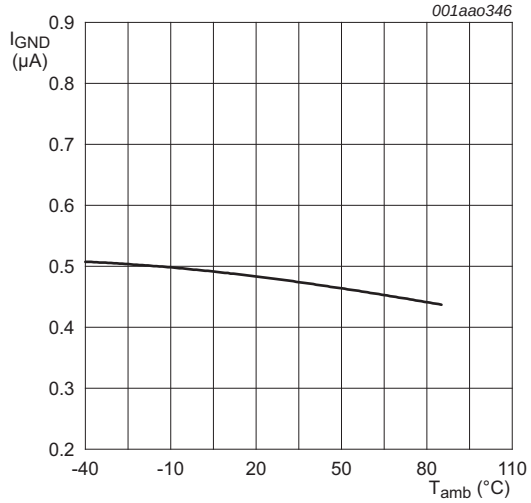
12. Static characteristics

Table 8. Static characteristics

$V_{I(VIN)} = V_{I(EN)}$, unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

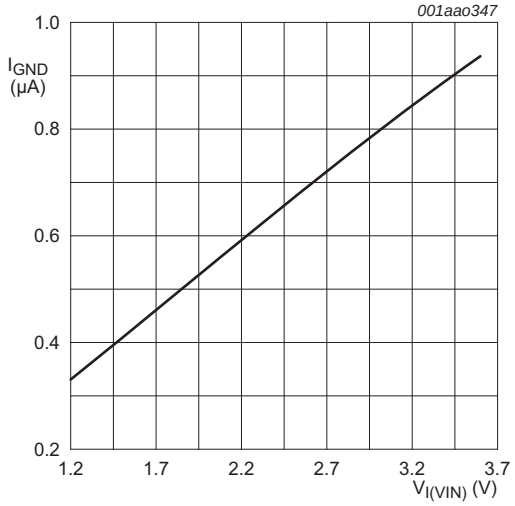
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	EN input						
		$V_{I(VIN)}$ = 1.1 V to 1.3 V	-	-	-	1.0	-	V
		$V_{I(VIN)}$ = 1.3 V to 1.8 V	-	-	-	1.2	-	V
		$V_{I(VIN)}$ = 1.8 V to 3.6 V	-	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	EN input						
		$V_{I(VIN)}$ = 1.1 V to 1.3 V	-	-	-	-	0.3	V
		$V_{I(VIN)}$ = 1.3 V to 1.8 V	-	-	-	-	0.4	V
		$V_{I(VIN)}$ = 1.8 V to 3.6 V	-	-	-	-	0.45	V
R_{pd}	pull-down resistance	EN input	-	4	-	-	-	MΩ
I_{GND}	ground current	$V_{I(VIN)}$ = 3.6 V; VOUT open; see Figure 5 and Figure 6	-	-	-	–2	-	µA
$I_{S(OFF)}$	OFF-state leakage current	$V_{I(VIN)}$ = 3.6 V; $V_{I(EN)}$ = GND; $V_{O(VOUT)}$ = GND; see Figure 8	-	0.1	-	-	2	µA
R_{dch}	discharge resistance	VOUT output	-	280	-	-	-	Ω

12.1 Graphs



$V_{I(VIN)}$ = 1.8 V; $V_{I(EN)}$ = 1.8 V; I_{LOAD} = 500 mA.

Fig 5. Waveform showing the ground current versus temperature



$V_{I(EN)}$ = $V_{I(VIN)}$; T_{amb} = 25 °C; I_{LOAD} = 500 mA.

Fig 6. Waveform showing the ground current versus input voltage on pin VIN

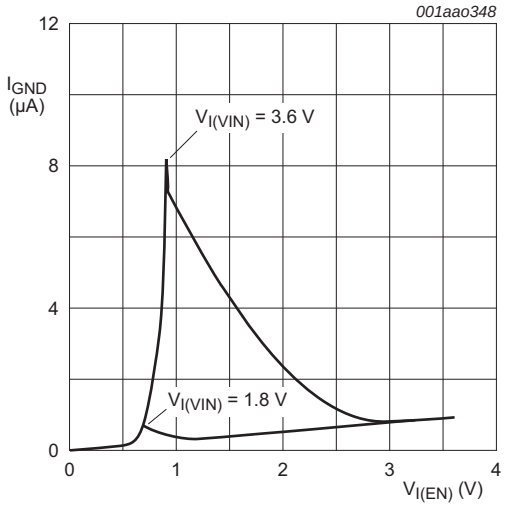
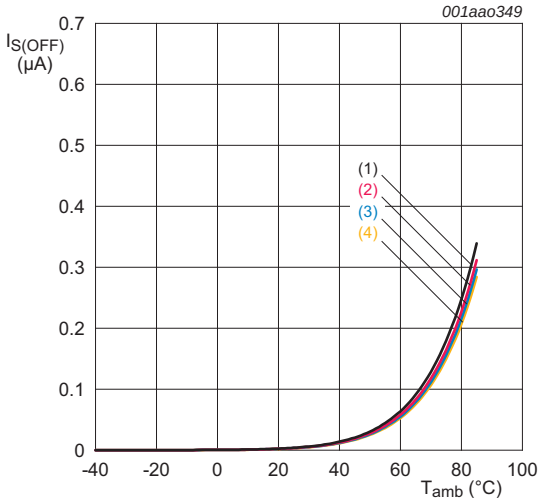


Fig 7. Waveform showing the additional ground current versus input voltage



$V_{I(EN)}$ = GND.

(1) $V_{I(VIN)}$ = 3.6 V.

(2) $V_{I(VIN)}$ = 2.5 V.

(3) $V_{I(VIN)}$ = 1.8 V.

(4) $V_{I(VIN)}$ = 1.2 V.

Fig 8. Waveforms showing the OFF-state leakage current versus temperature

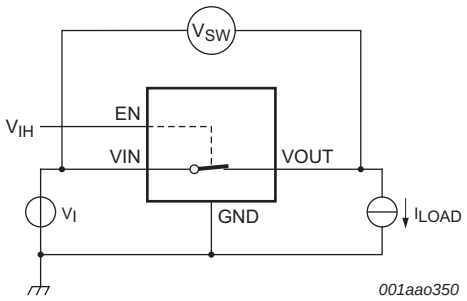
12.2 ON resistance

Table 9. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

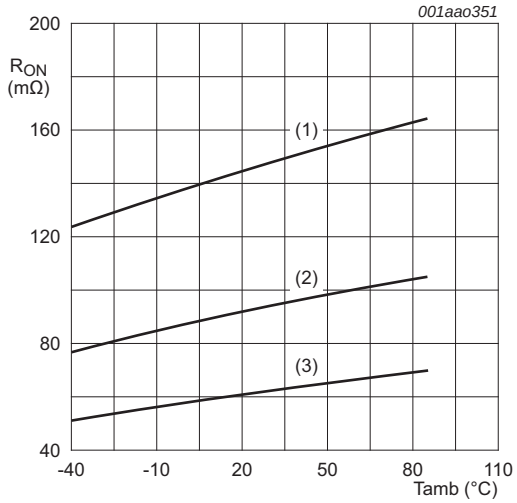
Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
R_{ON}	ON resistance	$V_{I(EN)}$ = 1.5 V; I_{LOAD} = 200 mA; see Figure 9, Figure 10 and Figure 11				
		$V_{I(VIN)}$ = 1.2 V	-	150	-	mΩ
		$V_{I(VIN)}$ = 1.5 V	-	110	-	mΩ
		$V_{I(VIN)}$ = 1.8 V	-	95	130	mΩ
		$V_{I(VIN)}$ = 2.5 V	-	75	-	mΩ
		$V_{I(VIN)}$ = 3.6 V	-	65	-	mΩ

12.3 ON resistance test circuit and waveforms



$R_{ON} = V_{SW} / I_{LOAD}$.

Fig 9. Test circuit for measuring ON resistance



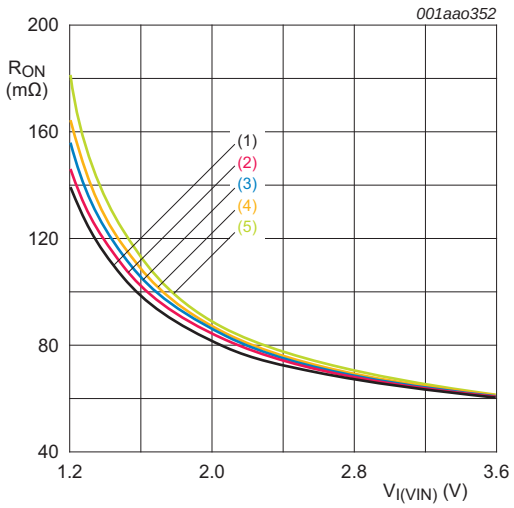
I_{LOAD} = 100 mA.

(1) $V_{I(VIN)}$ = 1.2 V.

(2) $V_{I(VIN)}$ = 1.8 V.

(3) $V_{I(VIN)}$ = 3.6 V.

Fig 10. Waveform showing the ON resistance versus temperature



$V_{I(EN)} = V_{I(VIN)}$; T_{amb} = 25 °C.

(1) I_{LOAD} = 10 mA.

(2) I_{LOAD} = 100 mA.

(3) I_{LOAD} = 250 mA.

(4) I_{LOAD} = 350 mA.

(5) I_{LOAD} = 500 mA.

Fig 11. Waveform showing the ON resistance versus input voltage

13. Dynamic characteristics

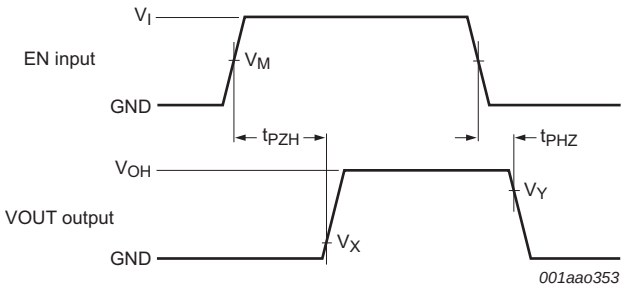
Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			Unit
				Min	Typ	Max	
t_{en}	enable time	EN to VOUT; see Figure 12	[1]				
		$V_{I(VIN)}$ = 1.8 V		-	80	-	µs
		$V_{I(VIN)}$ = 3.6 V		-	40	-	µs

[1] t_{en} is the same as t_{PZH}.

13.1 Waveform and test circuits



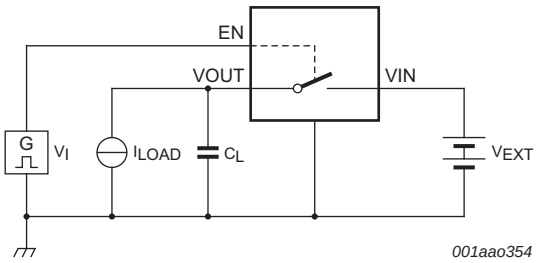
Measurement points are given in Table 11.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 12. Switching times

Table 11. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VIN)}$	V_M	V_X	V_Y
1.1 V to 3.6 V	0.5 × $V_{I(EN)}$	0.1 × V_{OH}	0.9 × V_{OH}



Test data is given in Table 12.

Definitions test circuit:

R_L = Load resistance.

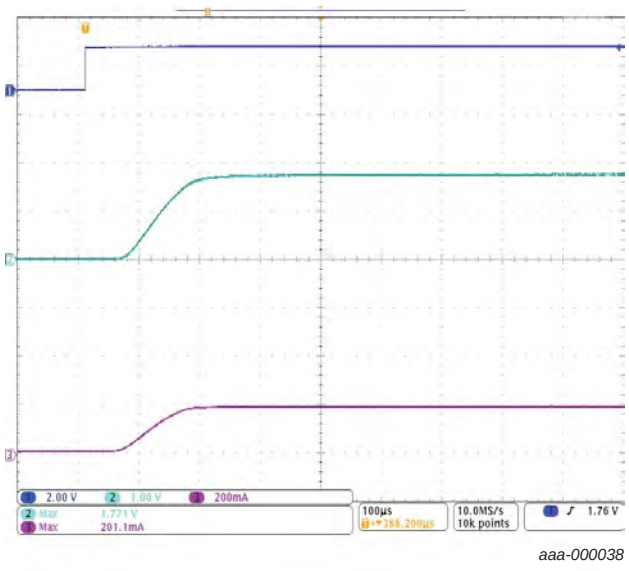
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

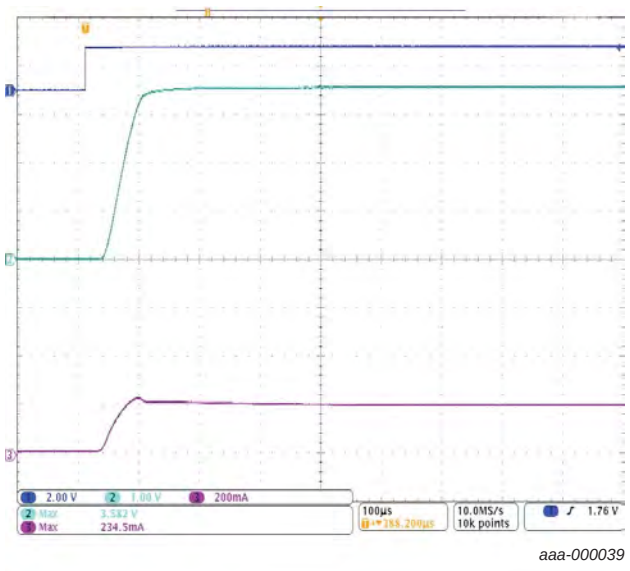
Table 12. Test data

Supply voltage	Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	I_{LOAD}
1.1 V to 3.6 V	1.5 V	1 μF	200 mA



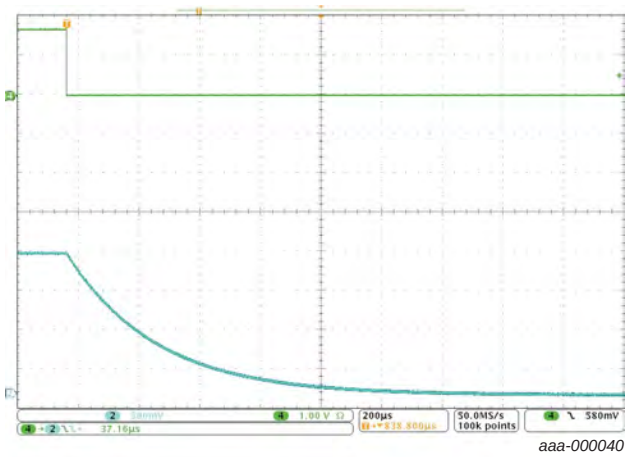
$V_{I(VIN)}$ = 1.8 V; $V_{I(EN)}$ = 1.8 V; C_L = 1 μF; I_{LOAD} = 200 mA.

Fig 14. Waveform showing the enable time versus inrush current



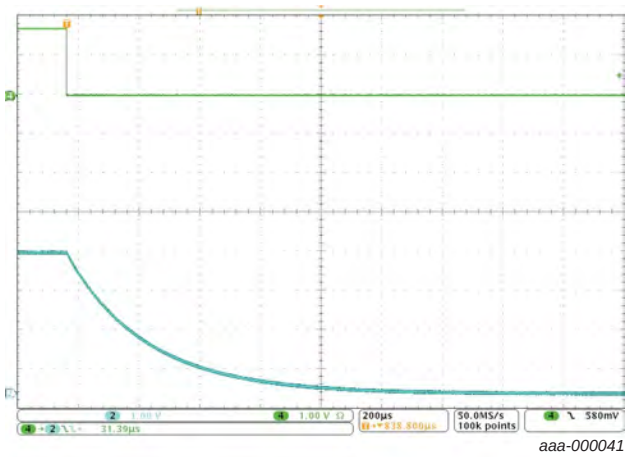
$V_{I(VIN)}$ = 3.6 V; $V_{I(EN)}$ = 1.8 V; C_L = 1.0 μF; I_{LOAD} = 200 mA.

Fig 15. Waveform showing the enable time versus inrush current



$V_{I(VIN)}$ = 1.8 V; $V_{I(EN)}$ = 1.8 V.

Fig 16. Waveform showing the disable time

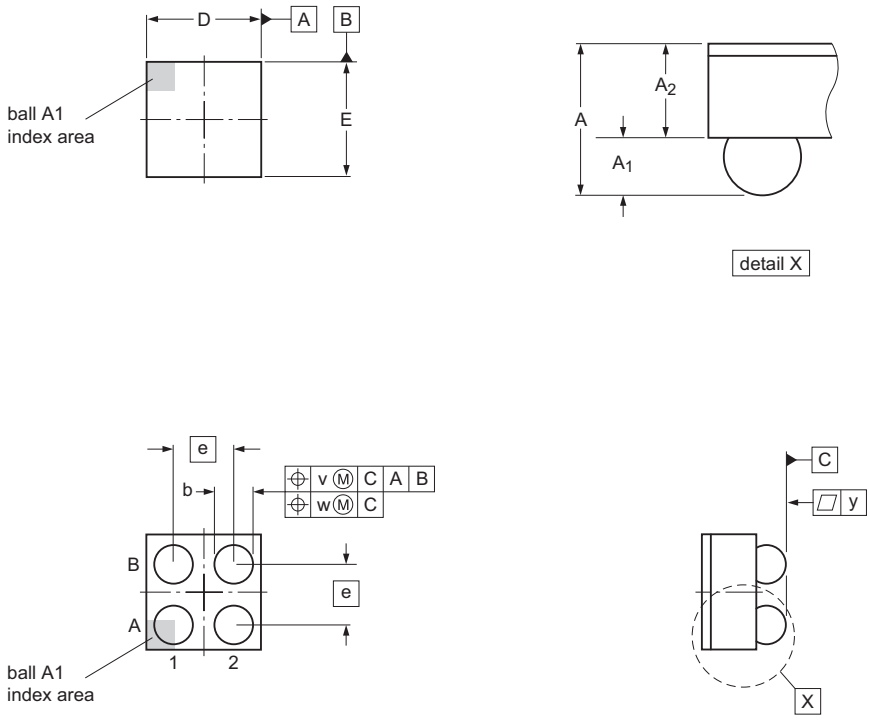


$V_{I(VIN)}$ = 3.6 V; $V_{I(EN)}$ = 3.6 V.

Fig 17. Waveform showing the disable time

14. Package outline

WLCSP4: wafer level chip-size package.
4 bumps; body 0.76 x 0.76 x 0.51 mm. (Backside Coating included) **NX3P190/NX3P191**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	v	w	y
	max	0.54	0.22	0.32	0.29	0.81	0.81				
mm	nom	0.51	0.20	0.31	0.26	0.76	0.76	0.40	0.025	0.025	0.03
	min	0.48	0.18	0.30	0.23	0.71	0.71				

nx3p190_191_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NX3P190/NX3P191						~~11-05-24~~ 11-06-09

Fig 18. Package outline WLCSP4 (NX3P190/NX3P191)

15. Abbreviations

Table 13. Abbreviations

Acronym	Description
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor

16. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3P191 v.5	20140114	Product data sheet	-	NX3P191 v.4
Modifications:	• Figure title row figure 7 corrected (errata).			
NX3P191 v.4	20121022	Product data sheet	-	NX3P191 v.3
NX3P191 v.3	20120903	Product data sheet	-	NX3P191 v.2
NX3P191 v.2	20111104	Product data sheet	-	NX3P191 v.1
NX3P191 v.1	20110831	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

19. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 January 2014
Document identifier: NX3P191