P3A1604UK

4-bit dual supply translating transceiver; auto direction sensing

Rev. 1.0 — 10 December 2024 Product data sheet

1 General description

The P3A1604UK is a 4-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features four 1-bit input-output ports (A and B), one output enable input (OE), and two supply pins (V_{CCA} and V_{CCB}). V_{CCA} can be supplied at any voltage between 0.72 V and 1.98 V. V_{CCB} can be supplied at any voltage between 1.62 V and 3.63 V. This flexibility makes the device suitable for translating between any of the voltage nodes (0.8 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V). Pins A and OE are referenced to V_{CCA} and pin B is referenced to V_{CCB}. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state.

2 Features and benefits

- Auto direction sensing and bidirectional voltage level translation
- Wide supply voltage range:
  - V_{CCA}: 0.72 V to 1.98 V and V_{CCB}: 1.62 V to 3.63 V
- No power-sequencing required
- Maximum data rate (DDR) per bit
  - Open-drain: 6.8 Mbit/s (3.4 MHz)
  - Push-pull: 40 Mbit/s (20 MHz)
- Support I3C/I2C/SMBus/SPI/UART interfaces
- Longer one-shot pulse for driving larger capacitive loads with much reduced ringing and overshoot
- A-side and OE inputs accept voltages up to 1.98 V
- B-side inputs accept voltages up to 3.63 V
- Electrostatic discharge (ESD) protection:
  - Human body model (HBM) JESD22-A114E Class 2 exceeds 2000 V
  - Charged device model (CDM) JESD22-C101E exceeds 500 V
- I/O latch-up current 100 mA, JESD 78
- Package:
  - WLCSP12 (1.405 mm x 1.055 mm, 0.35 mm pitch)
- Specified from -40 °C to +125 °C

3 Applications

- Mobile
- I3C/I^2C/SMBus
- SPI
- Server

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
P3A1604UK	4U[1]	WLCSP12	wafer level chip scale package; 12 balls with 0.35 mm pitch; 1.405 mm x 1.055 mm	SOT2063-4

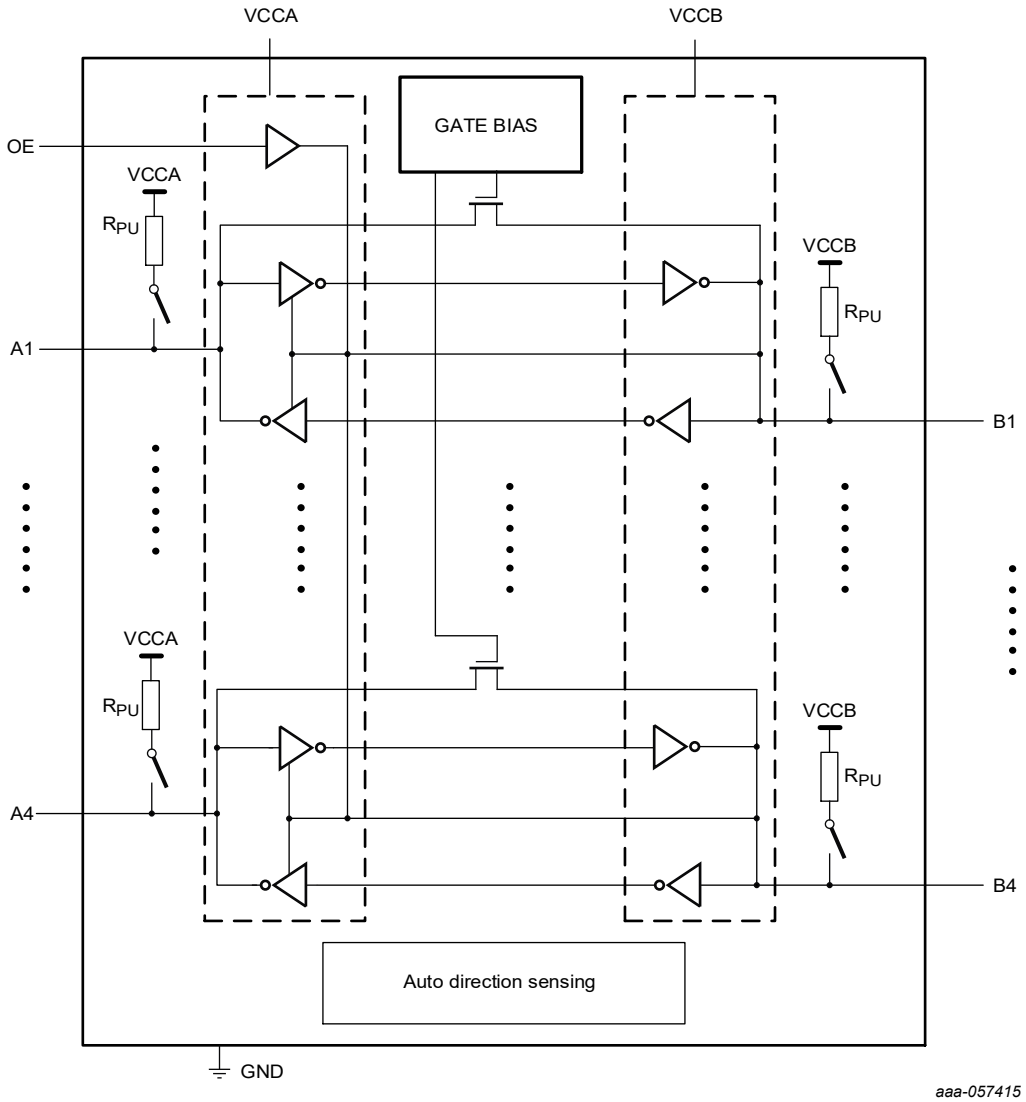
[1] "X4" for engineering sample and "4U" for production

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3A1604UK	P3A1604UKAZ	WLCSP12	reel 7" q1/t1 *special mark chips dp	4400	T_{amb} = -40 °C to +125 °C

5 Block diagram

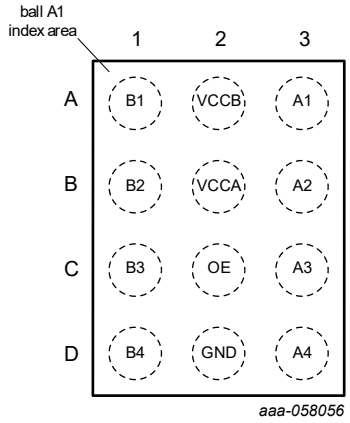


The R_{PU} = 10 kΩ. When OE = LOW, the R_{PU} is disabled.

Figure 1. Block diagram

6 Pinning information

6.1 Pinning



Transparent top view, terminal side down

Figure 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B1	A1	data input or output (referenced to V_{CCB})
V_{CCB}	A2	supply voltage B
A1	A3	data input or output (referenced to V_{CCA})
B2	B1	data input or output (referenced to V_{CCB})
V_{CCA}	B2	supply voltage A
A2	B3	data input or output (referenced to V_{CCA})
B3	C1	data input or output (referenced to V_{CCB})
OE	C2	output enable input (active High). Referenced to V_{CCA}
A3	C3	data input or output (referenced to V_{CCA})
B4	D1	data input or output (referenced to V_{CCB})
GND	D2	Ground
A4	D3	data input or output (referenced to V_{CCA})

7 Functional description

7.1 Architecture

The architecture of the device does not require an extra input signal to control the direction of data flow from A to B or B to A.

The P3A1604UK is a "switch" type voltage translator using two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate one-shot accelerator that detects and accelerates rising and falling edges on the I/O pins.

Table 4 describes the function for different OE and I/O states.

Table 4. Function table

Supply voltage		Input[1]	Input/output[1]	
V_{CCA}	V_{CCB}	OE	A	B
0.72 V to 1.98 V and $V_{CCA} \leq V_{CCB}$	1.62 V to 3.63 V	L	Z	Z
0.72 V to 1.98 V and $V_{CCA} \leq V_{CCB}$	1.62 V to 3.63 V	H	input or output	output or input
GND[2]	GND[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.
[2] When either V_{CCA} or V_{CCB} is at GND level, the device goes into Power-down mode.

7.2 Input driver requirements

As the P3A1604UK is a switch-type translator, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time (t_{THL}), and propagation delay (t_{PHL}), are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with an output impedance below 50 Ω is used.

7.3 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. The P3A1604UK has a longer one-shot pulse for driving larger capacitive loads.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on P3A1604UK PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 10 ns min to 30 ns max). It ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

If required, a series resistor on the signal path is recommended. See Section 8.1 for more detail description.

7.4 Power up

During operation, V_{CCA} must never be higher than V_{CCB}. However, during power up, $V_{CCA} \geq V_{CCB}$ does not damage the device, so either power supply can be ramped up first.

It requires 50 µs max after V_{CCB} reached regulating voltage and 4 µs max after V_{CCA} reached regulating voltage for the internal circuit setup correctly.

There is no special power up sequencing required. The P3A1604UK includes circuitry that disables all output ports when either V_{CCA} or V_{CCB} is switched off.

7.5 Enable and disable

An output enable input (OE) is used to enable/disable the device. The OE is referenced to V_{CCA}. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load)

indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (ten) indicates the amount of time the user must allow for one-shot circuitry to become operational after OE is taken HIGH. Before the ten (3 µs max), the I/O status should be ignored.

To ensure the high-impedance OFF-state during power up or power down, pin OE should be tied to GND through a pulldown resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

7.6 Pullup or pulldown resistors on I/O lines

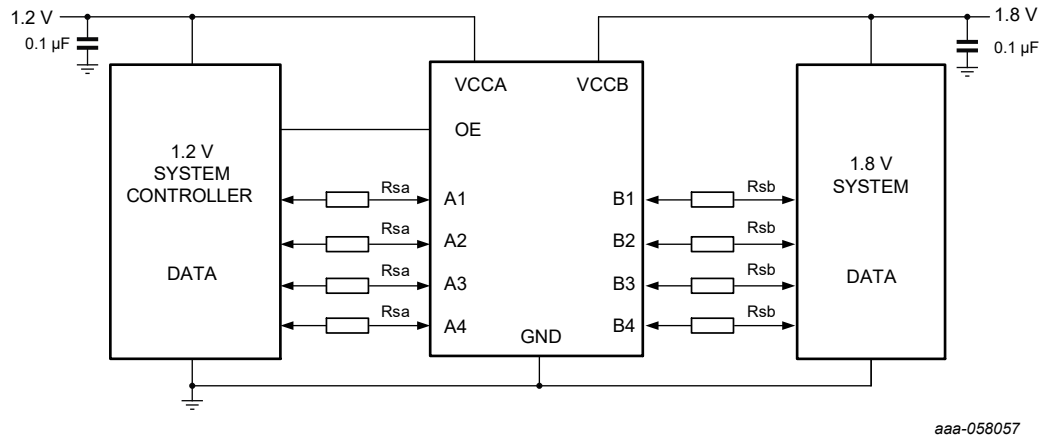
The A port I/O has an internal 10 kΩ pullup resistor to V_{CCA}. The B port I/O has an internal 10 kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, add an external resistor in parallel to the internal 10 kΩ. This pullup resistor affects the VOL level. When OE goes LOW, the internal pullups of the P3A1604UK are disabled. For Open Drain signal, at least one side pullup R on either A side or B side I/O pin is required. The pulldown resistor is not recommended to avoid incorrect I/O logic level.

8 Application information

8.1 Applications

P3A1604UK can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device can support both open-drain and push-pull interfaces like I3C/I2C/SMBus/SPI/UART. See Figure 3 for the typical application circuit.

If the PCB trace length is too long (> 30 cm) or the parasitic impedance is too large, the I/O signal may have overshoot/undershoot or oscillation. A series resistor Rs on each I/O pin is recommended to reduce the overshoot/undershoot and avoid the oscillation. The recommended value is 30 Ω. Adjust the Rs value for optimized signal integrity is required based on with different wire lengths and PCB parasitic R/L/C. Ensure the Rs should not be too high to affect the VOL level.



V_{CCA} range: 0.72 V to 1.98 V, V_{CCB} range: 1.62 V to 3.63 V.

Rsa and Rsb (~ 30 Ω) are optional based on the signal integrity.

For open-drain signal, at least one side pullup R on either A side or B side I/O pin is required.

Figure 3. Typical application circuit

8.2 Architecture

Figure 4 describes the architecture of P3A1604UK design for both push-pull and open drain mode. The architecture uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high), N-channel Pass gate transistor and a pullup resistor (to provide DC-bias and drive capabilities) to meet these requirements. The design is directionless and does not need a direction control signal. The implementation supports both low-speed open-drain operation as well as high-speed push-pull operation. The N-channel Pass device T5 will be on only during the Low input cycle and will be off during the High input cycle.

When transmitting data from A-ports, during a rising edge and A port voltage = V_{IH}, both PMOS transistor T1 and T2 are turned on by OS1 (one-shot) and OS2 (one-shot) for a short duration respectively to reduce the low to high transition time. The T1 duration is around 10 ns. The T2 duration is around 10 ns min to 30 ns max, which depends on the CLB (load capacitance on the B side). Similarly, during a falling edge, when transmitting data from A to B and voltage = V_{IL}, both OS3 and OS4 one-shots turn on the N-channel transistor T3 and T4 for a short duration, which speeds up the high to low transition.

When transmitting data from B-ports, during a rising edge and B port voltage = V_{IH}, both PMOS transistor T1 and T2 are turned on by OS1 (one-shot) and OS2 (one-shot) for a short duration respectively to reduce the low to high transition time. The T2 duration is around 10 ns. The T1 duration is around 10 ns min to 30 ns max, which depends on the CLA (load capacitance on the A side). Similarly, during a falling edge, when transmitting data from B to A and voltage = V_{IL}, both OS3 and OS4 one-shots turn on the N-channel transistor T3 and T4 for a short duration, which speeds up the high to low transition.

The internal pullup resistor RupA and RupB are typical value of 10 k and are controlled by switches S1 and S2 respectively. Switches S1 and S2 are controlled by their respective input signal and OE.

- Pullup resistors are connected only when the switches are closed.
  - The switches are closed only when the input signal is High and OE enabled.
- Pullup resistors are disconnected when the switches are open. Any one of the conditions have the switch open:
  - the respective input signal is low.
  - the OE input signal is low.

For push-pull application, the external pullup resistors are not required since at least one side is driven with a clear High or Low state.

For open-drain application, at least one external pullup resistor is required for pulling signal A from low state to high state. The external pullup resistor can be either on A side or B side. The rising time can be estimated with Rup_ext x (CLA + CLB) + one-shot time (~10 ns). Where the Rup_ext is an external pullup resistor, CLA is the total load capacitance on the A side. CLB is the total load capacitance on the B side.

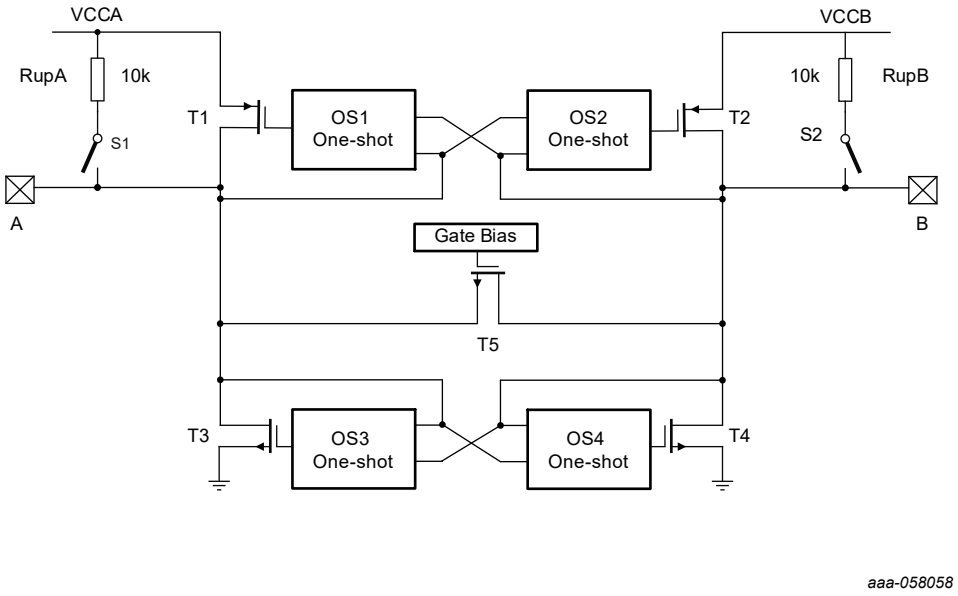


Figure 4. Architecture of P3A1604UK (one channel)

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	supply voltage A	$V_{CCA} \leq V_{CCB}$	[1]	-0.5	+2.5	V
V_{CCB}	supply voltage B		[1]	-0.5	+4.2	V
V_I	input voltage	A port and OE input		-0.5	+2.5	V
		B port		-0.5	+4.2	V
V_O	output voltage	Active mode				
		A or B port	[2] [3]	-0.5	V_{CCO} + 0.5	V
		Power-down or 3-state mode				
		A port		-0.5	+2.5	V
		B port		-0.5	+4.2	V
T_{stg}	storage temperature			-65	+150	°C

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] V_{CCO} + 0.5 V should not exceed the associated V_{CCO} maximum limiting value.

10 Thermal characteristics

Table 6. Thermal resistance information[1][2]

Symbol	Parameter	Value (type)	Unit
RθJA	Junction to ambient	77.9	°C/W
ψJT	Junction to top characterization	9.3	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal test board meets JEDEC specification for this package (JESD51-9).

11 Recommended operating conditions

Table 7. Recommended operating conditions[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	supply voltage A	$V_{CCA} \leq V_{CCB}$ & 1.98 V	[2]	0.72	1.98	V
V_{CCB}	supply voltage B			1.62	3.63	V
VI_EN	OE input voltage			-0.3	V_{CCA}+0.3	V
T_{amb}	ambient temperature			-40	+125	°C
T_J	junction temperature		[3]	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	A or B port; push-pull driving				
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V	[2]	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] V_{CCA} must be less than or equal to V_{CCB} and 1.98 V.
[3] The TJ limits shall be supported by proper thermal PCB design taking the power consumption and the thermal resistance into account.

12 Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	A port					
		V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 1.62 V to 3.63 V		V_{CCA} – 0.2			V
		V_{CCA} = 0.9 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V; & $V_{CCA} \leq V_{CCB}$		0.65 x V_{CCA}			V
		B port					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V; & $V_{CCA} \leq V_{CCB}$		0.65 x V_{CCB}			V
		OE input					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V; & $V_{CCA} \leq V_{CCB}$		0.65 x V_{CCA}			V
V_{IL}	LOW-level input voltage	A or B port					
		V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 1.62 V to 3.63 V;	[1]	-		0.25 x V_{CCA}	V
		V_{CCA} = 0.9 V to 1.98 V;	[1]	-		0.35 x V_{CCA}	V

Table 8. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{CCB} = 1.62 V to 3.63 V; & $V_{CCA} \leq V_{CCB}$					
		OE input					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V; & $V_{CCA} \leq V_{CCB}$		-		0.35 x V_{CCA}	V
V_{OHA}	HIGH-level output voltage	I_O = -10 µA					
		V_{CCB} = 1.62 V to 3.63 V; $V_I \geq 0.65 \times V_{CCB}$	[2]				
		V_{CCA} = 0.72 V to 0.9 V	[2]	0.70 x V_{CCA}		-	V
		V_{CCA} = 0.9 V to 1.98 V; & $V_{CCA} \leq V_{CCB}$	[2]	0.75 x V_{CCA}		-	V
V_{OHB}	HIGH-level output voltage	I_O = -10 µA					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V; $V_I \geq 0.65 \times V_{CCA}$	[2]	0.75 x V_{CCB}		-	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 1 mA	[2] [3]				
		V_I = 0.15 V; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V		-		0.30	V
I_I	input leakage current	OE; OE = 0 V or V_{CCA}; V_I = 0 V or V_{CCI}; V_{CCA}= 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V		-		1	µA
I_{OZ}	OFF-state output current	A or B port, OE = 0 V; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V	[2]	-		2	µA
		V_{CCA} = 0 V or V_{CCB} = 0 V				3	µA
I_{CC}	supply current	OE = V_{CCA}, V_I = 0 V or V_{CCI}; I_O = 0 A	[4]				
		ICCA					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V		-		5	µA
		V_{CCA} = 1.98 V; V_{CCB} = 0 V		-		5	µA
		V_{CCA} = 0 V; V_{CCB} = 3.63 V		-		-5	µA
		ICCB					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V		-		15	µA
		V_{CCA} = 1.98 V; V_{CCB} = 0 V		-		-15	µA
		V_{CCA} = 0 V; V_{CCB} = 3.63 V		-		15	µA

Table 8. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		ICCA + ICCB					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 1.62 V to 3.63 V		-		20	µA
C_I	input capacitance	OE input; V_{CCA} = 1.2 V; V_{CCB} = 3.3 V		-	2	-	pF
C_{IO}	input/output capacitance	A port	[5]	-	7	-	pF
		B port	[5]	-	5.5	-	pF

[1] V_{IL} of A and B port is the value with respect to V_{CCA}.
[2] V_{CCO} is the supply voltage associated with the output.
[3] This spec has more margin. The Ron (resistance between input and output at low stage) max = 50 Ω. The equation for VOL is VOL= Vi + Io * Ron.
[4] V_{CCI} is the supply voltage associated with the input
[5] The C_{IO} is defined when A port and B port are isolated.

13 Dynamic characteristics

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for waveform see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		V_{CCB}				Unit
				1.8 V ± 10 %		3.3 V ± 10 %		
				Min	Max	Min	Max	
V_{CCA} = 0.8 V ± 10 %								
t_{PHL}	HIGH to LOW propagation delay	A to B			6		5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B			8		7	ns
t_{PHL}	HIGH to LOW propagation delay	B to A			5		4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A			2		2	ns
ten	enable time	OE to A; B			3		3	µs
t_{dis}	disable time	OE to A; no external load	[2]		0.4		0.4	µs
		OE to B; no external load	[2]		0.4		0.4	µs
		OE to A			0.8		0.8	µs
		OE to B			0.7		0.7	µs

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for waveform see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		V_{CCB}				Unit
				1.8 V ± 10 %		3.3 V ± 10 %		
				Min	Max	Min	Max	
t_{TLH}	LOW to HIGH output transition time	A port			3		3	ns
		B port			9		3	ns
t_{THL}	HIGH to LOW output transition time	A port			3		3	ns
		B port			3		3	ns
$t_{sk(o)}$	output skew time	between channels			0.3		0.3	ns
t_W	pulse width	data inputs		25		25		ns
f_{data}	data rate	DDR	[3] [4]	0.128	40	0.128	40	Mbit/s
V_{CCA} = 1.2 V ± 10 %								
t_{PHL}	HIGH to LOW propagation delay	A to B			5		5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B			5		5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A			5		4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A			2		2	ns
ten	enable time	OE to A; B			3		3	µs
t_{dis}	disable time	OE to A; no external load	[2]		0.4		0.4	µs
		OE to B; no external load	[2]		0.4		0.4	µs
		OE to A			0.8		0.8	µs
		OE to B			0.7		0.7	µs
t_{TLH}	LOW to HIGH output transition time	A port			6		4	ns
		B port			6		3	ns
t_{THL}	HIGH to LOW output transition time	A port			3		3	ns
		B port			3		3	ns
$t_{sk(o)}$	output skew time	between channels			0.3		0.3	ns
t_W	pulse width	data inputs		25		25		ns

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for waveform see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		V_{CCB}				Unit
				1.8 V ± 10 %		3.3 V ± 10 %		
				Min	Max	Min	Max	
f_{data}	data rate	DDR	[3] [4]	0.128	40	0.128	40	Mbit/s
V_{CCA} = 1.8 V ± 10 %								
t_{PHL}	HIGH to LOW propagation delay	A to B			5		5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B			5		5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A			5		4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A			3		3	ns
ten	enable time	OE to A; B			3		3	µs
t_{dis}	disable time	OE to A; no external load	[2]		0.4		0.4	µs
		OE to B; no external load	[2]		0.4		0.4	µs
		OE to A			0.8		0.8	µs
		OE to B			0.7		0.7	µs
t_{TLH}	LOW to HIGH output transition time	A port			6		4	ns
		B port			6		3	ns
t_{THL}	HIGH to LOW output transition time	A port			3		3	ns
		B port			3		3	ns
$t_{sk(o)}$	output skew time				0.3		0.3	ns
t_W	pulse width	data inputs		25		25		ns
f_{data}	data rate	DDR	[3] [4]	0.128	40	0.128	40	Mbit/s

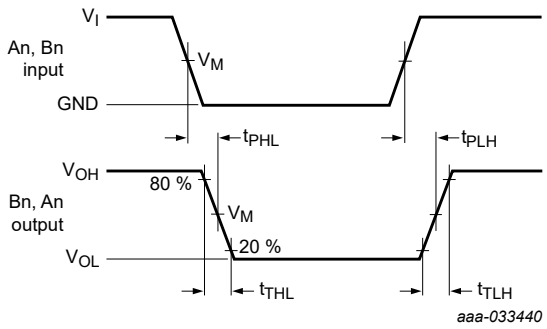
[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}

[2] Delay between OE going LOW and when the outputs are disabled.

[3] Assuming CL (load capacitance) ≤ 50 pF and equal time for 1 and 0 bit information. The one-shot accelerator duration (30 ns max) is proportional to CL and determined by the internal circuit.

[4] The spec is DDR (Double Data Rate) per bit. The 40 Mbit/s equivalents to 20 MHz.

14 Waveforms

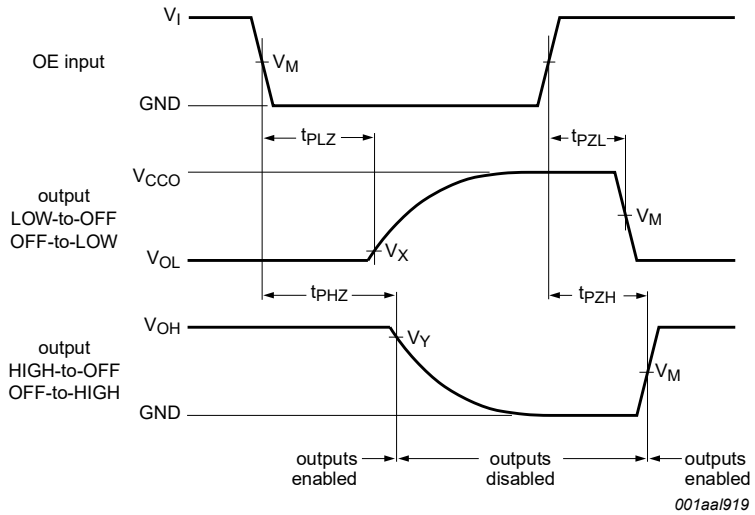


Measurement points are given in Table 10.

VOL and VOH are typical output voltage levels that occur with the output load.

The data input (A, B) to data output (B, A) propagation delay times

Figure 5. The data input (A, B) to data output (B, A) propagation delay times



Measurement points are given in Table 10. VOL and VOH are typical output voltage levels that occur with the output load.

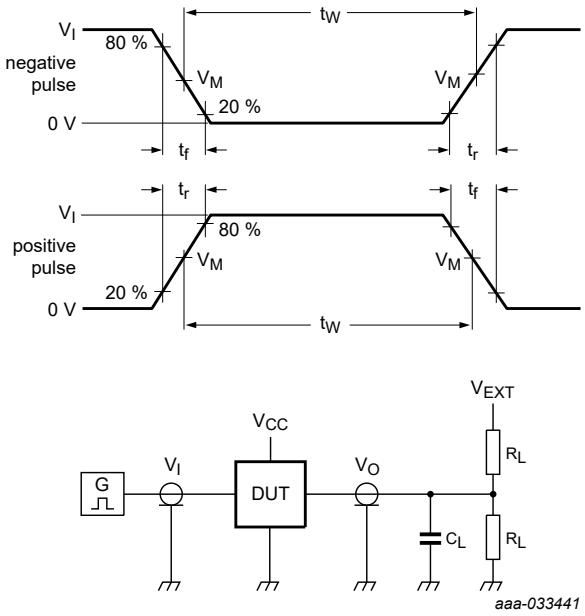
Figure 6. Enable and disable times

Table 10. Measurement points

V_{CCI} is the supply voltage associated with the input and VCCO is the supply voltage associated with the output.

Supply Voltage	Input[1]	Output[2]		
V_{CCO}	**V_M**	**V_M**	**V_X**	**V_Y**
0.8 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.08 V	VOH - 0.08 V
1.2 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.12 V	VOH - 0.12 V
1.8 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.18 V	VOH - 0.18 V
3.3 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.3 V	VOH - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 11

All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz; ZO = 50 Ω; dV/dt ≥ 1.0 V/ns.

RL = Load resistance.

CL = Load capacitance including jig and probe capacitance.

VEXT = External voltage for measuring switching times.

Figure 7. Test circuit for measuring switching times

Table 11. Test data

Supply Voltage		Input		Load		V_{EXT}		
V_{CCA}	V_{CCB}	V_I [1]	Δt/ΔV	CL[2]	RL[3]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[4]
0.72 V to 1.98 V; & ≤ V_{CCB}	1.62 V to 3.63 V	V_{CCI}	≤ 1.0 ns/V	50 pF	50 kΩ , 1 MΩ	open	open	2 V_{CCO}

[1] V_{CCI} is the supply voltage associated with the input.
[2] For I3C maximum CL.
[3] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, RL = 1 MΩ; for measuring enable and disable times, RL =50 kΩ.
[4] V_{CCO} is the supply voltage associated with the output.

15 Package outline

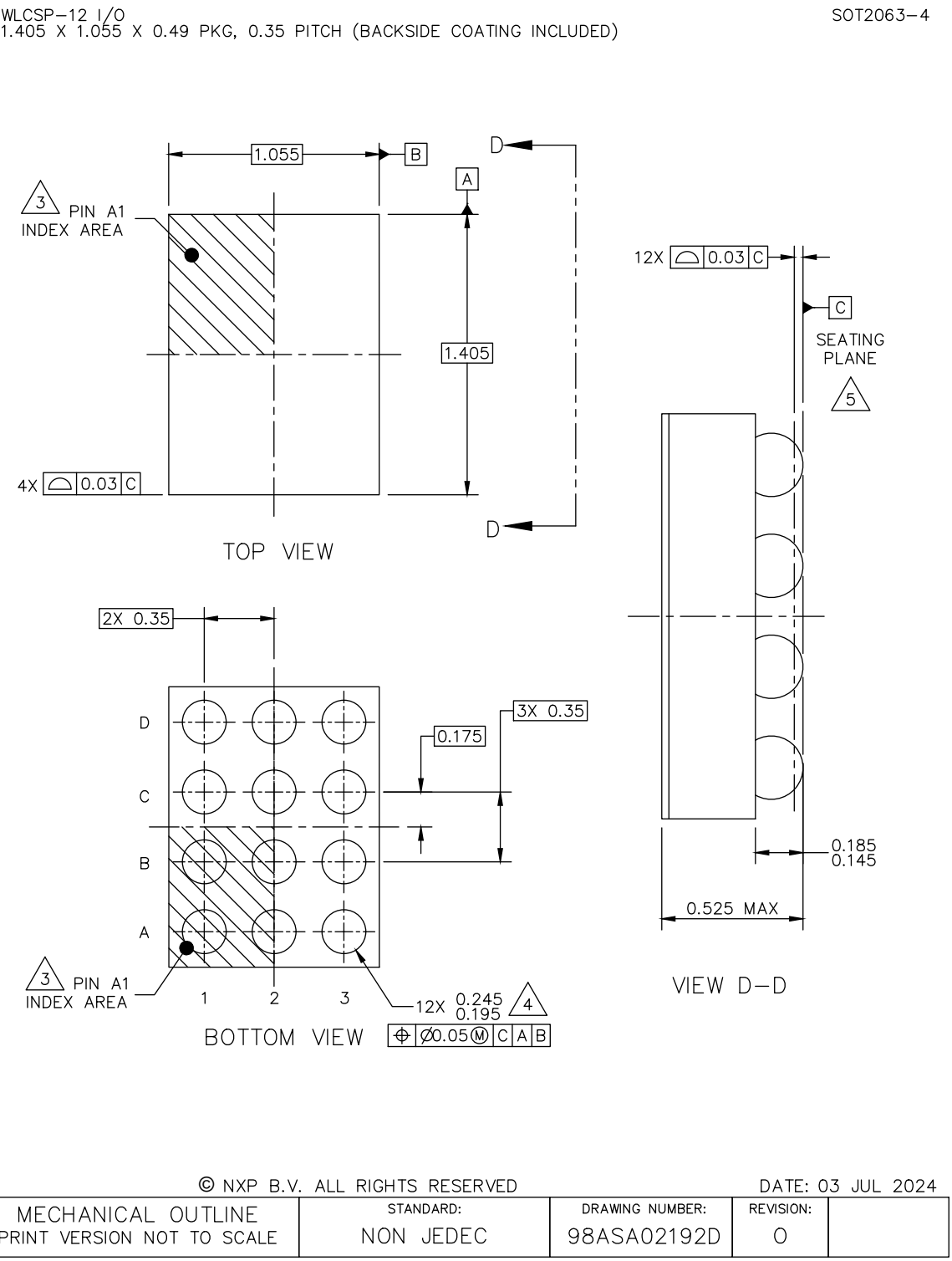


Figure 8. Package outline SOT2063-4 (WLCSP12)

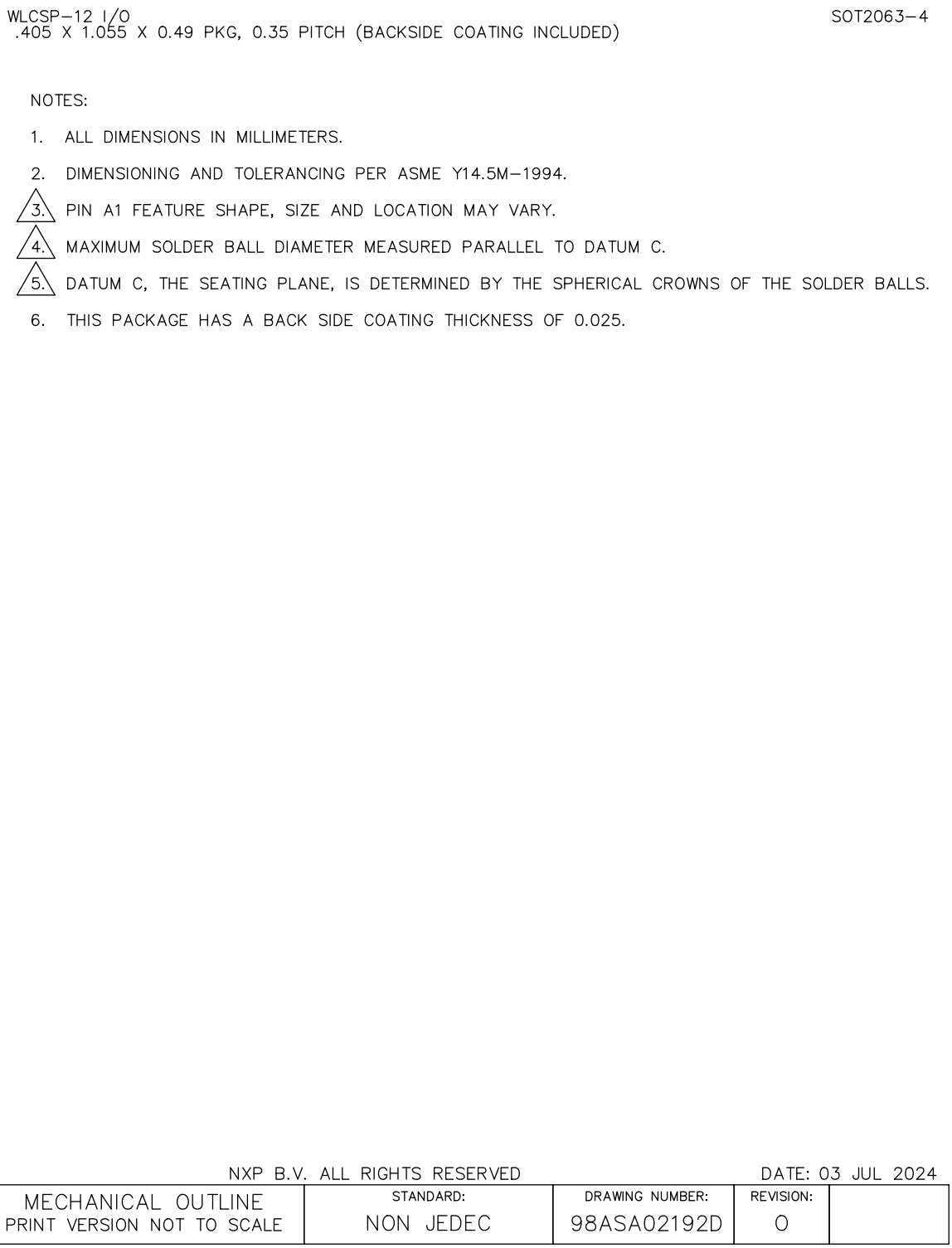


Figure 9. Package outline SOT2063-4 (WLCSP12); notes

16 Soldering

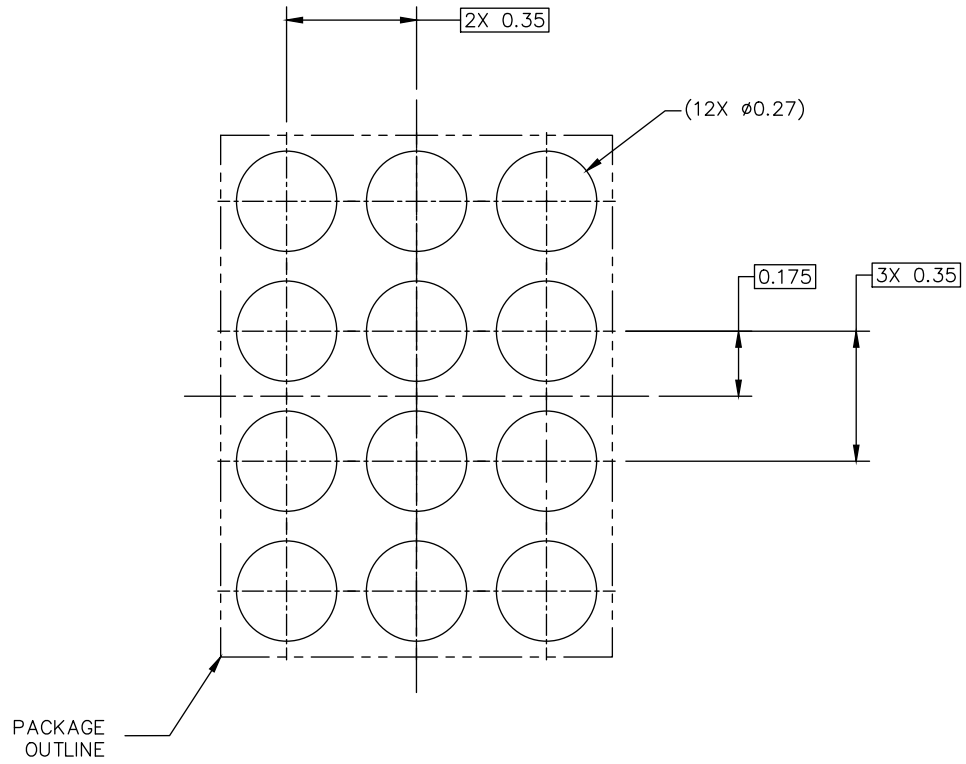
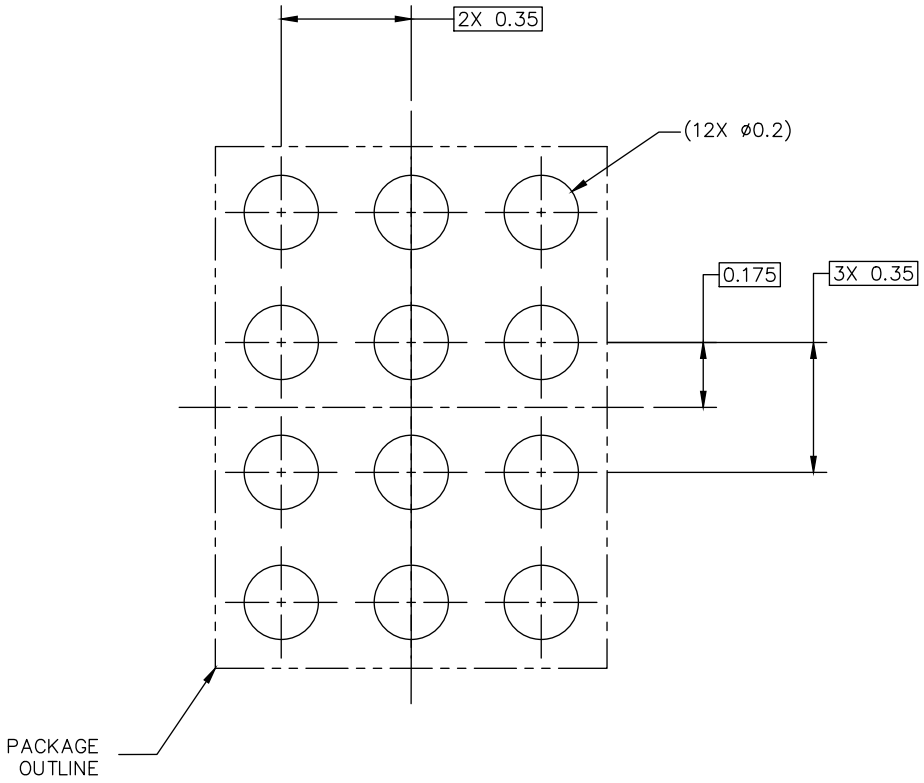


Figure 10. Soldering footprint for SOT2063-4 (WLCSP12); solder mask opening pattern

WLCSP−12 I/O
1.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063−4



PCB DESIGN GUIDELINES − I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

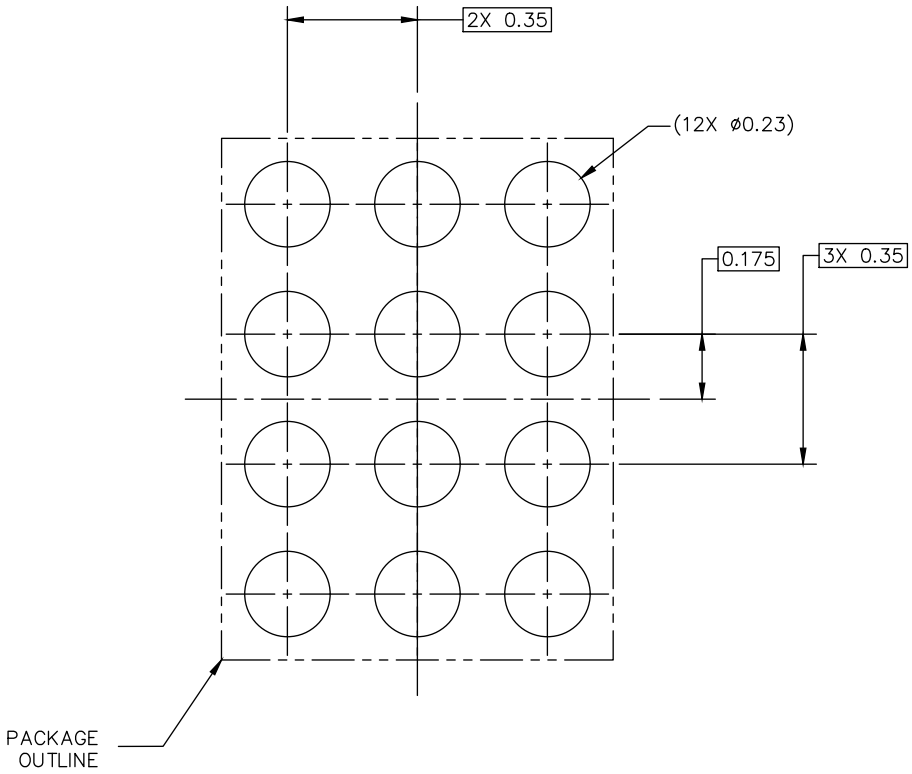
DATE: 03 JUL 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02192D	REVISION: O	

Figure 11. Soldering footprint for SOT2063-4 (WLCSP12); I/O pads and solderable area

WLCSP−12 I/O
.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063−4



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES − SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 03 JUL 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02192D	REVISION: O	

Figure 12. Soldering footprint for SOT2063-4 (WLCSP12); solder paste stencil

17 Revision history

Table 12. Revision history

Document ID	Release date	Description
P3A1604UK v.1.0	10 December 2024	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents