SL3S1206

UCODE 9

Rev. 3.5 — 12 February 2025   **Product data sheet**

1 General description

UCODE 9 offers high performance and features for use in the most demanding RFID tagging applications.

Particularly well suited for inventory management applications, for example, retail and fashion, baggage tagging, and smart logistics with its great RF performance for any given form factor, UCODE 9 enables long read ranges and fast inventory of dense RFID tag populations. With its broadband design, it offers the possibility to manufacture true global RFID labels with great performance across worldwide regulations.

2 Features and benefits

2.1 Key features

- Read sensitivity -24 dBm
- Write sensitivity -22 dBm
- Innovative functionality
  - Drop-in replacement to UCODE 9 due to similar assembled input capacitance
  - Self-Adjust
  - Memory Safeguard
  - Dynamic backscatter
  - Pre-serialization of 96-bit EPC
- Compatible with single-slit antenna
- 96-bit unique tag identifier (TID) factory locked, including 48-bit unique serial number
- EPC Gen2v2.1

2.1.1 Memory

- 96-bit of EPC memory
- Supports pre-serialization of 96-bit EPC
- 96-bit Tag IDentifier (TID) factory-locked
- 48-bit unique serial number factory-encoded into TID
- 32-bit kill password to permanently disable the tag
- Wide operating temperature range: -40 °C up to +85 °C
- Minimum 100k write cycle endurance

2.2 Supported features

- All mandatory commands of the EPCglobal Gen2v2.1 specification are implemented including:
  - Kill Command

- The following optional commands are implemented in conformance with the EPC specification:
  - BlockWrite (2 words, 32-bit)

- Self-Adjust for automated tag performance optimization

All supported features of the UCODE 9 can be activated using standard EPCglobal READ / WRITE commands. No custom commands are needed to take advantage of all the features.

3 Applications

3.1 Target market

- Retail
  - Brick and mortar
  - E-commerce
  - Omnichannel
- Supply chain management
- Airline baggage tracking

3.2 Applications

- Highly accurate and fast inventory management, enabling omnichannel retail processes
- Tracking along the supply chain from source to store
- High-speed store checkout process, bringing convenience to the customer
- Loss prevention
- After sales operations: return and warranty management

For other applications, contact NXP Semiconductors for support.

4 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Name	IC type	Description	
SL3S1206FUD2/HA	Wafer	UCODE 9	Die on sawn 12" 120 µm wafer 10 µm Polyimide spacer with Large Pads; Conventional Dicing	Not applicable
SL3S1206FUD2/HAP	Wafer	UCODE 9	Die on sawn 12" 120 µm wafer 10 µm Polyimide spacer with Large Pads; Plasma Dicing	Not applicable

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet   **Rev. 3.5 — 12 February 2025**   Document feedback

4 / 31

5 Block diagram

The UCODE 9 IC consists of three major blocks:

• Analog interface
• Digital control
• EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader which is then processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol, and handles communication with the EEPROM, which contains the EPC and the user data.
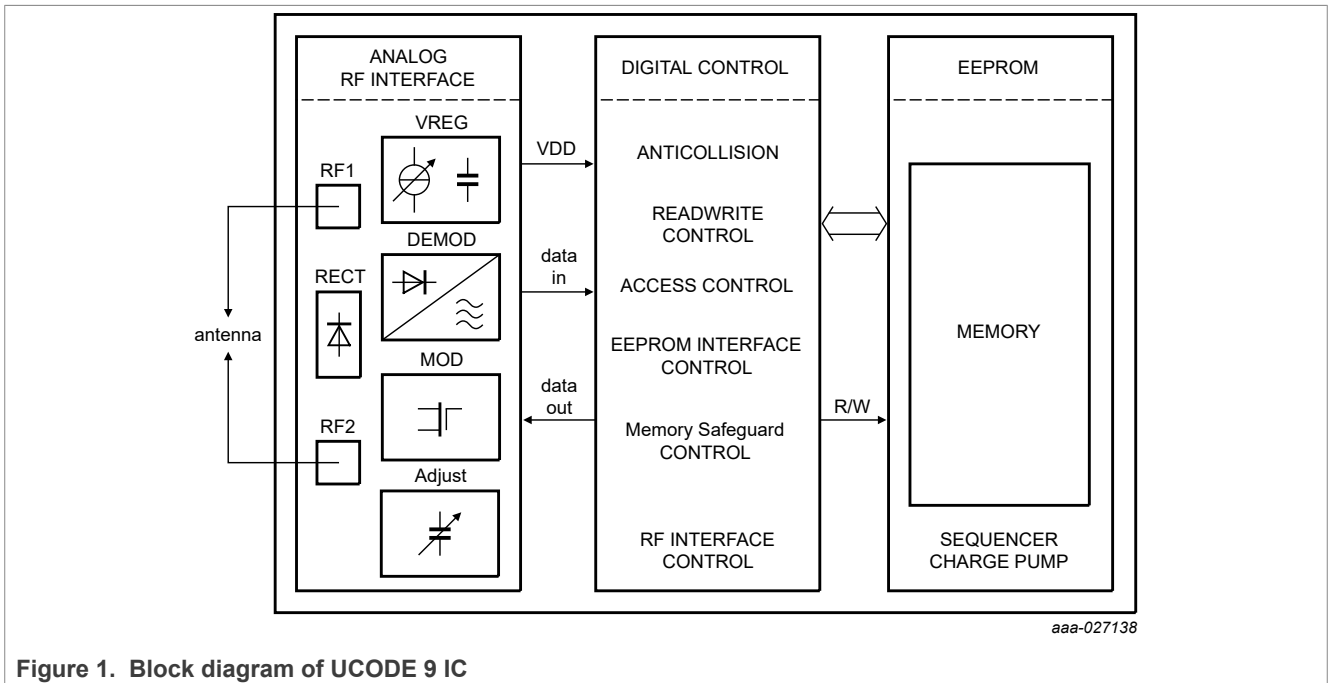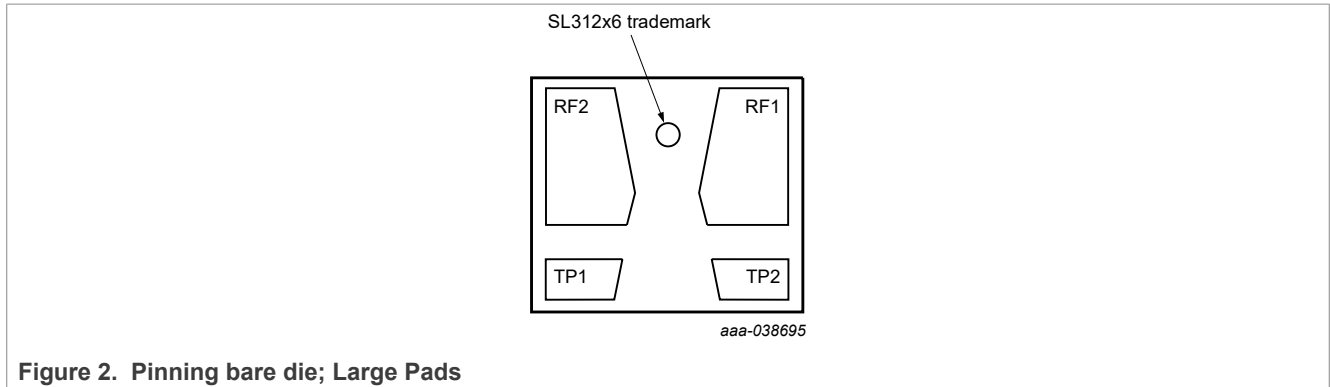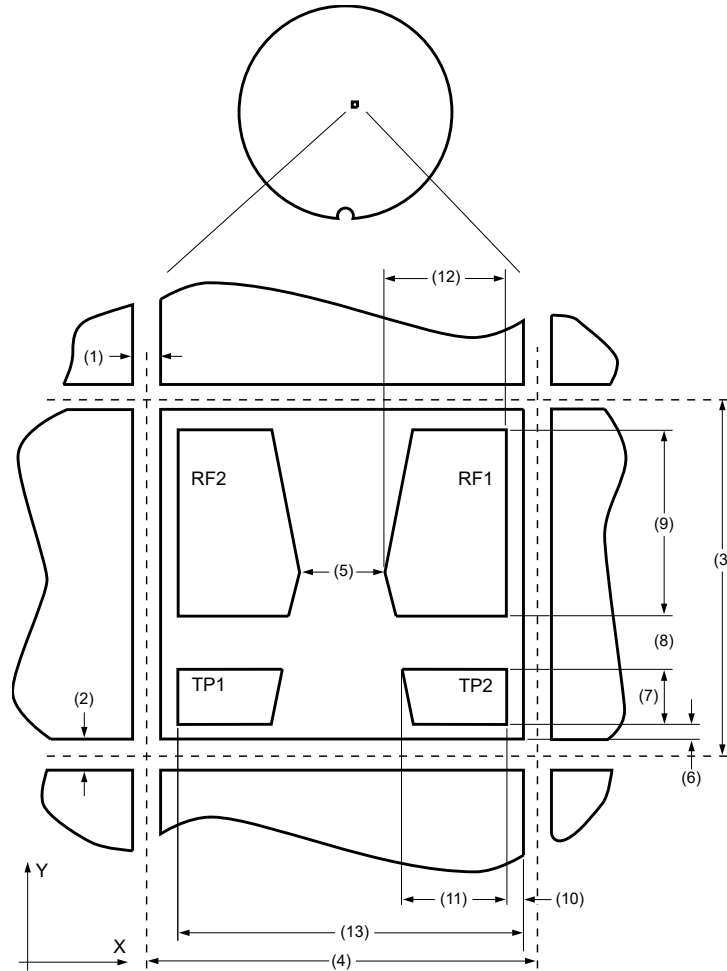

aaa-027138

Figure 1. Block diagram of UCODE 9 IC

Product data sheet

6   Pinning information

Figure 2. Pinning bare die; Large Pads

6.1 Pin description

Table 2. Pin description bare die

Symbol	Description
TP1	test pad 1
RF1	antenna connector 1
TP2	test pad 2
RF2	antenna connector 2

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet

Rev. 3.5 — 12 February 2025

Document feedback

6 / 31

7 Wafer layout

not to scale!

aaa-038696

1. Die to die distance (metal sealring - metal sealring) 39 μm, (X-scribe line width: 35 μm)
2. Die to die distance (metal sealring - metal sealring) 39 μm, (Y-scribe line width: 35 μm)
3. Chip step, Y-length: 415 μm
4. Chip step, X-length: 465 μm
5. Bump to bump distance X (RF1 - RF2): 115 μm
6. Distance bump to metal sealring Y: 21.5 μm
7. Bump size (TP1, TP2) Y: 59.5 μm
8. Bump to bump distance Y (RF1 - TP2, RF2 - TP1): 50 μm
9. Bump size (RF1, RF2) Y: 223.5 μm
10. Distance bump to metal sealring X: 21.5 μm
11. Bump size (TP1, TP2) X: 114.5 μm
12. Bump size (RF1, RF2) X: 134 μm
13. Distance bump to metal sealring X: 404.5 μm

Remark: *TP1 and TP2 are electrically disconnected after dicing.*

Figure 3. UCODE 9, 12" wafer layout, conventional dicing, Large Pads

not to scale!
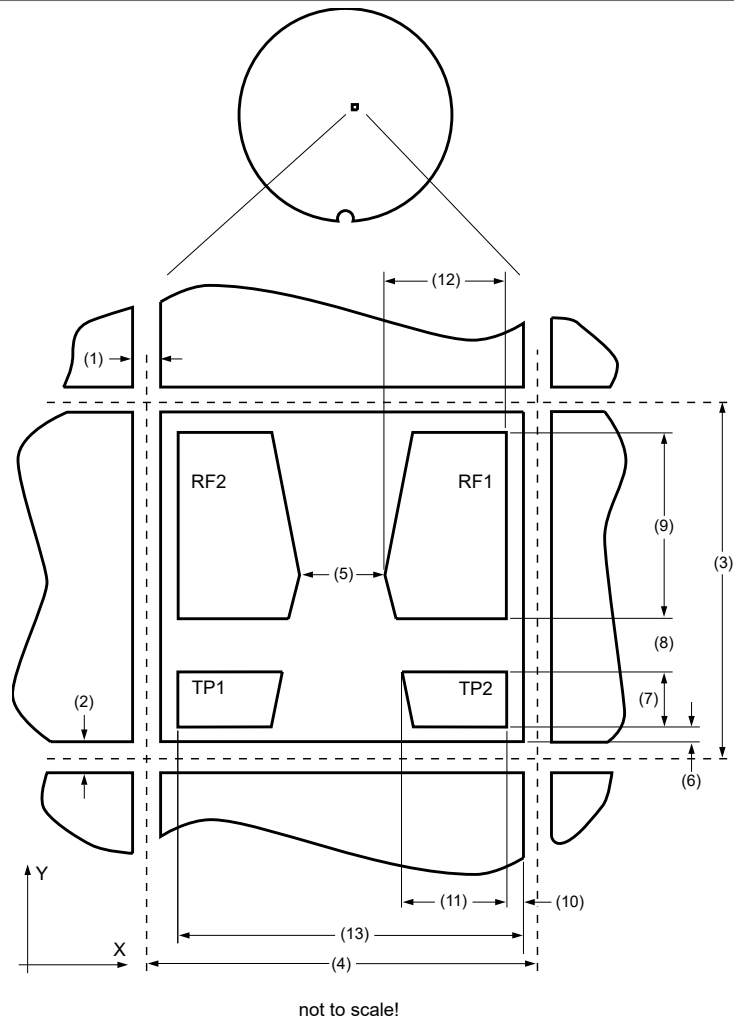
aaa-038696

1. X-scribe line width: typ. 7 μm
2. Y-scribe line width: typ. 7 μm
3. Chip step, Y-length: 395.6 μm
4. Chip step, X-length: 434.6 μm
5. Bump to bump distance X (RF1 - RF2): 115 μm
6. Distance bump to metal sealring Y: 16.5 μm
7. Bump size (TP1, TP2) Y: 70.5 μm
8. Bump to bump distance Y (RF1 - TP2, RF2 - TP1): 50 μm
9. Bump size (RF1, RF2) Y: 223.5 μm
10. Distance bump to metal sealring X: 16.5 μm
11. Bump size (TP1, TP2) X: 114.5 μm
12. Bump size (RF1, RF2) X: 134 μm
13. Distance bump to metal sealring X: 399.5 μm

Figure 4. UCODE 9, 12" wafer layout, plasma dicing, Large Pads

SL3S1206
All information provided in this document is subject to legal disclaimers.
© 2025 NXP B.V. All rights reserved.

Product data sheet
Rev. 3.5 — 12 February 2025
Document feedback

8 / 31

8 Mechanical specification

UCODE 9 wafers are available in 120 µm thickness. The 120 µm thick wafer includes a 10 µm polyimide spacer resulting in less coupling between the antenna and the active circuit, leaving more room for process control (for example, pressure).

8.1 Wafer specification

8.1.1 12-inch wafer, conventional dicing

See [3].

Table 3. 12-inch specification, conventional dicing, Large Pads

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	300 mm (12") unsawn
Thickness	120 µm ± 15 µm
Number of pads	4
Pad location	nondiagonal / placed in chip corners
Process	CMOS 0.14 µm
Batch size	25 wafers
Net printed dies per wafer	342742
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size excluding scribe	0.43 mm × 0.38 mm = 0.16 mm^2
Scribe line width	X-dimension = 35 µm
	Y-dimension = 35 µm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 µm total thickness of passivation
Polyimide spacer	10 µm ± 2 µm
Au pads	
Pad material	> 99.9 % pure Au
Pad hardness	35 – 80 HV 0.005
Pad shear strength	> 70 MPa
Pad height	3 µm

SL3S1206

Product data sheet **Rev. 3.5 — 12 February 2025** Document feedback

9 / 31

Table 3. 12-inch specification, conventional dicing, Large Pads...*continued*

Pad height uniformity	
– within a die	max. 2 µm
– within a wafer	max. 4 µm
Pad flatness	max. 3 µm
Pad size	
– RF1, RF2 (max. For details, see Section 7 "Wafer layout")	134 µm × 223.5 µm
– TP1, TP2 (max. For details, see Section 7 "Wafer layout")	114.5 µm × 59.5 µm
Pad size variation	± 5 µm

8.1.2 12-inch wafer, plasma dicing

See [3].

Table 4. 12-inch specification, Plasma Dicing, Large Pads

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	300 mm (12") unsawn
Thickness	120 µm ± 15 µm
Number of pads	4
Pad location	nondiagonal / placed in chip corners
Process	CMOS 0.14 µm
Batch size	25 wafers
Net printed dies per wafer	389411
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size excluding scribe	0.426 mm × 0.387 mm = 0.16 mm^2
Scribe line width	X-dimension = 8.6 µm
	Y-dimension = 8.6 µm
Passivation on front	
Type	Sandwich structure
Material	PE-Oxide (on top)
Thickness	2.25 µm total thickness of passivation
Polyimide spacer	10 µm ± 2 µm
Au pads	
Pad material	> 99.9 % pure Au

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet

Rev. 3.5 — 12 February 2025

Document feedback

10 / 31

Table 4. 12-inch specification, Plasma Dicing, Large Pads*...continued*

Pad hardness	35 – 80 HV 0.005
Pad shear strength	> 70 MPa
Pad height	3 μm
Pad height uniformity	
– within a die	max. 2 μm
– within a wafer	max. 4 μm
Pad flatness	max. 3 μm
Pad size	
– RF1, RF2 (max. For details, see Section 7 "Wafer layout")	134 μm × 223.5 μm
– TP1, TP2 (max. For details, see Section 7 "Wafer layout")	114.5 μm × 70.5 μm
Pad size variation	± 5 μm

8.1.3 Fail die identification

No ink dots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See [3].

8.1.4 Map file distribution

See [3].

SL3S1206
Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 3.5 — 12 February 2025

© 2025 NXP B.V. All rights reserved.

Document feedback

11 / 31

9 Functional description

9.1 Air interface standards

The UCODE 9 fully supports all parts of the "EPC[TM] Radio-Frequency Identity Protocols Generation-2 UHF RFID, Specification for RFID Air Interface, Protocol for Communications at 860 MHz to 960 MHz, Version 2.1" [1].

9.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE 9. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum power for the UCODE 9 on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a smoothed DC voltage to the analog and digital modules of the IC.

The antenna that is attached to the chip may use a direct contact (DC) connection between the two antenna pads. Therefore, the UCODE 9 also enables loop antenna design.

9.3 Data transfer

9.3.1 Interrogator to tag Link

An interrogator transmits information to the UCODE 9 by modulating an UHF RF signal. The UCODE 9 receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the UCODE 9 by modulating an RF carrier.

For further details, refer to [1].

9.3.2 Tag to interrogator Link

Upon transmitting a valid command, an interrogator receives information from a UCODE 9 tag by transmitting an unmodulated RF carrier and listening for a backscattered reply. The UCODE 9 backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details, refer to [1].

The UCODE 9 communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subcarrier.

SL3S1206

Product data sheet   Rev. 3.5 — 12 February 2025   Document feedback

12 / 31

9.4 Supported commands

UCODE 9 supports all **mandatory** EPCglobal v2.1 commands including

• KILL command

In addition, the UCODE 9 supports the following **optional** commands:

• Block Write (32 bit)

9.5 UCODE 9 memory

The UCODE 9 memory is implemented according to EPCglobal v2.1:

Table 5. UCODE 9 memory sections

Name	Size	Bank
Reserved memory (32 bit Kill password) [1]	32 bit	00b
EPC (excluding 16 bit CRC-16 and 16-bit PC)	96 bit	01b
UCODE 9 Configuration Word	16 bit	01b
TID (including permalocked unique 48-bit serial number)	96 bit	10b

[1]   It is strongly recommended to use diversified passwords for individual tags

The logical address of all memory banks begins at zero (00h).

In addition to the four memory banks, one configuration word to handle the UCODE 9 specific features is available at EPC bank 01 address bit-200h. The configuration word is described in detail in Section 9.6.1

The TID complies with the GS1 EPC Tag Data Standard. See [2].

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet   **Rev. 3.5 — 12 February 2025**   Document feedback

13 / 31

9.5.1 UCODE 9 overall memory map

Table 6. UCODE 9 overall memory map

Bank	Address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	Kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	Access password	all 00h	hardwired to 0, locked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16: refer to [1]		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	0b	hardwired to 0
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 7Fh	EPC	EPC	[1]	unlocked memory
Bank 01 Config Word	200h	EPC	RFU	0b	locked memory
	201h	EPC	RFU	0b	locked memory
	202h	EPC	EPC NOK	0b	indicator bit
	203h	EPC	RFU	0b	locked memory
	204h	EPC	RFU	0b	locked memory
	205h	EPC	RFU	0b	locked memory
	206h	EPC	RFU	0b	locked memory
	207h	EPC	Self-Adjust disable	0b	permanent bit[2]
	208h	EPC	Dynamic backscatter	0b	permanent bit[2]
	209h	EPC	max. backscatter strength	1b	permanent bit[2]
	20Ah	EPC	RFU	0b	locked memory
	20Bh	EPC	RFU	0b	locked memory
	20Ch	EPC	RFU	0b	locked memory
	20Dh	EPC	RFU	0b	locked memory
	20Eh	EPC	RFU	0b	locked memory
	20Fh	EPC	RFU	0b	locked memory
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	1000 0000 0110b	locked memory
	14h	TID	config word indicator	1b[3]	locked memory
	15h to 1Fh	TID	tag model number	TMNR[4]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory

[1] `HEX E280 6995 0000 nnnn nnnn nnnn 0000 0000 or HEX E280 6915 0000 nnnn nnnn nnnn 0000 0000` where n are the nibbles of the SNR from the TID.
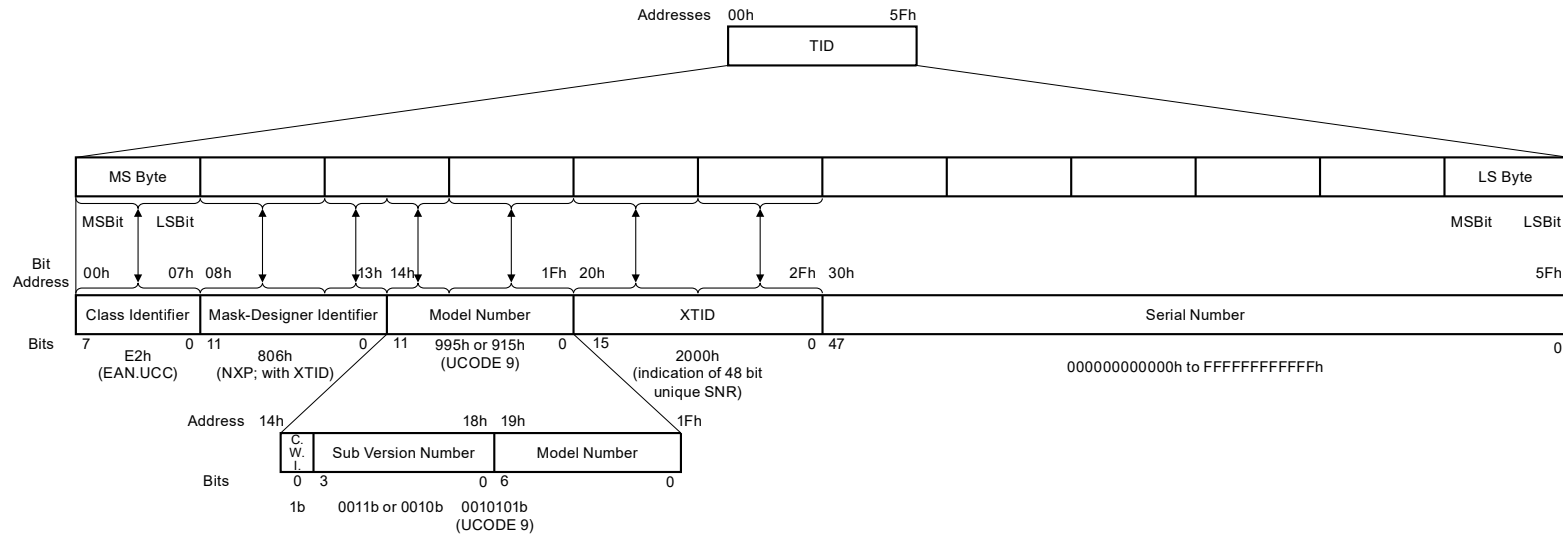[2] Permanent bit: permanently stored bits in the memory; Read/Writeable according to EPC bank lock status, see Section 9.6.1
[3] Indicates the existence of a Configuration Word at the end of the EPC number.
[4] See Figure 5.

9.5.2 UCODE 9 TID memory details

First 48 bit of TID memory	Class ID	Mask Designer ID	Model Number			
			Config Word Indicator	Sub Version Nr.	Version (Silicon) Nr.	XTID Header
UCODE 9	E28069952000	E2h	806h	1b	0011b	0010101b	2000h
	E28069152000	E2h	806h	1b	0010b	0010101b	2000h

Figure 5. UCODE 9 TID memory structure

SL3S1206

Product data sheet **Rev. 3.5 — 12 February 2025**

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Document feedback

15 / 31

9.6 Supported features

The UCODE 9 is equipped with a number of additional features. They are implemented in such a way that standard EPCglobal READ / WRITE commands can be used to operate these features.

The Configuration Word, as mentioned in the memory map, describes the additional features at address 200h of the EPC memory.

Bit 14h of the TID indicates the existence of a Configuration Word. This flag enables the selection of configuration word enhanced transponders in mixed tag populations.

9.6.1 UCODE 9 features control mechanism

The different features of the UCODE 9 can be activated / de-activated by addressing or changing the content of the corresponding bit in the configuration word at address 200h in the EPC memory bank (Table 7). The de-activation of the action bit features will only happen after chip reset.

Table 7. Configuration word UCODE 9

Indicator bit			Locked memory				Permanent bit
RFU	RFU	EPC NOK	RFU	RFU	RFU	RFU	Self-Adjust disable
0	1	2	3	4	5	6	7

Table 8. Configuration word UCODE 9 ... continued

Permanent bit	Permanent bit	Locked memory					
Dynamic backscatter	max.backscatter strength	RFU	RFU	RFU	RFU	RFU	RFU
8	9	10	11	12	13	14	15

The configuration word contains 3 different types of bits:

- **Permanent bits**: permanently stored bits in the memory
  Self-Adjust disable
  Dynamic backscatter
  Max. Backscatter Strength
- **Indicator bit**: cannot be changed by command
  EPC NOK

The activation or the de-activation of the feature behind the permanent bits happens only when attempting to write a "1" value to the related bit (value toggling) - writing "0" value has no effect. If the feature is activated, the related bit will be read with a "1" value and, if de-activated, with a "0" value. The permanent bits can only be toggled by using standard EPC WRITE (not a BlockWrite) if the EPC bank is unlocked. If the EPC is permalocked, they cannot be changed.

A SELECT on the Configuration word is treated as not-matching.

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet

Rev. 3.5 — 12 February 2025

Document feedback

16 / 31

9.6.2 Self-Adjust

9.6.2.1 Description

The UCODE 9 has an automatic mechanism implemented which adjusts the chip sensitivity to a maximum in the operated environment. This adjustment will be performed at startup and selects between three different input capacitance values (center capacitance -60 fF / +100 fF). The feature is enabled by default, but can also be deactivated by the config word bit 207h (Self-Adjust disable). In case of deactivation, the center capacitance is used.

9.6.3 Dynamic backscatter

9.6.3.1 Description

UCODE 9 introduces the new enhanced Dynamic backscatter feature in addition to the standard UCODE backscatter control. The three modes can be controlled by modifying bit 208h and bit 209h within the configuration word. Per default, maximum backscatter is enabled in order to achieve maximum read rates. In case backscatter strength reduction is necessary nominal backscatter strength can be selected.

The third new introduced Dynamic Backscatter mode enables maximum backscatter at low chip power levels and gradually reduces the backscatter strength at high-power levels enabling the best performance and also meet regulatory limits.

Table 9. Backscatter Control

Dynamic Backscatter Bit	Max. Backscatter Bit	Description
0	0	Nominal Backscatter
0	1	Maximum Backscatter
1	0	Dynamic Backscatter
1	1	Maximum Backscatter

9.6.4 Memory Safeguard

9.6.4.1 Description

The Memory Safeguard of UCODE 9 consist of two different countermeasures which ensures the integrity of the stored data:

ECC (Error correction code):

The implemented ECC is applied on the complete UCODE 9 memory and requires no user action. With this feature, a single bit failure in the memory is detected and corrected automatically. In case of 2-bit fail, an indication as described below is given.

EPC Memory:

Config word bit 202h (EPC NOK) provides an indication that a 2-bit failure occurred in the EPC memory by changing its value to "1". In such a case, UCODE 9 will respond with an EPC value of F's indicating a corrupted EPC. A read of the EPC memory content will provide the actual content.

SL3S1206
Product data sheet

All information provided in this document is subject to legal disclaimers.
Rev. 3.5 — 12 February 2025

© 2025 NXP B.V. All rights reserved.
Document feedback
17 / 31

Parity check:

A parity check on the TID is implemented to offer the possibility to identify a change in the TID. The parity bit (Even parity) will be calculated and locked in the manufacturing process. For a check, the TID content needs to be read out and parity checked.

9.6.5 Pre-serialization of the 96-bit EPC

9.6.5.1 Description

UCODE 9 is delivered with a pre-serialized content of the 96-bit EPC, which is the initial programmed length of the EPC.

The EPC content is identical to the TID content except of the 16-bit XTID content which is set to 16-bit 0's.
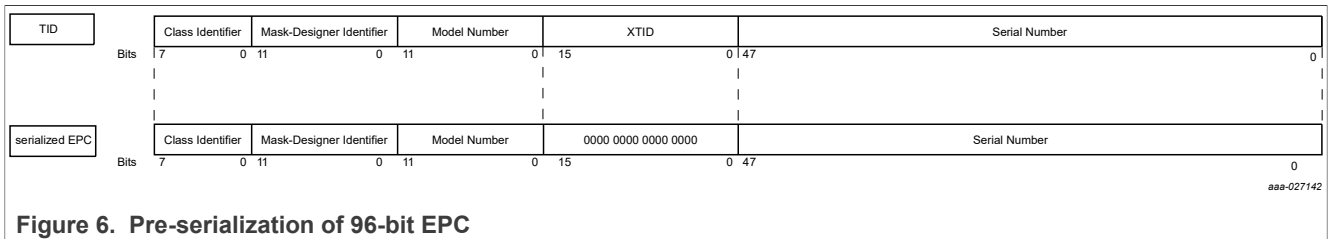
Figure 6. Pre-serialization of 96-bit EPC

9.6.6 Single-slit antenna solution

9.6.6.1 Description

In UCODE 9, the test pads TP1 and TP2 are electrically disconnected and therefore can be safely short-circuited to the RF pads (RF1, RF2). See Figure 7.

A single antenna enables easier assembly and antenna design. In addition to the standard antenna assembly, the related increased input capacitance (Table 11) can be used for optimization for different antenna design.
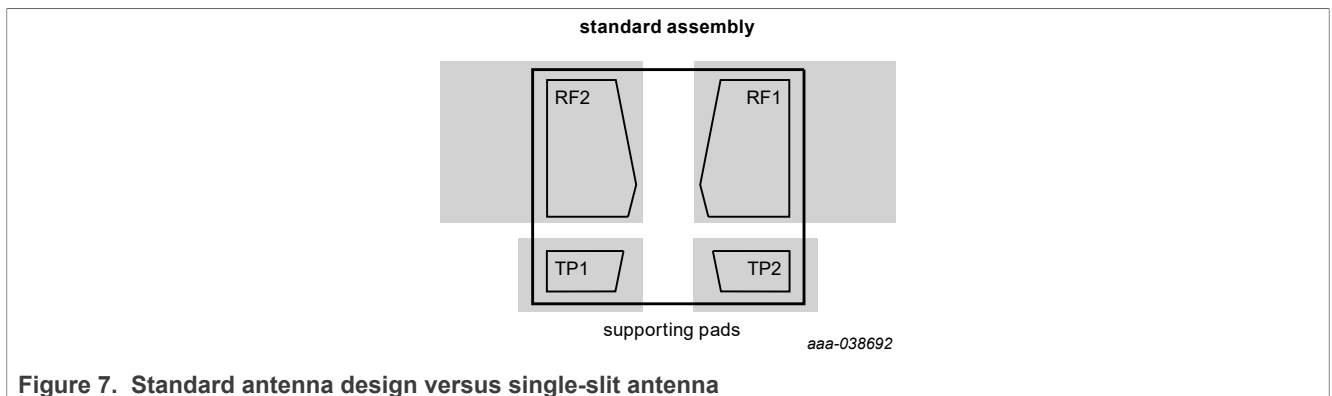
Figure 7. Standard antenna design versus single-slit antenna
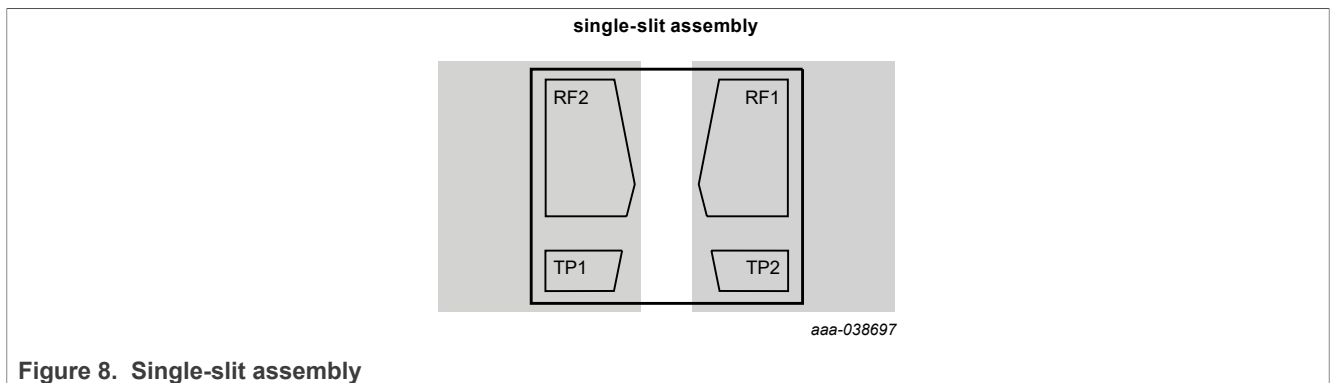
Figure 8. Single-slit assembly

9.6.7 Large pads

9.6.7.1 Description

The large gold pads of UCODE 9 enable more robust and reliable assembly. This pad design allows for more freedom in the placement accuracy (see Figure 9).
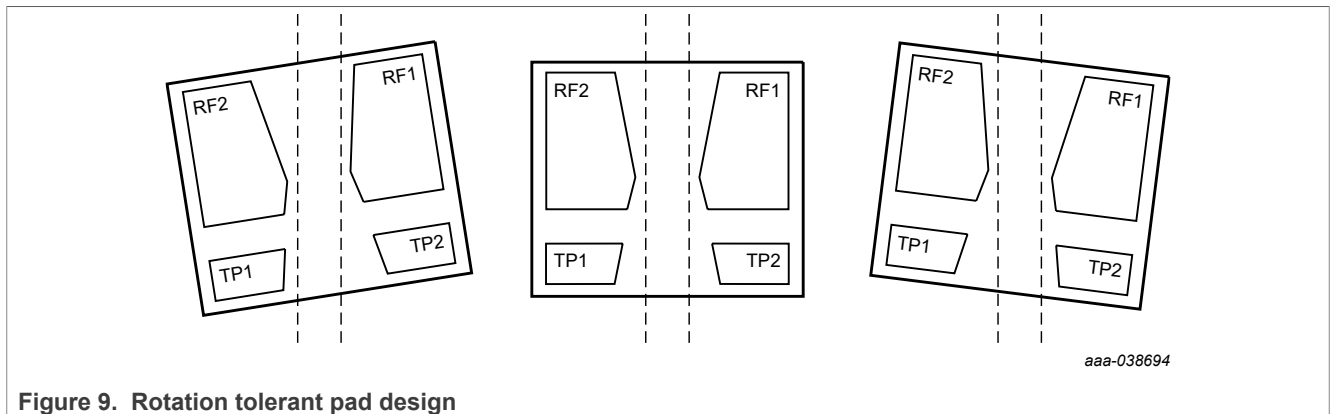
Figure 9. Rotation tolerant pad design

9.6.8 Permalock

UCODE 9 permalock is implemented according to EPCglobal using the LOCK command with a payload of FFFFFh.

For any payload other than FFFFFh UCODE 9 backscatters an error code.

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet

Rev. 3.5 — 12 February 2025

Document feedback

20 / 31

10 Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to RFN. [1] [2]

Symbol	Parameter	Conditions		Min	Max	Unit
Bare die limitations						
T_{stg}	storage temperature			-55	+125	°C
T_{amb}	ambient temperature			-40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[3]	[4]	-	± 2	kV
Pad limitations						
P_i	input power	maximum power dissipation, RF1/RF2 pad		-	100	mW

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] According to ANSI/ESDA/JEDEC JS-001

[4] For ESD measurement, the die chip has been mounted into a CDIP8 package.

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet

Rev. 3.5 — 12 February 2025

Document feedback

21 / 31

11 Characteristics

11.1 UCODE 9 bare die characteristics

Table 11. UCODE 9 RF interface characteristics (RF1, RF2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			840	-	960	MHz
$P_{i(min)}$	minimum input power	READ sensitivity	[1]	-	- 24	-	dBm
$P_{i(min)}$	minimum input power	WRITE sensitivity	[1]	-	-22	-	dBm
t	encoding speed	16-bit	[2]	-	0.6	-	ms
		32-bit (block write)	[2]	-	1	-	ms
C_i	chip input capacitance	parallel, blade diced	[3] [4] [5]	-	0.715	-	pF
C_i	chip input capacitance	parallel, plasma diced	[3] [4] [5]	-	0.700	-	pF
R_P	chip resistance	parallel	[4]	-	3.6	-	kΩ
Z	chip impedance	915 MHz, blade diced	[3] [4] [5]	-	9-j243	-	Ω
Z	chip impedance	915 MHz, plasma diced	[3] [4] [5]	-	10-j248	-	Ω
Z	typical assembled impedance[6]	915 MHz, blade diced	[7] [8] [9]	-	15-j231	-	Ω
Z	typical assembled impedance[6]	915 MHz, plasma diced	[7] [8] [9]	-	16-j237	-	Ω
Z	typical assembled impedance in case of single-slit antenna assembly[10]	915 MHz	[7] [11] [9]	-	10-j191	-	Ω

[1]   Tag sensitivity on a 2.15 dBi gain antenna
[2]   When the memory content is "0000...".
[3]   Measured with a 50 Ω source impedance directly on the chip
[4]   At minimum operating power
[5]   at center capacitor of Self-Adjust
[6]   see Figure 7
[7]   The antenna shall be matched to this impedance
[8]   Assuming 35 fF additional assembly capacitance
[9]   At center capacitor of Self-Adjust
[10] see Figure 8
[11] Assuming 195 fF (Blade)/210fF (Plasma) additional assembly+test pad capacitance

Table 12. UCODE 9 memory characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
EEPROM characteristics							
t_{ret}	retention time	T_{amb} ≤ 55 °C		20	-	-	year
		T_{amb} ≤ 85 °C		10	-	-	year
		T_{amb} ≤ 125 °C		1	-	-	year
$N_{endu(W)}$	write endurance			100k	-	-	cycle

12 Packing information

12.1 Wafer

See [3].

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet **Rev. 3.5 — 12 February 2025**

Document feedback

23 / 31

13 Abbreviations

Table 13. Abbreviations

Acronym	Description
CRC	cyclic redundancy check
CW	continuous wave
DSB-ASK	double side band-amplitude shift keying
DC	direct current
EAS	electronic article surveillance
EEPROM	electrically erasable programmable read only memory
EPC	electronic product code (containing header, domain manager, object class and serial number)
FM0	bi-phase space modulation
G2	Generation 2
IC	Integrated Circuit
PIE	pulse interval encoding
PSF	product status flag
RF	radio frequency
UHF	ultra high frequency
SECS	Semi Equipment Communication Standard
TID	tag identifier

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet

Rev. 3.5 — 12 February 2025

Document feedback

24 / 31

14 References

[1] EPCglobal: EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 2.1 (July 2018)

[2] EPCglobal: EPC Tag Data Standard, Release 1.13 (November 2019)

[3] Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, BU-S&C document number: 1862**[1]

---

1 ** ... document version number

15 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Supersedes
SL3S1206 v.3.5	12 February 2025	Product data sheet	SL3S1206 v.3.4
Modifications:	Editorial changes. • Document security status changed to "Public", no content change.		
SL3S1206 v.3.4	28 May 2024	Product data sheet	SL3S1206 v.3.3
Modifications:	• Section 8.1.2 "12-inch wafer, plasma dicing": Table 4: Net printed dies per wafer updated.		
SL3S1206 v.3.3	24 March 2023	Product data sheet	SL3S1206 v.3.2
Modifications:	• Section 8.1.1 "12-inch wafer, conventional dicing": updated. • Section 9.5.1 "UCODE 9 overall memory map": updated. • Section 9.5.2 "UCODE 9 TID memory details": updated.		
SL3S1206 v.3.2	03 June 2022	Product data sheet	SL3S1206 v.3.1
Modifications:	• UCODE 9 with Plasma Dicing delivery form added. • Section 4 "Ordering information": updated. • Section 7 "Wafer layout": Plasma diced wafer updated. • Section 8.1.2 "12-inch wafer, plasma dicing": added. • Section 11.1 "UCODE 9 bare die characteristics": updated. • Editorial changes		
SL3S1206 v.3.1	02 December 2021	Product data sheet	530930
Modifications:	• Section 11.1 "UCODE 9 bare die characteristics": Update retention times. • Remove SELECT as feature control mechanism. • Insert comment on recommended password diversification.		
SL3S1206 v.3.0	15 December 2020	Product data sheet	530920
Modifications:	• Data sheet status changed to "Product data sheet", no content change.		
530920	03 December 2020	Preliminary data sheet	530911
Modifications:	• Section 7 "Wafer layout": Update of pad dimensions • Section 9.5.2 "UCODE 9 TID memory details": Update of TMN • Section 9.6.2 "Self-Adjust": Capacitance values added • Section 11.1 "UCODE 9 bare die characteristics": updated.		
530911	20 August 2020	Objective data sheet	530910
Modifications:	• Section 10 "Limiting values": T_{amb} updated. • Section 9.6.3 "Dynamic backscatter" Paragraph format updated. • Section 9.6.4 "Memory Safeguard": Paragraph added. • Section 2.1 "Key features": Memory safeguard added.		
530910	22 July 2020	Objective data sheet	-

SL3S1206

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Product data sheet

Rev. 3.5 — 12 February 2025

Document feedback

26 / 31

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

UCODE — is a trademark of NXP B.V.

Tables

SL3S1206

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 3.5 — 12 February 2025

© 2025 NXP B.V. All rights reserved.

Document feedback

29 / 31

Figures

Contents