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Differences Between the MPC82X Series Microprocessors

1. Differences between the MPC821 and the MPC823

The MPC823 is mostly a subset of the MPC821 microprocessor. To create the MPC823, the following modifications were made to the MPC821:

- Instruction cache was reduced from 4K to 2K
- Data cache was reduced from 4K to 1K
- Instruction and data MMUs were reduced from 32 to 8 TLB entries each
- Pin count was reduced from 357 to 256 pins
- Package size was reduced from 25mm (XP) to 23mm (ZT)
- Address bus was reduced from 32 bits to 26 bits
- Bisync protocol was removed from the serial communication controller
- PCMCIA support was reduced to a single channel, PCMCIA channel B
- One serial communication controller was removed from the CPM leaving a single channel (SCC2)
- One USB channel was added to CPM in place of SCC1
- High-speed IRDA support (1.152Mbps and 4Mbps) was added
- Centronics protocol was removed
- Video controller was added to support NTSC/PAL monitors
- CAM for Ethernet/IEEE 802.3 protocol is not supported

The *MPC823 User's Manual Revision 1* and the *MPC823e User's Manual Revision 0* discuss the operation, possible configurations, and specifications of the MPC823 and the MPC823e microprocessors, respectively. The manuals are available in hardcopy, on CD-ROM, and are available to download as a Portable Document Format (PDF) files. Contact your local Motorola sales office or refer to the contact information at the end of this document to order this and other MPC823 device documents.

2. Differences between each revision of MPC823 silicon

Table 1. Feature Differences Between Each Revision of the MPC823 Silicon

FEATURES	REV 0	REV A	REV B
Mask Numbers	3F98S 3F98S 1F98S 0F98S	0H89G	0H97G, 1H97G, 3H97G
Dual Port RAM (DPRAM) SIze	5KB	8KB	8KB
DPRAM Microcode Capacity	1K	2K	2K
Number of Active SCCs	1 (SCC2)	1 (SCC2)	2 (SCC2 & SCC3) *See pages 3 and 4 for details*
Baud Rate Generators	2	4*	4*
5V Compatibility	ALL Pins Except: EXTAL, XTAL, and XFC	JTAG and General Purpose I/O (i.e.,I/O Ports A,B,C,D) Pins ONLY	JTAG and General Purpose I/O (i.e., I/O Ports A,B,C, D) Pins ONLY
LCD Controller	Base	Improved FRC Algorithm (Resulting in Better Image Quality at Lower Refresh Rates)	Improved FRC Algorithm (Resulting in Better Image Quality at Lower Refresh Rates
Universal Serial Bus	**Base**	**Base**	**Host Functionality:** -Added support for low speed devices (was not supported on Rev A). This allows the host to communicate with low speed devices through a hub. **Slave Functionality:** -Removed the generation of TxE interrupt when NACK is transmitted. -The transmitter responds with NACK until the TX FIFO has reached a certain watermark. In Rev A, the transmission of a packet was not conditioned on the FIFO reaching a watermark. -More robust detection of start of packet. Some USB errata were fixed in Rev B. See updated USB section of the MPC823 User's Manual Rev 1.

*BRG04 Cannot Be Output Externally

3. SCC3-Related documentation changes for the MPC823 Rev B silicon

The following prioritized list contains the processing order of the microcontroller from highest to lowest priority.

1. Reset in CPM command register or at reset
2. SDMA bus error
3. Commands issued to the command register, including DSP-related commands
4. IDMA DREQ1 (default setting)
5. IDMA DREQ2 (default setting)
6. USB Reception (RX)
7. USB Transmission (TX)
8. SCC2 RX
9. SCC2 TX
10. SCC3 RX
11. .SCC3 TX
12. IDMA DREQ1 (option 2)
13. IDMA DREQ2 (option 2)
14. SMC1 RX
15. SMC1 TX
16. SMC2 RX
17. SMC2 TX
18. SPI RX
19. SPI TX
20. I2C RX
21. I2C TX
22. RISC timer tables
23. IDMA DREQ1 (option 3)
24. IDMA DREQ2 (option 3)

✥

When programming the CPM Command Register (CPCR) for SCC3, the CH_NUM (channel number field) is 1000.

✥

The SCC3 Parameter RAM memory base address is DPRAM_Base + 0x1e00 = IMMR + 0x3e00.

✥

The SCC3 does not support IrDA.

✥

In the Serial Interface RAM Entries table, Channel Select for SCC3 is:

CSEL-Channel Select
011 = The bit/byte group is routed to SCC3.

✥

The Serial Interface Clock Route Register (SICR) fields for SCC3 are:

Bits 8-15 are used for SCC3
Bit 8 is GR3
Bit 9 is SC3
Bits 10-12 are R3CS
Bits 13-15 are T3CS

✥

When programming the parallel port for SCC3, the MPC823 Rev B will implement SCC3 using the following pins:

Pin P15 is PB[30]/SPICLK/TXD3
Pin P14 is PB[29]/SPIMOSI/RXD3
Pin N11 is PB[25]/SMTXD1/TXD3
Pin T11 is PB[24]/SMRXD1/RXD3
Pin P13 is PC[13]/L1ST7/~RTS3
Pin P6 is PC[5]/L1TSYNCA/~SDACK1/~CTS3
Pin T4 is PC[4]/L1RSYNCA/~CD3

The CPM interrupt controller encoding of the five low-order bits of the interrupt vector is shown in the Encoding the Interrupt Vector table. For interrupt number 1C in the table, the interrupt source is SCC3 and the interrupt vector number is 11100.

✥

The following changes were made to the CPM Interrupt Configuration Register (CICR) for SCC3:

SCDP-SCCd Priority Order
This field defines whether the USB or SCCs will assert a request in the SCCd priority position.
10 = SCC3 will assert its request in the SCCd position.
11 = Neither the USB or SCCx will assert its request in the SCCd position.

SCCP-SCCc Priority Order
This field defines whether the USB or SCCs will assert a request in the SCCc priority position.
10 = SCC3 will assert its request in the SCCc position.
11 = Neither the USB or SCC will assert its request in the SCCc position.

SCBP-SCCb Priority Order
This field defines whether the USB or SCCs will assert a request in the SCCb priority position.
10 = SCC3 will assert its request in the SCCb position.
11 = Neither the USB or SCC will assert its request in the SCCb position.

SCAP-SCCa Priority Order
This field defines whether the USB or SCCs will assert a request in the SCCa priority position.
10 = SCC3 will assert its request in the SCCa position.
11 = Neither the USB or SCC will assert its request in the SCCa position.

✥

In the CPM Interrupt Pending Register (CIPR) for SCC3, Bit 3 is called SCC3 and Bit 4 is reserved.

✥

In the CPM Interrupt Mask Register (CIMR) for SCC3, Bit 3 is called SCC3 and Bit 4 is reserved.

✥

In the CPM Interrupt In-Service Register (CISR) for SCC3, Bit 3 is called SCC3 and Bit 4 is reserved.

4. Differences between MPC823 and MPC823e

The following modifications were made to the MPC823 Revision B to create the MPC823e:

- The instruction cache was increased to 16K from 2K
- The data cache was increased to 8K from 1K
- The instruction and data memory management units each consist of 32TLB entries
- A time-division multiplex channel (TDMB) was added to the serial interface

Table 2. Differences between MPC823 revision B and MPC823e

FEATURE	823	823e
TLB	8 entry	32 entry
DCACHE size	1 K	8 K
ICACHE size	2 K	16 K
ICACHE associativity	2-way	4-way
ROM microcode size	8 K	16 K

If you are moving from MPC823 to MPC823e, code modification, if any, will be minimal. Be aware that the following changes may affect your code:

- ICACHE:16K, 4 ways set associative
  ICACHE organization is 256 sets, 4 lines per set, and 4 words per line. ICACHE lines are aligned on 4-word boundaries in memory. On an instruction fetch, bits 20-27 of the instruction's address point into the cache to retrieve the tags and data of one set (the MPC823 used bits 21-27). The IC_ADR bits changed.
- DCACHE: 8KB, 2 ways set associative
  DCACHE organization is 256 sets, 2 lines per set, and 4 words per line. DCACHE lines are aligned on 4-word boundaries in memory. The DC_ADR (for a CACHE read command) bits changed. The DC_DAT (tag read format) bits changed.
- Memory Management Unit(MMU): 32 entry TLB. There are bit changes in the following registers: MI_CTR, MD_CTR.
- IrDA is only available on SCC2.
- Time Slot Assigner has two TSA ports: TDMa and TDMb. There are bit changes or field name changes in the registers that are used to program TDM's. See Table 3 for the pins the TDMb uses.
- SCC: MPC823 Rev B and MPC823e silicon have two SCCs (SCC2, SCC3). The MPC823 Rev 0 and Rev A silicon had only one SCC (SCC2). See Table 4 for the pins the SCC3 uses.

Table 3. MPC823e TDMb pins

PIN NAME	PIN NUMBER
PA[6]/CLK2/$\overline{\text{TOUT1}}$/TIN3/L1RCLKB	P8
PB[24]/SMRXD1/RXD3/L1RXDB	T11
PB[23]/$\overline{\text{SMSYN1}}$/$\overline{\text{CTS3}}$/$\overline{\text{SDACK1}}$/L1RSYNCB	T10
PB[22]/$\overline{\text{SMSYN2}}$/$\overline{\text{SDACK2}}$/L1TSYNCB	R9
PC[15]/$\overline{\text{DREQ1}}$/L1ST5/L1TXDB	R16

Table 4. MPC823e SCC3 pins

PIN NAME	PIN NUMBER
PB[30]/SPICLK/TXD3	P15
PB[29]/SPIMOSI/RXD3	P14
PB[25]/SMTXD1/TXD3	N11
PB[24]/SMRXD1/L1RXDB/RXD3	T11
PC[13]/L1ST7/$\overline{\text{RTS3}}$	P13
PC[5]/L1TSYNCA/$\overline{\text{SDACK1}}$/$\overline{\text{CTS3}}$	P6
PC[4]/L1RSYNCA/$\overline{\text{CD3}}$	T4

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