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MC68HC908QTxA/QYxA to MC68HC08QTx/QYxROM Conversion Guidelines

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1 Introduction

This engineering bulletin describes converting from the MC68HC908QTxA/QYxA to MC68HC08QTx/QYx. The MC68HC08QTx /QYx is a read-only memory version of the MC68HC908QTxA/QYxA devices.

For information on converting from MC68HC908QTx/QYx to QYx ROM refer to “MC68HC08QTx/QYx Conversion Guidelines” (document number EB674).

In this document, the MC68HC08QTx/QYx is referred to as the QYx ROM. The MC68HC908QYxA is referred to as the QYxA. This document provides information needed to convert from QYxA to the ROM QYx and highlights suggestions for making this change.

Contents

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2 Considerations When Transitioning to QYx ROM

The ROM QYx contains slight variations to certain modules on the QYxA. These differences must be taken into account when migrating to the ROM QYx from the QYxA. For more information refer to the MC68HC08QY4 data sheet.

2.1 Oscillator Module Settings (OSC)

The QYx ROM has an identical register set as the QYxA. This means that the bit-by-bit locations within the registers are the same; however, the power-on reset (POR) state of the OSCSC register is not identical between the QYxA and the QYx ROM.

The ICFS bits in the oscillator status and control register (OSCSC) allow the internal oscillator to be configured for operation at 4, 8, or 12.8 MHz (1, 2, or 3.2 MHz BUS respectively). The QYxA has a POR default setting that enables the internal clock to function at 12.8 MHz (3.2 MHz BUS). The QYx ROM can run at a lower voltage than the QYxA. Due to this, the QYx ROM internal clock has a slower clock frequency value upon reset. It is set to 4 MHz (1 MHz BUS). This is important to note when migrating from QYxA to QYx ROM because leaving the default value in this register when submitting the ROM code results in a slower speed than is realized on the QYxA part.

2.1.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	OSCOPT1	OSCOPT0	ICFS1	ICFS0	ECFS1	ECFS0	ECGON	ECGST
Write:								
Reset:	0	0	1	0	0	0	0	0
	= Unimplemented							

Figure 1. Oscillator Status and Control Register (OSCSC) on QYxA

Table 1. ICFS1:ICFS0—Internal Clock Frequency Select Bits for QYxA

ICFS1	ICFS0	Internal Clock Frequency
0	0	4.0 MHz
0	1	8.0 MHz
1	0	12.8 MHz — default reset condition
1	1	Reserved

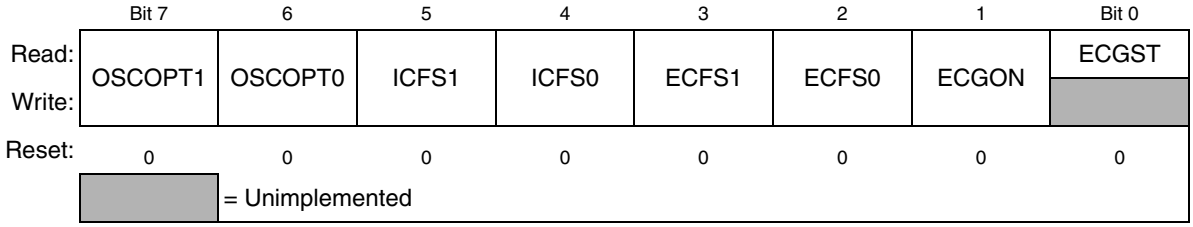

Figure 2. Oscillator Status and Control Register (OSCSC) on QYx ROM

Table 2. ICFS1:ICFS0—Internal Clock Frequency Select Bits for QYx ROM

ICFS1	ICFS0	Internal Clock Frequency
0	0	4.0 MHz — default reset condition
0	1	8.0 MHz
1	0	12.8 MHz
1	1	Reserved

2.2 Operating Voltage Range

The operating voltage range for the QYx ROM supports 1.8 to 3.6 V, 2.7 to 3.3 V, and 4.5 to 5.5 V operation based on a selection in the ROM order form. This is a wider range than the QYxA. Due to the extended range of operation, certain parameters must be considered. These include the maximum BUS speed allowed by the processor and the low-voltage inhibit (LVI) trip points. Table 3 and Table 4 detail the differences.

Table 3. QYxA Characteristics

Operating Voltage	Max BUS Speed	Typical LVI Trip
3 V	4 MHz	2.55 V
5 V	8 MHz	4.2 V

Table 4. QYx ROM Characteristics

Operating Voltage	Max BUS Speed	Typical LVI Trip
1.8 – 3.6 V	2.1 MHz	1.95 V[1]
3 V	4 MHz	1.95 V
5 V	8 MHz	4.2 V

[1] The LVI is recommended to be disabled via software at this low operating voltage because the threshold crosses the operating range. There is a bandgap voltage reference available to calculate values of Vdd. The internal bandgap can then be used to perform a software LVI. An explanation on how this is done can be found in “On-Chip System Protection Basics for Automotive HCS08 Microcontrollers” (document number AN3305).

2.3 Trim Calculation

When using the internal oscillator on the QYx ROM or QYxA, a trim value must be used to achieve the most accurate frequency. On the QYxA, this value is calculated and programmed to location 0xFFC0 by the factory or by a programming tool when the micro is programmed. The QYx ROM trim value (also location 0xFFC0) can be calculated and programmed at the factory only. The QYx ROM order form is used to select the frequency and voltage to which this trim value is correlated.

In both cases, when the internal oscillator is used, the trim value stored in location 0xFFC0 must be loaded via software to the OSCTRIM register upon initialization.

3 Code Changes Checklist

Below is a checklist to review during the conversion process. This checklist points out all the issues that must be addressed as the code is ported from QYxA to QYx ROM.

- Does the application use the internal oscillator?

  If so, the ICFS bits in the oscillator status and control register (OSCSC) must be written to by the software for the desired setting because the POR default values differ between the QYxA and the QYx ROM.

  When using the internal oscillator, the desired trim value also needs to be selected on the ROM order form.
- Does the application use the 3 V LVI reset?

  If so, the 3 V LVI reset setting on QYxA now configures a 2 V LVI on QYx ROM. If this is not acceptable for the application, a software LVI can be created. An explanation on how this is done can be found in “On-Chip System Protection Basics for Automotive HCS08 Microcontrollers” (document number AN3305).

4 Development Tools

Development hardware used for QYxA can be used with ROM QYx. The ROM QYx is pin-for-pin compatible with QYxA and can be placed on existing QYxA hardware.

Because the QYxA is register compatible with the QYx ROM, the same project used for the QYxA may be used when creating submission code for the QYx ROM.

For in-circuit debugging, existing Cyclone/Multilink tools and associated hardware can be used. Emulation can be achieved by using the EML08QCBLTYE.

5 Differences in Packaging

All ROM QYx packages are lead free. All packages the QYxA supports are not supported by the ROM QYx. The ROM QYx supports the 8-pin SOIC package, the 16-pin SOIC, and the 16-pin TSSOP.

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