Mask Set Errata 1

68HC908MR24 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the analog-to-digital converter (ADC) and the low-voltage inhibit (LVI) applicable to this 68HC908MR24 MCU mask set device:

- 1J37F

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 3H62A. Slight variations to the mask set identification code may result in an altered version number, for example 4H62A.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “9115” indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

MSE Published Date: 4/7/99

A/D RETURNS INCORRECT CONVERSION VALUE

Starting a new analog-to-digital (A/D) conversion while the A/D is performing a conversion can cause an error which will result in the value of the current conversion being returned as 511 decimal, regardless of which channel is being used or the magnitude of the voltage on that channel.

The error will occur if the new conversion is started in the 15th or 16th A/D cycle of the current conversion.

A new A/D conversion is started on any write to the A/D status and control register (ADSCR). Setting the ADCO bit in the ADSCR to a 1 will place the A/D in continuous conversion mode; setting ADCO to 0 will cause a single conversion to occur.

To prevent this error from affecting system operation, if continuous conversion mode of operation is used and writes to the ADSCR occur, the result of the next conversion should be ignored. If continuous conversion is not enabled, an A/D conversion should be allowed to complete before writing to ADSCR.

LVI TRIP POINT SELECTION

The LVI (low-voltage inhibit) module will not provide a consistent trip point. It is recommended that the LVI be disabled on this mask set by setting LVIPWR (bit 2) to a 0 in the MOR (mask option register) (address $1F).

Additional mask set erratas can be found on the World Wide Web at www.mcu.motsps.com/lit/errata/index.html.

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