Mask Set Errata 4
M68HC912D60 Microcontroller Unit

INTRODUCTION

This mask-set errata provides information pertaining to the following 68HC912D60 MCU mask set devices:

- 4F73K, available from January 1999.

Some items do not report bugs but only contain customer information.

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter, for example F74B. Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code, for example 0F74B.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code “9115” would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC, PC, ZC or XC prefix. An SC, PC or ZC prefix denotes special/custom device. An XC prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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ATD: CONVERSION OF THE (VRH-VRL)/2 INTERNAL REF VOLTAGE RETURNS $7F, $80 OR $81 AR311

The (VRH-VRL)/2 internal reference conversion result may be $7F, $80 or $81.

Work-around If the (VRH-VRL)/2 internal reference is used (perhaps for system diagnostics), expected pass result may be $7F, $80 or $81.

BDM: CLKSW IS CLEARED BY FIRMWARE AR461

This is primarily an issue only for developers of BDM interface equipment (BDM pods). The BDM logic was changed to allow switching between XTAL/2 and a possibly faster bus rate clock. If you set the CLKSW bit (faster bus rate clock) in the BDM STATUS register (with a WRITE_BD_BYTE @ FF01 command, and then later send a GO, TRACE1, or TAG_GO command (or encounter a $00 opcode with ENBDM=0), the CLKSW bit is cleared by BDM firmware such that the BDM speed switches back to the default (XTAL/2) rate.

Work-around When communicating at the bus rate (CLKSW=1), issue a new WRITE_BD_BYTE command (at the XTAL/2 rate) to set the CLKSW bit in BDM_STATUS after any GO, TRACE1, or TAG_GO command or if BDM communications fail unexpectedly.

BDM: FAILURE TO RELEASE ADDRESS BUS AFTER MEMORY ACCESS AR538

When the BDM module is using XTAL/2 as its reference clock and the PLL is providing the clock for the CPU buses, a BDM logic circuit can fail to release control of the address bus after completing a memory access. When the next BDM serial command is completed, the BDM gives up control of the address bus, but by this time the CPU is already lost. This often results in the CPU eventually reaching a $00 opcode and getting into active BDM mode.

Work-around The error can be avoided if the BDM operates from the same clock source as the bus. Everything works after reset because both the BDM and the bus use XTAL/2 as the clock source. If the CLKSW bit is changed to one before engaging the PLL, the system also works (although the host must change communication speed to match the bus frequency changes).

In some systems the PLL is turned on and off and the bus frequency can be changed at random intervals and there is no practical way for a host to track these changes without access to the E-clock frequency. In these systems there is no workaround.

BDM AR572

When the BDM module is using synchronized XTAL/2 (CLKSW=0) as its reference clock and the PLL is providing the clock for the CPU bus (BCSP=1), data cannot be read back correctly through the BDM. The chance of reading wrong data increases when the bus frequency increases (with different PLL prescaler). All data read will not be correct when the Bus frequency is near four times the XTAL frequency. READ_W will return the requested address as data. READ_B will return the upper and lower byte of address if the requested address is even and odd respectively. Write through BDM is normal.

Work-around No customer workaround is available for this clock selection. However, CLKSW=0, BCSP=0 (Supported by all bdm i/f software) and CLKSW=1, BCSP=1 (support is unknown) combination are still ok.

BDM:

It is possible to lose BDM communication when executing long instructions, 11 cycles or more (IDIV, FDIV, EMACS, EDIVS, IDIVS), if the PLL is being used as the SYSCLK source.

Work-around Do not use the PLL as SYSCLK source when using the BDM interface to debug code that uses instructions taking ≥ 11 cycles, or insert a breakpoint before such an instruction and single step over it before continuing code execution.

BKP: ADDRESS AND DATA REGISTERS RESET ONLY ON POR AR463

Breakpoint Address and Data registers are properly reset only upon Power on Reset.

Work-around To ensure BRKAH, BRKAL, BRKDH and BRKDL registers have the correct default values, always clear each immediately after reset.

CGM: CPU STOPS GOING INTO WAIT BEFORE STRETCHED CYCLE IS FINISHED AR475

When the device exits WAIT mode, it does not return to the correct location within the routine if the stack is positioned in external memory and if the stretch bits have been enabled to lengthen the clock.

Work-around To overcome this problem, locate the stack in internal RAM resources and/or clear the stretch bits to prevent clock stretching.

CGM: CRYSTAL START-UP WITHOUT DELAY AT CLOCK MONITOR RESET AR509

When a clock monitor reset occurs, the crystal may start-up with no delay period. As a result, the MCU attempts to fetch reset vectors before the crystal has fully stabilized.

Work-around

When clock monitor failure has occurred, hold the reset signal until the crystal has reached stable oscillation.

In some applications the clock monitor reset is used to detect an accidental crystal clock loss. An alternative solution is to engage the PLL and enable the limp-home mode. As the limp-home mode is enabled, the clock monitor will not reset the MCU (NOLHM =0 in PLLCR). In case of clock loss, the limp-home mode will be engaged.

If the crystal clock is restored, the PLL will be automatically re-engaged. As the transition from PLL to limp-home and vice versa is smooth, the CPU will continue to run the code even if the crystal oscillation amplitude is not fully stabilized.

The LHIF flag in PLLFLG is set when MCU enters or exits the limp-home condition.

CGM: CANNOT INTERRUPT OUT OF STOP WITH DLY=1 AR565

STOP mode cannot be exited using interrupts when DLY=1 depending on where the Real-Time-Interrupt (RTI) counter is when the STOP instruction is executed. The RTI counter is free-running during normal operation and is only reset at the beginning of Reset, during Power-on-Reset, and after entry into STOP. The free-running counter will generate a one cycle pulse every 4096 cycles. If that pulse occurs at the exact same time that the stop signal from the CPU is asserted then the OSC is stopped but the internal stop signal will remain low. In this state the OSC is shut off until RESET.

Work-around

1. If you are not using the Real Time Interrupt function you can wait for a RTI flag before entering into STOP to guarantee the counter is in a safe state. When executing the following code all interrupt sources except for those used to exit STOP mode must be masked to prevent a loss of synchronization.
   A loss of synchronization can occur if an interrupt is processed between the setting of the RTIF and the execution of the STOP instruction. Also, you must enable the RTI counter in the initialization code, set to the fastest RTI time-out period, and the RTIE bit should NOT be set.

```
        BRCLRRTIFLG,#RTIF,RTIFClr; RTIF flag is already clear
        LDAB#RTIF; if it's set, clear the flag.
        STABRTIFLG
RTIFClr:BRCLRRTIFLG,#RTIF,*; wait until the RTIFLG is set.
        NOP
        NOP
        NOP
        STOP   ; enter stop mode
```

2. If you are driving a clock in (not using the OSC) then you could set DLY=0.
3. Pseudo-STOP and DLY=0 could be used. The oscillator will be kept alive during STOP at the expense of power consumption but no recovery delay is needed. Set the PSTP bit and clear DLY bit prior to going to STOP.
4. Limp Home and DLY=0 could be used. The part comes out of STOP in limp home mode while the crystal recovers. If a known frequency is not a requirement, this workaround avoids having the crystal alive in STOP mode. Clear the NOLHM and DLY bits prior to going to STOP.

CGM: OSCILLATOR START-UP WITH 8MHZ AND 16MHZ CRYSTALS AND RESONATORS AR536

It is possible that oscillator start up will fail with high frequency crystals and resonators under specific environmental conditions where moisture forms on the pins of the MCU, creating a leakage path to Vss or Vdd.

Typical conditions for failure are the following: 8Mhz or higher frequency crystal or resonator and leakage on the EXTAL pin to Vss corresponding to an impedance of 8M ohms.

No failures have been observed with moisture affecting oscillator start-up with resonators or crystals at or below 4Mhz frequency. Once started, the oscillation is not affected by moisture. The issue is only related to oscillator start-up.

Work-around

Conformal coating (water repellent or sealant) is required across the oscillator components and oscillator pins of the MCU where there is a possibility of the leakage paths described above.

The most critical area is around the EXTAL pin of the MCU where it is more likely to have a small spacing between EXTAL exposed tracks and low voltage sources. In particular the EXTAL and RESET pins are next to each other. At Power-on, the RESET pin is held to Vss in most systems and may be the most likely leakage path if condensation forms on the MCU pins.

CGM: STOP DOES NOT TAKE TIME-OUT WHEN RESET CAUSES THE RELEASE AR431

When coming out of STOP by using reset, the crystal start-up delay time-out does not occur. This means the MCU may be attempting to run before the crystal has become stable.

Work-around When coming out of STOP with reset, hold the reset signal until the crystal has reached a stable oscillation.

CGM: CRYSTAL OPERATION AR593

The variation of operational parameters within a given crystal part number may include a distribution of parts that present impedance conditions at start-up that will not function with the current design of the CGM. While typical parts may function correctly, problems may be seen in actual production runs.

Work-around Quartz crystal operation should be restricted to maximum 8MHz.

1. Use 8MHz (or slower) oscillator and generate higher bus frequencies using the PLL module.
2. Use alternative ceramic resonator.
3. Where mimimal clock jitter is critical, use external ’brick’ quartz oscillator module.

FLASH: CANNOT BE PROGRAMMED RELIABLY AT HIGH TEMPERATURES AR469

Work-around To enhance Flash programming reliability at elevated temperatures, the Flash bulk erase pulse time (Tepulse) should be reduced from 90-110ms to 5-10ms.

INT: EDGE SENSITIVE IRQ DOES NOT WORK CORRECTLY DURING STOP AR528

When using an edge sensitive IRQ signal to trigger an interrupt service routine and the IRQ is not released during servicing, the part will not enter stop mode if the following executed instruction is STOP.

Work-around

When IRQ is set to be edge sensitive, release pin before executing STOP instruction.

Wait until the transmit buffer is empty (TDRE == 1) and then disable the transmission (Set TE == 0).

INT: WAIT CANNOT BE EXITED IF XIRQ/IRQ LEVEL DEASSERTION OCCURS WITHIN PARTICULAR WINDOW OF TIME AR600

The device can get trapped in WAIT mode if, on exiting the WAIT instruction, the deassertion timing of the XIRQ or level-sensitive IRQ occurs within a particular timeframe. Only reset will allow recovery. Noise/bounce on the pins could also cause this problem.

Work-around

1. Use edge-triggered IRQ (IRQE=1) instead of XIRQ or level-triggered IRQ.
2. Use RTI , timer interrupts, KWU or other interrupts (except level-sensitive IRQ or XIRQ) to exit WAIT. If using RTI, it must be enabled in WAIT (RSWAI=0) and the COP must be disabled (CME=0).
3. Assert XIRQ or level-sensitive IRQ until the interrupt subroutine is entered.
4. Add de-bouncing logic to prevent inadvertent highs when exiting WAIT.

INT: DISABLING INTERRUPT WITH I MASK BIT CLEAR CAN CAUSE SWI AR527

If the source of an interrupt is taken away by disabling the interrupt without setting the I mask bit in the CCR, an SWI interrupt may be fetched instead of the vector for the interrupt source that was disabled.

Work-around

Before disabling an interrupt using a local interrupt control bit, set the I mask bit in the CCR.

IOB: AR510

Expanded mode operation causes an increase in bus driver shoot through current pin leakage which can cause inaccurate A/D conversions.

Work around

Enabling reduced drive on Ports A, B and E while the device is in expanded mode reduces the amoun t of VDD/VSS noise caused by bus driver shoot through current. Therefore, the A/D accuracy meets specified limits.

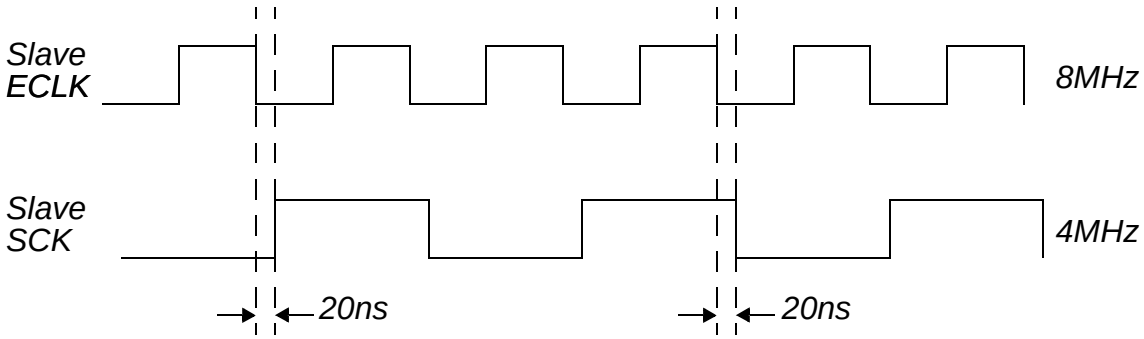
KWU: FILTER MAY NOT PREVENT PULSES SHORTER THAN 2µS FROM WAKING THE PART FROM STOP AR578

The key wake up filter may not prevent pulses shorter than 2µs from waking the part from STOP.

SPI: SPIF FLAG IS NOT SET WHEN OPERATING IN SLAVE MODE AR568

If the SPI on the HC912D60 is operated in slave mode, the SPIF flag is occasionally not set when valid data is received. The failing condition only occurs if the slave node's ECLK signals falling edge leads the SPI's incoming SCK signal by a specific phase difference.

NOTE: *The failure is very rare and has only been witnessed when the slaves ECLK falling edge leads the SCK by (20nS ± 4nS). The failure never occurs if the SPI is operated as the master. The diagram below shows an example of the timing relationship when the failure occurs.*



Work-around

1. Only use the SPI in slave mode if there is a fixed clock phase relationship between the master and slave clocks, avoiding the above scenario.

OR

2. Implement a software timeout to gate reception of data. May require use of additional I/O for handshaking.

GPIO: FUNCTION CANNOT BE RE-ENABLED ON TX PIN IMMEDIATELY AR571

The Tx pin cannot be changed to GPIO immediately. The GPIO function will become enabled only after the current transmission is complete.

Work-around

Wait until the trasmit buffer is empty (TDRE == 1) and then disable the transmission (Set TE == 0) while transmission is in progress.

ESD: ELECTROSTATIC DISCHARGE PERFORMANCE

The 68HC912D60 (4F73K) passes AEC ESD only upto and including the following voltages:

- 1000V Human Body Model
- 100V Machine Model

PLL: LIMP HOME MODE AR627

The device can prematurely indicate that the oscillator has stabilized releasing the part from Limp Home clock mode to the oscillator clock mode with an unstable oscillator. This can cause unpredictable behavior of the MCU. This situation can arise with short external power-on reset periods and / or crystal oscillator circuits that exhibit slow startup characteristics. If the PLL is not being used (Vddpll connected to Vss) Limp Home mode is disabled and this issue does not apply.

All customers should review any applications based on the referenced devices. If the crystal clock is stabilized before the external RESET line is released and the customer is not using stop mode (pseudo-stop is not affected) then there is no problem. If the clock is not stable when external RESET is released then they should contact Motorola for consultation.

Common practice for the start up mode of operation of HC12 microcontrollers is for the external RESET line to be held active until such time as the crystal has stabilized at its operating frequency. On release of the external RESET line and when the WCR (counter register) reaches a count of 4096 cycles, normal operating mode is entered with the CPU clocked from the crystal frequency (see fig. 1).

The HC12 mode of operation known as Limp-Home Mode (LHM) is enabled when the VDDPLL pin is at VDD and is entered if for any reason the external crystal ceases to oscillate. During this mode the CPU will be clocked from the free-running VCO clock of the PLL (at a nominal frequency of 1MHz). If LHM is enabled during the start-up phase (i.e. VDDPLL=5V, NOLHM bit=0) and the external RESET line is not held active until after the crystal frequency is stable then the device starts up

in LHM since no crystal oscillations will be detected. This situation can arise with short reset periods and/or crystals that exhibit slow start-up characteristics.

For the first 4096 cycles i.e. during the internal reset period, Limp Home mode will be de-asserted if oscillator activity is detected by the clock monitor circuit -due to the asserted Reset signal there can be no CPU activity during the Reset phase. Following release of the external or internal POR RESET in LHM (which ever is later) the crystal oscillator is sampled by the clock monitor circuit after another 4096 VCO clock cycles and at intervals of 8192 clock cycles thereafter until the crystal is deemed to be operating. If the crystal oscillator is showing activity at the time it is checked then it will be deemed to be good, even though it may not have fully stabilized, and LHM will be de-asserted. This can cause the device to switch from LH mode to normal mode with the CPU clocked from an unstable signal from the crystal oscillator (see fig. 2) resulting in unpredictable function of the CPU.

The COP Reset doesn't exhibit this behavior as, although the same reset sequence is followed, the oscillator isn't stopped.

When exiting Stop mode (DLY=1) a similar 4096 cycle delay is executed and therefore this behavior could also show up at this time. In applications where this is likely to be an issue, using pseudo-stop is recommended as an alternative. Current draw will increase <100 ?A at 4MHz in pseudo stop versus stop mode.

Following a loss of external clock in normal operation, Limp Home mode will be entered successfully but if the oscillator is reconnected for some reason a similar situation may arise.

The Reset condition can be overcome by allowing the crystal oscillator circuit to stabilize before releasing the external RESET line (see fig. 3). Operation is similar to that shown in fig 2.

To determine if crystal is 'stable' at the release of reset can be difficult and the time can vary some from board to board. If the customer has special high impedance probes, it is possible to monitor the amplitude of the voltage from XTAL to ground (<2 pF scope probes are recommended). Please note that any loading on the circuit can affect its operation. (Any resistance to ground or Vdd on the EXTAL pin can greatly attenuate the amplifier gain and cause erroneous operation.)

A second way to measure the oscillator startup time is to monitor the XFC pin. This method does not require a high impedance scope probe. The PLL will not lock until the oscillator clock feeding it is present and stable. Remove the external reset circuit and during power up watch the XFC pin. The voltage should start high (Vdd). After the part releases internal reset it will drop to some stable voltage between Vdd and Vss. If external reset (measured independent from this test) is held till this 'stable voltage' time the oscillator will be stable. Please note the filter components mounted on the XFC pin will affect this ramp (for evaluation purposes, alternative components can be selected to provide a fast lock time). More than one board should be measured because of pcb and crystal variability. It is also recommended that the test be run over the operating temperature of the device.

Lastly, an alternative and simpler approach is to just hold reset low for a substantial time (> 100 milliseconds) after Vdd has reached the operating voltage range.

In some applications it may be possible avoid this issue by delaying the connection of Vddpll to Vdd until the device has exited reset. This will sacrifice the limp home mode safety function upon startup, i.e. the part will no longer be able to start without a functioning crystal. A similar technique (disable PLL under software control) can be used to overcome the limitations of Stop mode.

Limp-Home mode start-up issue

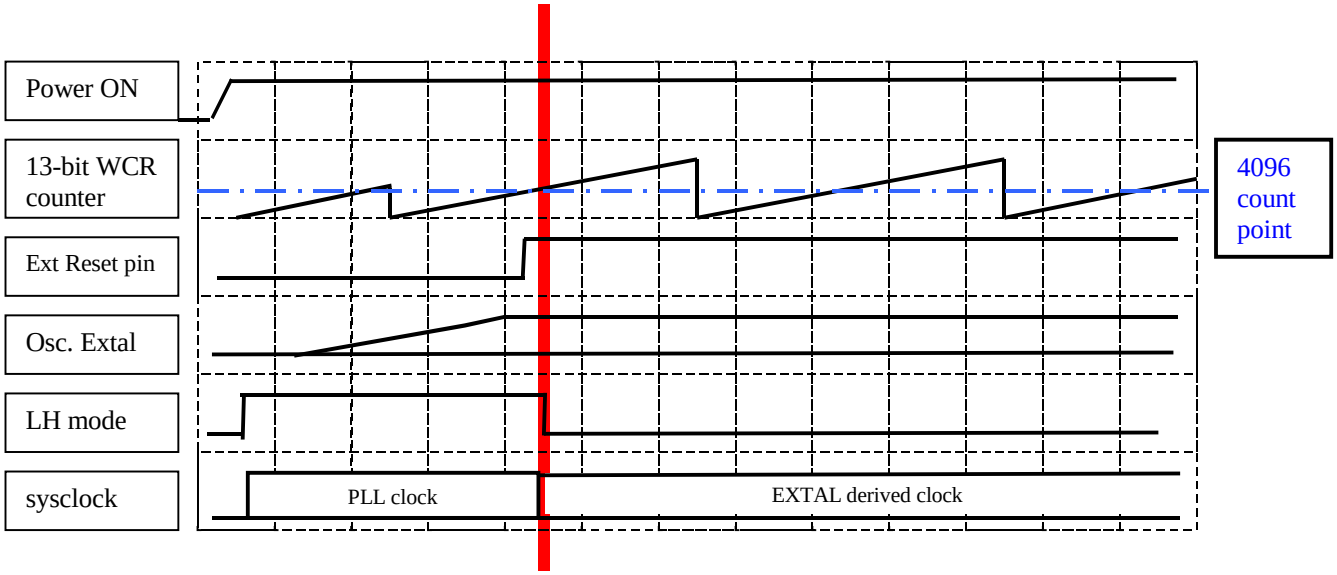


Figure 1. Representation of Normal start-up condition

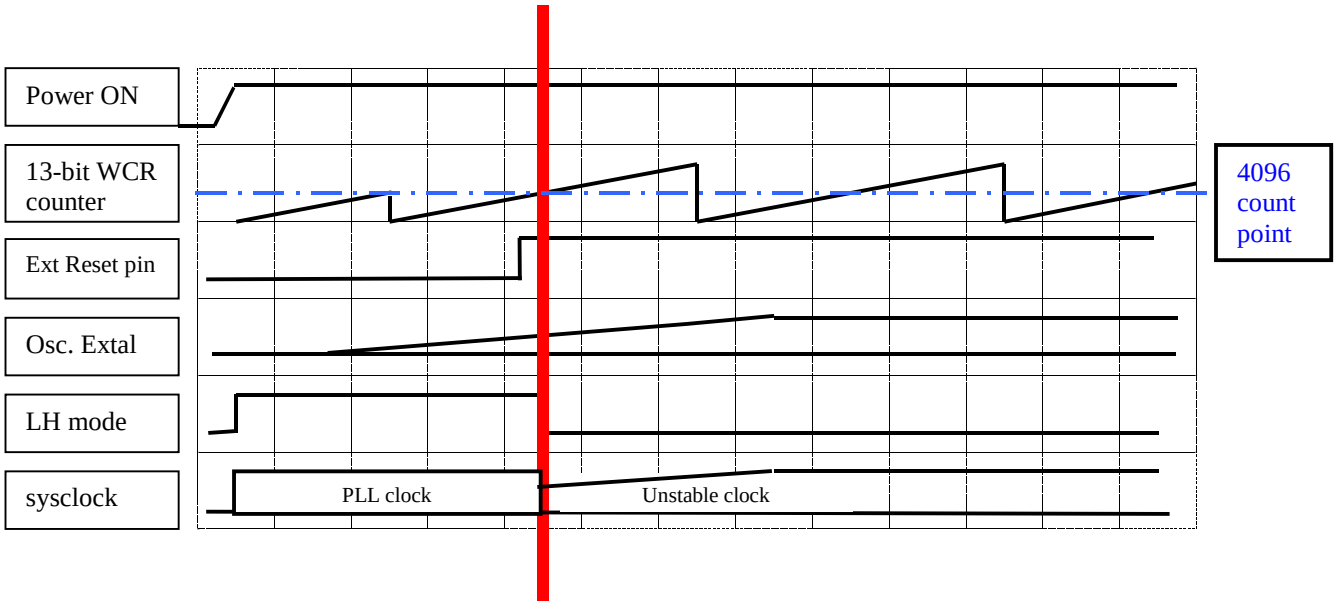


Figure 2. Representation of unreliable start-up mode with slow crystal

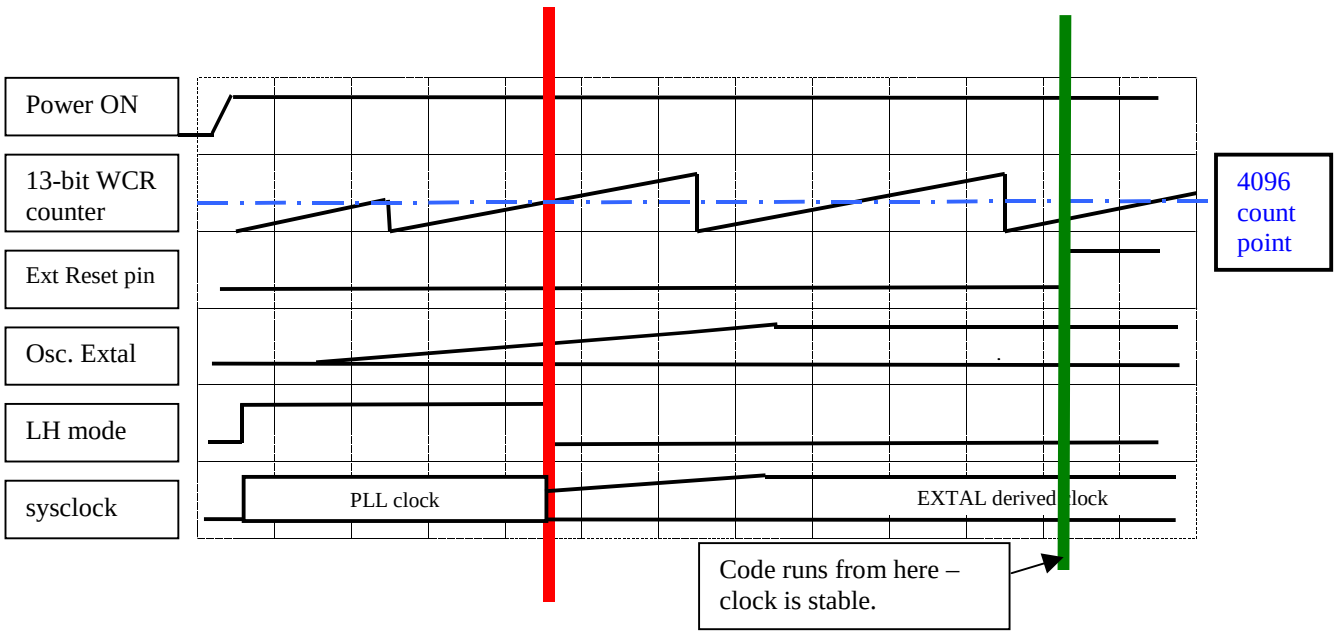


Figure 3. Representation of preferred means of overcoming issue with Figure 2

Additional mask set errata can be found on the World Wide Web at http://www.mcu.motsps.com/documentation/index.html