MOTOROLA

Chip Errata
DSP56156 Digital Signal Processor
Mask: E25H

ERRATA

Errata Description	Applies to Mask
1. There are three speed grades of the E25H silicon of the DSP56156: 40 MHz, 50 MHz and 60 MHz. These three speed grades are tested as shown in the table below.	D13N E69A E25H

Table 1: E25H Marking and Testing Conditions

Characteristic	Symbol	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Supply Voltage	V_{CC}	4.75	5.25	4.75	5.25	4.75	5.25	V
Junction Temperature	T_J	—	115	—	115	—	115	°C

The PLL is functional and tested at 60 MHz for the speed grades.

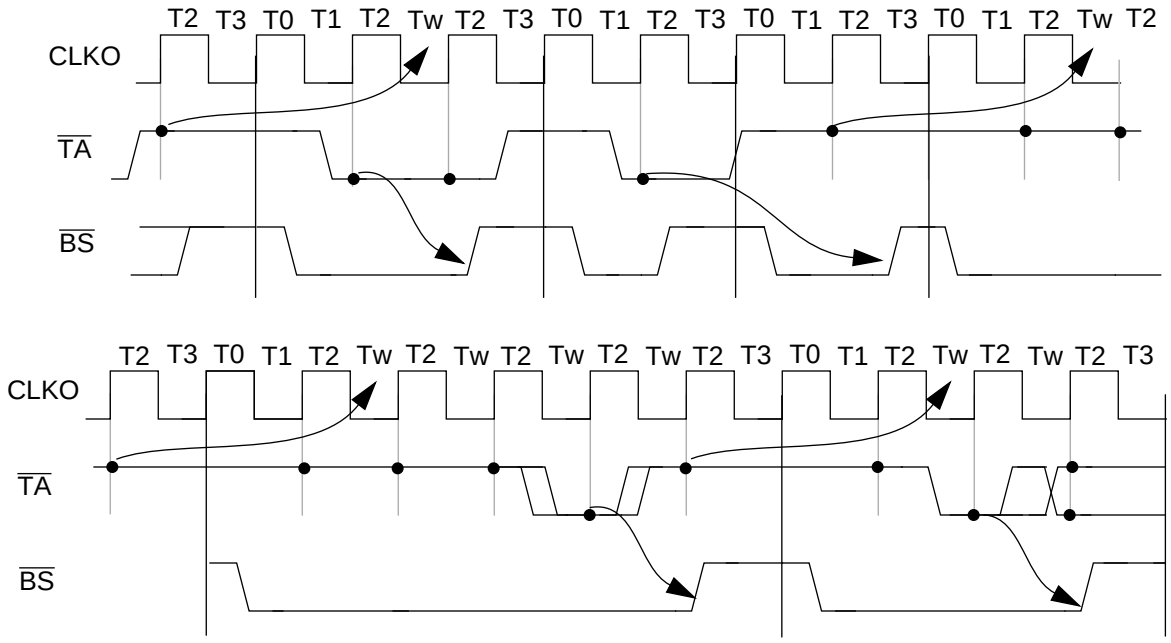
The codec is functional and tested with a 20 MHz external clock, 0 dB gain on the A/D input and D/A output, 128 decimation ratio. The A/D is tested with a 0.4 Vrms signal at 1.5 KHz and the D/A with a digitally generated sine wave 50% full scale at 2 KHz. Under those conditions, the SNR and THD of the A/D and D/A are better than 60 dB.

2. The $\overline{TA}$ pin behavior of this mask set (as well as all previous mask sets) does not match the $\overline{TA}$ definition described in the DSP56156 data sheet (2/1/92). The $\overline{TA}$ behavior is described below; it will be changed to the behavior described in the data sheet in a later revision of the silicon:	D13N D89T E69A E25H

Applies to Mask

Errata Description

$\overline{TA}$ (Transfer Acknowledge) - active low input. If there is no external bus activity, the $\overline{TA}$ input is ignored by the DSP. When there is external bus cycle activity, $\overline{TA}$ can be used to insert wait states in the external bus cycle. $\overline{TA}$ is sampled on the leading edge of T2. Any number of wait states from 1 to infinity may be inserted by using $\overline{TA}$. If $\overline{TA}$ is sampled high one clock period before the beginning of a bus cycle, at least one wait states will be inserted in the bus cycle. The bus cycle will end 4T after the $\overline{TA}$ has been sampled low on a leading edge of the clock, if the Bus Control Register (BCR) value does not program more wait states. The number of wait states is determined by the $\overline{TA}$ input or by the BCR, whichever is longer. $\overline{TA}$ is still sampled during the leading edge of the clock when wait states are controlled by the BCR value. In that case, $\overline{TA}$ will have to be sampled low during the leading edge of the last wait state programmed by the BCR (4T before the end of the bus cycle programmed by the BCR) in order not to add any wait states. If $\overline{TA}$ is sampled low (asserted) at the leading edge of T2 preceding the bus cycle, and if no wait states are specified in the BCR register, zero wait states will be inserted in the external bus cycle.



$\overline{TA}$ Controlled Accesses

3. At higher voltages, the TFS bit in the SSI's status register will not be set under all conditions when it would normally be set. The actual voltage at where this failure occurs is process dependent, and can fail at voltages as low as 4.7 V and above, depending on the processing. This failure is independent of temperature and frequency. — D13N, D89T, E69A, E25H

Errata Description	Applies to Mask
4. The $\overline{BS}$ signal is being deasserted before $\overline{TA}$ is deasserted if the BCR is programmed for one or more wait states. In this case, the $\overline{BS}$ signal ignores the $\overline{TA}$ signal and is deasserted under control of the BCR even though $\overline{TA}$ is still active and should cause $\overline{BS}$ to remain active. This problem occurs at: f_{OSC} = 60 MHz, $T_J \geq 25$ °C, $V_{CC} \leq 5$ V This problem has not been reported on parts rated at less than 60 MHz, although it has been seen at 50 MHz at 5 V and may be appear at other speeds. The temporary solution is to use either the BCR register or the $\overline{TA}$ signal to insert wait states but not both.	D13N D89T E69A E25H F44E E98S
5. The lock bit detection circuitry in the PLL fails to operate correctly in an overdamped system. A work around is to use a smaller capacitance value for the SXFC capacitor to GND. However reducing this capacitor value will increase PLL jitter. If jitter is found to be unacceptable then it is recommened to switch to a larger capacitance once the lock bit has been asserted. If this (hardware) fix cannot be done then the operating software for the device must be changed from a polling technique on the lock bit to simply waiting for 5mS for the PLL to lock before enabling the PLL to the core.	D13N D89T E69A E25H F44E E98S

NOTES

1. An over-bar (i.e. $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56156 mask numbers apply.
3. Manuals and data sheets may also have errata that is documented on the appropriate errata sheet as discovered.

-end-