MOTOROLA

Chip Errata
DSP56156 Digital Signal Processor
Mask: E98S/F44E/G68P

ERRATA

Errata Description	Applies to Mask
1. Description: There are three speed grades of the E98S / F44E / G68P silicon of the DSP56156: 40 MHz, 50 MHz, and 60 MHz. These three speed grades are tested as shown in the table below.	E98S F44E G68P

Table 1 E98S/F44E/G68P Marking and Testing Conditions

Characteristic	Symbol	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Supply Voltage	V_{CC}	4.75	5.25	4.75	5.25	4.75	5.25	V
Junction Temperature	T_J	—	115	—	115	—	115	°C

The PLL is functional and tested at 60 MHz for the speed grades.

The codec is functional and tested with a 20 MHz external clock, 0 dB gain on the A / D input and D / A output, and 128 decimation ratio. The A / D is tested with a 0.4 Vrms signal at 1.5 KHz and the D / A with a digitally generated sine wave 50% full scale at 2 KHz. Under those conditions, the SNR and THD of the A / D and D / A are better than 65 dB.

2. Description: The $\overline{BS}$ signal is being deasserted before $\overline{TA}$ is deasserted if the BCR is programmed for one or more wait states. In this case, the $\overline{BS}$ signal ignores the $\overline{TA}$ signal and is deasserted under control of the BCR even though $\overline{TA}$ is still active and should cause $\overline{BS}$ to remain active. This problem occurs at: $f_{OSC} = 60$ MHz $T_J \geq 25$ °C $V_{CC} \geq 5$ V This problem has not been fully characterized. Although it has not been reported on parts rated at less than 60 MHz, it has been seen at 50 MHz at 5 V and may be appear at other speeds. Workaround: Insert wait states using either the BCR or the $\overline{TA}$ signal, but not both.	E98S F44E G68P

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Errata Description	Applies to Mask
3. Description: The lock bit detection circuitry in the PLL fails to operate correctly in an overdamped system. Workaround: Use a smaller value capacitor for the SXFC capacitor connection to GND. However, reducing this capacitor value increases PLL jitter. If the resulting jitter level is unacceptable, then switch to a larger capacitor once the lock bit has been asserted. The table below lists the recommended SXFC capacitor values to utilize the lock bit detection circuitry. **Table 2 SXFC Size** If this second (hardware) fix is not possible within specific design constraints, then, instead of using the operating software to poll the lock bit, insert a simple 5 ms wait into the operating software to allow the PLL to lock before enabling the PLL to the core.	E98S F44E G68P

Mask	Recommended Value
E98S	680 pF
F44E	680 pF
G68P	**390 pF**

NOTES

1. An over-bar (i.e., $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56156 mask numbers apply.

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