ERRATA

DATE: February 9, 2009

PRODUCT GROUP: MCO

PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

Summary of Errata

This Errata supersedes all previous errata for this product, and assumes you have the latest versions of the Data Sheet and User's Guide, available at www.nxp.com. For detailed descriptions, please see the following pages.

Key to Status: √ = Erratum/documentation fixed in this version of silicon
I = Under Investigation
S = Specification Change
o = Erratum (work around available)
● = Erratum (no work around available)

ERRATA NUMBER	BLOCK	SUMMARY	STATUS	
			A0	A1
524-525-BOOT-01	Boot Controller	The Boot Controller cannot boot from I^2C or UART in Version A.0 silicon	●	√
524-525-LCD-01A	Color LCD Controller	Some STN LCD data bits unavailable on A.0 silicon (LH79524 only)	**o**	√
524-525-LCD-01B		Some STN LCD data bits unavailable on A.0 silicon (LH79525 only)	**o**	√
524-525-DOC-01	Documentation	Four pins are mislabeled in 6-15-05 Data Sheet	√	√
524-525-DOC-02		TEST2 pin function incorrect in 6-15-05 Data Sheet	√	√
524-525-EMC-01	External Memory Controller	Minimum SDRAM data input hold time (tIHD) specification not met with A.0 silicon	**o**	√
524-525-RCPC-01	RCPC	The internal lock signal for the main system PLL may show 'loss-of-lock' condition	**o**	**o**
524-525-USB-01	USB Device	USB Controller can lose data if interrupted during DMA transfer	**o**	√
524-525-USB-02		Start of AHB DMA burst at 1KB address boundary function	**o**	√
524-525-USB-03		EOP state slightly early in USB Controller Signal Quality Tests	**o**	√
524-525-USB-04		Only DMA Mode 0 available to the USB Controller on Version A.0 silicon	**o**	√
524-525-USB-05		Interrupt not generated at completion of a DMA transfer when last packet is of size MAXP-1	**o**	√
524-525-USB-06		End Point FIFO addresses incorrect in User's Guide	√	√

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

Boot Controller

524-525-BOOT-01 The Boot Controller cannot boot from I^2C or UART in A.0 silicon

DESCRIPTION: Cannot boot from I^2C or UART in A.0 silicon. Booting from NAND or NOR Flash works properly.

WORK AROUND: Use NAND or NOR Flash only for booting from external memory in Version A.0 silicon.

SOLUTION: Version A.1 silicon will function properly when booting from I^2C and UART, as well as NAND or NOR Flash.

NOTE: A.0 silicon (only), when booting from NAND Flash devices, it supports small block devices using sequential page read operations.

Color LCD Controller

524-525-LCD-01A Some STN LCD data bits unavailable on A.0 silicon (LH79524 only)

DESCRIPTION: Several LCD data bits are not pinned out, resulting in certain STN signals not being available. Table 1 shows the pinouts for Version A.0 silicon. The LH79524 is missing signals MUSTN6/CUSTN6 and MLSTN4/CLSTN4. This erratum applies only to Version A.0 silicon and only to the LH79524.

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):		
X	Silicon	LH79524/LH79525 version A.0, version A.1
X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
	Other	

DESCRIPTION

Table 1: LH79524 LCD Data Multiplexing for Version A.0 Silicon

CABGA BALL NO.	CABGA BALL NAME	STN						TFT
		MONO 4-BIT		MONO 8-BIT		COLOR		COLOR
		SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL
C2	LCDVD15	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	INTENSITY
C1	LCDVD14	X	X	X	X	X	X	BLUE4
C10	LCDVD13	X	X	X	X	X	X	BLUE3
A10	LCDVD12	X	X	X	MLSTN7	X	CLSTN7	BLUE2
A11	LCDVD11	X	X	X	MLSTN6	X	CLSTN6	BLUE1
B10	LCDVD10	X	X	X	MLSTN5	X	CLSTN5	BLUE0
C9	LCDVD9	X	MLSTN3	X	MLSTN3	X	CLSTN3	GREEN4
B9	LCDVD8	X	MLSTN2	X	MLSTN2	X	CLSTN2	GREEN3
A9	LCDVD7	X	MLSTN1	X	MLSTN1	X	CLSTN1	GREEN2
A8	LCDVD6	X	MLSTN0	X	MLSTN0	X	CLSTN0	GREEN1
B8	LCDVD5	X	X	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN0
C8	LCDVD4	X	X	MUSTN5	MUSTN5	CUSTN5	CUSTN5	RED4
A7	LCDVD3	X	X	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED3
B7	LCDVD2	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED2
C7	LCDVD1	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED1
A6	LCDVD0	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED0

NOTES:
'X' is Don't Care
'MLSTNx' = Mono Lower panel STN data bit 'x'
'MUSTNx' = Mono Upper panel STN data bit 'x'
'CLSTNx' = Color Lower panel STN data bit 'x'
'CUSTNx' = Color Upper panel STN data bit 'x'

DATE: February 9, 2009

PRODUCT GROUP: MCO

PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

WORK AROUNDS: There are two possible work arounds:

1. Since 4-bit Mono mode works fine, the CLCDC can be programmed to operate only in 4-bit Mono mode by programming the CLCDC CTRL:MONO8L bit to 0 and then use the CLCDC with a 4-bit LCD Data Bus.
2. This work around maintains all color integrity. Since different bits are unavailable on the upper and lower panel interface, Dual-panel mode can be used with a single panel, picking up the missing MUSTN6/CUSTN6 bit using MLSTN6/CLSTN6. Follow these steps to implement this work around:
   a. Set the UPBASE and LPBASE registers to the same value. These registers contain the pointer to the top of the frame buffer. Programming both to the same value presents identical data on the upper and lower STN signals (i.e. MUSTNx = MLSTNx).
   b. Connect the CUSTNx or MUSTNx pins to the application LCD as shown in Table 2.

Table 2: LH79524 to LCD Panel Connection for Work Around

SIGNAL	LH79524 BALL	STN LCD PANEL CONNECTION
MUSTN0/CUSTN0	C2	Data 0
MUSTN1/CUSTN1	A6	Data 1
MUSTN2/CUSTN2	C7	Data 2
MUSTN3/CUSTN3	B7	Data 3
MUSTN4/CUSTN4	A7	Data 4
MUSTN5/CUSTN5	C8	Data 5
MLSTN6/CLSTN6	A11	Data 6
MUSTN7/CUSTN7	B8	Data 7

The LCD will now function with correct color rendition.The required system bandwidth will increase due to twice the number of fetches from the frame buffer.

SOLUTION: The missing bits will be pinned out in Version A.1 silicon. For reference, the connection table for Version A.1 silicon is shown in Table 3. Signals added to Version A.1 are represented by ***bold italic***.

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):		
X	Silicon	LH79524/LH79525 version A.0, version A.1
X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
	Other	

DESCRIPTION

Table 3: LH79524 LCD Data Multiplexing for Version A.1 Silicon

CABGA BALL NO.	CABGA BALL NAME	STN						TFT
		MONO 4-BIT		MONO 8-BIT		COLOR		COLOR
		SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL
C2	LCDVD15	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	INTENSITY
C1	LCDVD14	X	X	X	***MLSTN4***	X	***CLSTN4***	BLUE4
C10	LCDVD13	X	X	***MUSTN6***	***MUSTN6***	***CUSTN6***	***CUSTN6***	BLUE3
A10	LCDVD12	X	X	X	MLSTN7	X	CLSTN7	BLUE2
A11	LCDVD11	X	X	X	MLSTN6	X	CLSTN6	BLUE1
B10	LCDVD10	X	X	X	MLSTN5	X	CLSTN5	BLUE0
C9	LCDVD9	X	MLSTN3	X	MLSTN3	X	CLSTN3	GREEN4
B9	LCDVD8	X	MLSTN2	X	MLSTN2	X	CLSTN2	GREEN3
A9	LCDVD7	X	MLSTN1	X	MLSTN1	X	CLSTN1	GREEN2
A8	LCDVD6	X	MLSTN0	X	MLSTN0	X	CLSTN0	GREEN1
B8	LCDVD5	X	X	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN0
C8	LCDVD4	X	X	MUSTN5	MUSTN5	CUSTN5	CUSTN5	RED4
A7	LCDVD3	X	X	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED3
B7	LCDVD2	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED2
C7	LCDVD1	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED1
A6	LCDVD0	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED0

NOTES:
'X' is Don't Care
'MLSTNx' = Mono Lower panel STN data bit 'x'
'MUSTNx' = Mono Upper panel STN data bit 'x'
'CLSTNx' = Color Lower panel STN data bit 'x'
'CUSTNx' = Color Upper panel STN data bit 'x'

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):		
X	Silicon	LH79524/LH79525 version A.0, version A.1
X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
	Other	

DESCRIPTION

524-525-LCD-01B Some STN LCD data bits unavailable on A.0 silicon (LH79525 only)

DESCRIPTION: Several LCD data bits are not pinned out, resulting in certain STN signals not being available. Table 4 shows the pinouts for Version A.0 silicon. The LH79525 is missing signals MUSTN0 and MUSTN1. This erratum applies only to Version A.0 silicon and only to the LH79525.

Table 4: LH79525 LCD Data Multiplexing for Version A.0 Silicon

PIN NO.	PIN NAME	STN MONO 4-BIT		TFT COLOR
		SINGLE PANEL	DUAL PANEL	SINGLE PANEL
145	LCDVD11	X	X	BLUE4
146	LCDVD10	X	X	BLUE3
147	LCDVD9	X	X	BLUE2
149	LCDVD8	X	X	BLUE1
151	LCDVD7	X	MLSTN3	GREEN4
153	LCDVD6	X	MLSTN2	GREEN3
154	LCDVD5	X	MLSTN1	GREEN2
155	LCDVD4	X	MLSTN0	GREEN1
156	LCDVD3	X	X	RED4
157	LCDVD2	X	X	RED3
158	LCDVD1	MUSTN3	MUSTN3	RED2
159	LCDVD0	MUSTN2	MUSTN2	RED1

NOTES:
'X' is Don't Care
'MLSTNx' = Mono Lower panel STN data bit 'x'
'MUSTNx' = Mono Upper panel STN data bit 'x'

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):		
X	Silicon	LH79524/LH79525 version A.0, version A.1
X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
	Other	

DESCRIPTION

WORK AROUND, LH79525: The LH79525 supports only 4-bit Mono STN, so there is only one work around:

This work around maintains grayscale integrity. Since different bits are unavailable on the upper and lower panel interface, Dual-panel mode can be used with a single panel, using the MLSTNx signals.

- Set the UPBASE and LPBASE registers to the same value. These registers contain the pointer to the top of the frame buffer. Programming both to the same value presents identical data on the upper and lower STN signals (i.e. MUSTNx = MLSTNx).
- Connect the pins to the application LCD as shown Table 5.

Table 5: LH79525 to LCD Panel Connection for Work Around

SIGNAL	LH79525 PIN	STN LCD PANEL CONNECTION
MLSTN0	155	Data 0
MLSTN1	154	Data 1
MLSTN2	153	Data 2
MLSTN3	151	Data 3

The LCD will now function with correct grayscale rendition. The required processing bandwidth will increase due to twice the number of fetches from the frame buffer.

SOLUTION: The missing bits will be pinned out in Version A.1 silicon. For reference, the connection table for Version A.1 silicon is shown in Table 6. Signals added to Version A.1 are represented by ***bold italic***.

Table 6: LH79525 LCD Data Multiplexing for Version A.1 Silicon

PIN NO.	PIN NAME	STN MONO 4-BIT	
		SINGLE PANEL	DUAL PANEL
145	LCDVD11	***MUSTN1***	***MUSTN1***
146	LCDVD10	***MUSTN0***	***MUSTN0***
147	LCDVD9		
149	LCDVD8		
151	LCDVD7		MLSTN3
153	LCDVD6		MLSTN2
154	LCDVD5		MLSTN1
155	LCDVD4		MLSTN0
156	LCDVD3		
157	LCDVD2		
158	LCDVD1	MUSTN3	MUSTN3
159	LCDVD0	MUSTN2	MUSTN2

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):		
X	Silicon	LH79524/LH79525 version A.0, version A.1
X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
	Other	

DESCRIPTION

Documentation

524-525-DOC-01 Four pins are mislabeled in 6-15-05 Data Sheet

DESCRIPTION: Four pins in each the LH79524 and LH79525 pinout tables have UART0 and UART1 reversed.

WORKAROUND: The correct labels for the pins are shown in the following tables. Use these descriptions in lieu of the descriptions in the 6-15-05 (and Beta) Data Sheets.

LH79524 Data Sheet Table 1 (Corrected Pin Descriptions)

CABGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
M4	PB4/SSPRX/I2SRXD/ UARTRX1/UARTIRRX1	I/O	General Purpose I/O Signal — Port B4; multiplexed with SSP Data In, I^2S Data In, UART1 Serial Data In, and UART1 Infrared Data In
P1	PB5/SSPTX/I2STXD/ UARTTX1/UARTIRTX1	I/O	General Purpose I/O Signal — Port B5; multiplexed with SSP Data Out, I^2S Data Out, UART1 Data Out, and UART1 IR Data Out
N2	PB6/INT0/UARTRX0/ UARTIRRX0	I/O	General Purpose I/O Signal — Port B6; multiplexed with UART0 Infrared Received Serial Data Input, UART0 Received Serial Data In, and External Interrupt 0
M3	PB7/INT1/UARTTX0/ UARTIRTX0	I/O	General Purpose I/O Signal — Port B7; multiplexed with UART0 Infrared Transmitted Serial Data Output, UART0 Serial Transmit Data Out, and External Interrupt 1.

LH79524 Data Sheet Table 2 (Corrected Pin Descriptions)

CABGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
M3	PB7	INT1/UARTTX0/UARTIRTX0	8 mA	1, 6
M4	PB4	SSPRX/I2SRXD/UARTRX1/UARTIRRX1	8 mA	2
N2	PB6	INT0/UARTRX0/UARTIRRX0	8 mA	1, 6
P1	PB5	SSPTX/I2STXD/UARTTX1/UARTIRTX1	8 mA	1

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

LH79525 Data Sheet Table 4 (Corrected Pin Descriptions)

LQFP PIN	SIGNAL NAME	TYPE	DESCRIPTION
40	PB4/SSPRX/I2SRXD/ UARTRX1/UARTIRRX1	I/O	General Purpose I/O Signal — Port B4; multiplexed with SSP Data In, I^2S Data In, UART1 Serial Data In, and UART1 Infrared Data In
39	PB5/SSPTX/I2STXD/ UARTTX1/UARTIRTX1	I/O	General Purpose I/O Signal — Port B5; multiplexed with SSP Data Out, I^2S Data Out, UART1 Data Out, and UART1 IR Data Out
38	PB6/INT0/UARTRX0/ UARTIRRX0	I/O	General Purpose I/O Signal — Port B6; multiplexed with UART0 Infrared Received Serial Data Input, UART0 Received Serial Data In, and External Interrupt 0
37	PB7/INT1/UARTTX0/ UARTIRTX0	I/O	General Purpose I/O Signal — Port B7; multiplexed with UART0 Infrared Transmitted Serial Data Output, UART0 Serial Transmit Data Out, and External Interrupt 1.

LH79525 Data Sheet Table 5 (Corrected Pin Descriptions)

LQFP PIN	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
37	PB7	INT1/UARTTX0/UARTIRTX0	8 mA	1, 6
38	PB6	INT0/UARTRX0/UARTIRRX0	8 mA	1, 6
39	PB5	SSPTX/I2STXD/UARTTX1/UARTIRTX1	8 mA	1
40	PB4	SSPRX/I2SRXD/UARTRX1/UARTIRRX1	8 mA	2

SOLUTION: The Data Sheet has been revised.

524-525-DOC-02 TEST2 pin function incorrect in 6-15-05 Data Sheet

DESCRIPTION: The description of the TEST2 pin operation was incorrect in the 6-15-05 (and Beta) Data Sheet.

WORKAROUND: The 6-15-05 Data Sheet stated that TEST 2 should be tied HIGH for Normal operation and pulled LOW for embedded ICE. This is not correct. The correct operation of TEST1 and TEST2 is shown in the following table:

TEST1	Tie HIGH for Normal Operation; pull LOW to enable Embedded ICE Debugging
TEST2	Tie HIGH for Normal Operation; pull HIGH to enable Embedded ICE Debugging

SOLUTION: The Data Sheet has been updated to include the descriptions above. Also, the following table was added to ensure clarity in the use of TEST1 and TEST2: .

MODE	TEST1	TEST2	nBLE0
Embedded ICE	0	1	1
Normal	1	1	x

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

External Memory Controller

524-525-EMC-01 Minimum SDRAM data input hold time (tIHD) specification not met with A.0 silicon

DESCRIPTION: Process, temperature, and voltage testing on A.0 silicon yields an tIHD parameter of 3.7 ns (VDD = 3.3 V ± 5%) and 3.9 ns (VDD = 3.3 V ± 10%). This may be more than the hold time guaranteed by some SDRAMs.

WORKAROUND: Most systems will not require a change. The combined 'flight time' associated with SDCLK and SDRAM data (167 ps/inch for a 50 Ω trace) in most memory system implementations may be sufficient to assure correct operation.

If the flight time is insufficient to assure correct operation, the SDCLK output signal from the LH79524/525 or the SDRAM data input to the LH79524/525 should be delayed. Delay can be added using one or more series terminators, a capacitive load to the SDCLK, and/or additional trace length on the SDCLK signal.

System designers are encouraged to understand the impact of load capacitance, SDRAM data out hold times for their respective load capacitance, and PC board trace implementation to successfully achieve the minimum hold time requirement.

Example 1: A Samsung K4S161622E SDRAM was selected with a minimum 2.5 ns Data Out hold time. The SDCLK trace from the SoC to the nearest SDRAM is 6 inches long, giving a 1 ns flight time. The minimum data bit trace from the SDRAM to the SoC is 2.0 inches long. The system power supply has a maximum voltage drop of 150 mV to VDD of the SoC.

SDCLK flight time:	1.0 ns
SDRAM Minimum data output hold time:	2.5 ns
SDRAM Data Out flight time:	0.33 ns
Total minimum hold time:	3.83 ns
Minimum required hold time (VDD ±5%):	3.7 ns

No modification is required to assure correct operation. Although the margin in the calculation is very small, this simple analysis does not account for extra margin available because the minimum output hold time on the SDRAM occurs with low temperature and high voltage conditions. Under these same conditions, the hold time requirement at the input to the SoC is also smaller than the specified worst-case requirement.

Example 2: An unusually aggressive board layout has an SDCLK board trace of 4.5 inches and a minimum data signal trace length of 1.0 inch. A low cost power system has a voltage tolerance of 10% on the 3.3 V I/O supply.

SDCLK flight time:	0.75 ns
SDRAM Minimum data output hold time:	2.5 ns
SDRAM Data Out flight time:	0.17 ns
Total minimum hold time:	3.42 ns
Required hold time (VDD ±10%):	3.9 ns

The memory subsystem fails to meet the minimum timing by almost 500 ps. Adding a series termination sufficient to ensure an additional 600 ps delay to SDCLK fixes the problem. As with Example 1, there is actually more margin than this simple analysis shows as the minimum required hold time. Because of CMOS circuitry characteristics, the calculation yields its minimum value at high temperature and low voltage conditions.

SOLUTION: Data Sheet tIHD value modified to 2.0 ns. Permanent erratum for A.0 silicon; Fixed in Version A.1 and later.

DATE: February 9, 2009

PRODUCT GROUP: MCO

PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

Reset, Clock, and Power Controller

524-525-RCPC-01 The internal lock signal for the main system PLL may show 'loss-of-lock' condition

DESCRIPTION: The internal PLL Lock signal may show 'loss-of-lock' for the main system PLL on both the LH79524 and LH79525 in versions A.0 and A.1 silicon. This results in the system clock (HCLK) stalling for short periods of time. The PLL operation guarantees there will be no 'short' clocks. The SoC stops the main system clocks (HIGH or LOW state) when the loss-of-lock occurs. PLL loss-of-lock is due to noise. Noise can be generated internal to the device or from external sources, and is typically worse at extreme temperatures (hot or cold) and higher voltages.

WORK AROUND: Customers are advised to determine if their designs could suffer problems due to the very brief clock stoppages described above. There are two possible work arounds:

1. **Follow the steps outlined in a) through f) when using a crystal connected to the SoC XTALIN and XTALOUT pins. These steps help to minimize the occurrence and impact of a PLL loss-of-lock condition, but do not eliminate the possibility of it occurring.**
   a. Signal Termination: Series termination should be used for any clock signals generated by the LH79524/525, not AC termination. In general, no termination is required on clock output traces that are shorter than six inches.
   b. UARTs: The UART[2:0] clocks can be sourced from the XTAL oscillator input or the system clock (HCLK). The source clock for each of the UARTs should remain (the default) XTAL oscillator input, which does not stop. When using the XTAL oscillator clock source, data continues to be sent and received when HCLK stops. Enabling the FIFO is recommended. Clock stoppages could delay response times in servicing FIFOs and interrupts. However this is not believed to be significant in a practical system.
   c. During high speed operation, the UART clocks are sourced from HCLK. Most communications protocols using the UART interface in this mode will be capable of recovering from a lost data event.
   d. I/O Voltage: Restricting the 3.3 V I/O voltage supply to 3.3 V or lower will reduce or eliminate the occurrence of this event.
   e. Edge Sensitive External Interrupts and DMA External Request: The LH79524/525 Data Sheet specifies edge-sensitive external interrupt requests and external DMA requests (DREQn) may have pulse widths as short as one HCLK cycle. This erratum requires that pulses be not less than 30 μs, or that the level sensitive mechanism be used for external interrupts.
   f. Divisor settings: Testing has shown that some PLL divisor settings are more susceptible to this issue than others. The following values have been shown to minimize the chance of loss-of-lock for CPUCLK= 76.2 MHz, SYSCLK = 50.8 MHz:
   - SYSPLLCTL(0xfffe20C0) 0x30B6; SYSRANGE = 1, SYSPREDIV = 2, SYSLOOPDIV = 54
   - CPUCLKPRE(0xfffe201C) 0x0002
   - SYSCLKPRE(0xfffe2018) 0x0003

2. **Use an external clock source, connected to the XTALIN pin on either the SoC, and operate in the PLL Bypass Mode.**

   SOLUTION: This is a permanent erratum.

DATE: February 9, 2009
PRODUCT GROUP: MCO
PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

USB

524-525-USB-01 USB Controller can lose data if interrupted during DMA transfer

DESCRIPTION: If the USB Master, when using DMA, is interrupted in the middle of a burst to the External Memory Controller (EMC) by a higher priority master that is also accessing the EMC, data will be lost.

The USB master (DMA) uses incrementing bursts of unspecified lengths on the AHB. It is possible (due to arbitration) for a USB DMA burst to be interrupted in the middle of a transfer. This can happen when higher priority devices such as the CLCD or Ethernet Controller are requesting the AHB. If the USB Controller AHB master shares external memory space with either the CLCD or Ethernet MAC Controller, (EMAC) the possibility arises that the burst to the EMC from the USB can be interrupted by a transfer to/from the EMC by either the CLCD or EMAC. If this situation arises, the USB Controller AHB master *must* (according to AMBA) regenerate the burst according to protocol. Currently, the USB Controller AHB master does not do this and hence is not AMBA compliant.

WORK AROUND: USB DMA to and from the EMC can be used as long as no higher-priority master (i.e. EMAC, CLCD or DMA) is targeting the EMC at the same time. In addition, USB DMA to and from internal SRAM can be used with no constraints.

SOLUTION: Permanent erratum for Version A.0; Fixed in Version A.1 and later.

524-525-USB-02 Start of AHB DMA burst at 1KB address boundary function

DESCRIPTION: If the transfer of a data packet crosses a 1KB address boundary, the USB Controller AHB DMA should start a new burst. This new burst is started when a transfer size of 8 bits is used, but does not start when data sizes of 16 or 32 bits are used.

WORK AROUND: Do not use DMA or ensure that 1K boundaries are not crossed.

SOLUTION: Permanent erratum for Version A.0; Fixed in Version A.1 and later.

524-525-USB-03 EOP state slightly early in USB Controller Signal Quality Tests

DESCRIPTION: The USB Controller fails to meet timing requirements during the EOP transmission section of the Full speed Signal Quality Tests (Eye Diagram test) on the USB interface. The violation happens due to an early start of the EOP state. The EOP start is approximately 1 ns early.

WORK AROUND: Because of the infinitesimal degree of the failure, it is unlikely that it will affect transaction quality.

SOLUTION: Permanent erratum for Version A.0; Fixed in Version A.1 and later.

524-525-USB-04 Only DMA Mode 0 available to the USB Controller on Version A.0 silicon

DESCRIPTION: The AUTO_CLR bit (bit 7) of the OUTCSR2 register does not function properly. In Version A.0 there is a possibility that Auto Clear will erroneously clear the Output Packet Ready event twice, which can result in lost data.

WORK AROUND: Do not use the Auto Clear function. Instead the processor must intervene and set the output packet ready bit manually or use the DMA in Mode 0. See also the other USB errata for constraints using DMA Mode 0.

SOLUTION: Permanent erratum for Version A.0; Fixed in Version A.1 and later.

DATE: February 9, 2009

PRODUCT GROUP: MCO

PART NUMBER: LH79524/LH79525

AFFECTED ITEM(s):			
	X	Silicon	LH79524/LH79525 version A.0, version A.1
	X	Document(s)	LH79524/LH79525 Data Sheet and User's Guide (Advance)
		Other	

DESCRIPTION

524-525-USB-05 Interrupt not generated at completion of a DMA transfer when last packet is of size MAXP-1

DESCRIPTION: If the AHB DMA is being used in Mode 1 to load a bulk transfer from the USB Device, and the size of the last packet of the transfer is one byte less than MAXP (i.e. MAXP-1), no DMA interrupt will be generated when the last packet has been loaded. (MAXP is the maximum packet size, programmed in the OUTMAXP Register).

See the OUTCSR2:DMA_MODE bit description in Table 17-39 of the User's Guide for a description of Mode 1 and Mode 2.

WORK AROUND: Two workarounds exist, one using polling and one using interrupts.

POLLING: Software can poll the OUTCOUNTx Register after the transfer has been set up. When this register reaches 0, the DMA transfer has completed.

INTERRRUPT: Software can program the DMA in Mode 1 to transfer a number of MAXP sized packets. Then software can transfer the last (MAXP-1) packet using Mode 0.

SOLUTION: Permanent erratum for Version A.0; Fixed in Version A.1 and later.

524-525-USB-06 End Point FIFO addresses incorrect in User's Guide

DESCRIPTION: The End Point (EP) FIFO addresses are incorrect in Table 17-3 in the Preliminary User's Guide.

WORK AROUND: The correct EP FIFO addresses are:

ADDRESS OFFSET	NAME	DESCRIPTION
0x080	EP0FIFO	FIFO for Endpoint 0
0x090	EP1FIFO	FIFO for Endpoint 1
0x0A0	EP2FIFO	FIFO for Endpoint 2
0x0B0	EP3FIFO	FIFO for Endpoint 3

SOLUTION: Later User's Guides will contain correct addresses.