ERRATA SHEET

Date: **2009 February 23**
Document Release: **Version 1.0**
Device Affected: **LPC2158**

This errata sheet describes both the functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

NXP
Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
1.0	2009 February 23	First Version

Identification:

The LPC2158 devices typically have the following top-side marking:

LPC2158xxx

xxxxxxx

xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2158:

Revision Identifier (R)	Comment
'B'	First device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
Core.1	Incorrect update of the Abort link register	B
SSP.1	Initial data bits/clocks corrupted in SSP transmission	B

Errata Overview - AC/DC Deviations

AC/DC Deviations	Short Description	Device Revision the deviation occurs in
NA	NA	NA

Errata Notes

Notes	Short Description	Device Revision the note applies to
Note 1	Port pin P0.31 must not be driven low during reset.	B
Note 2	When the input voltage is Vi ≥ Vdd I/O + 0.5 von port pin P0.25 (configured as general purpose input pin), current must be limited to less than 4 mA by using a series limiting resistor.	B

Functional Problems of LPC2158

Core.1 **Incorrect update of the Abort Link register in Thumb state**

Introduction: If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem: In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work around: In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

SSP.1 **Initial data bits/clocks of the SSP transmission are shorter than subsequent pulses at higher frequencies**

Introduction: The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI or a Microwire bus. The SSP can operate at a maximum speed of 30MHz and it referred to as SPI1 in the device documentation.

Problem: At high SSP frequencies, it is found that the first four pulses are shorter than the subsequent pulses.

At 30MHz, the first pulse can be expected to be approximately 10ns shorter and the second pulse around 5ns shorter. The remaining two pulses are around 2ns shorter than subsequent pulses.

At 25MHz, the length of the first pulse would be around 7ns shorter. The subsequent three pulses are around 2ns shorter.

At 20MHz only the first pulse is affected and it is around 2ns shorter. All subsequent pulses are fine.

The deviation of the initial data bits/clocks will decrease as the SSP frequency decreases.

Work-around: None.

Errata Notes

Note 1: Port pin P0.31 must not be driven low during reset. If low on reset the device behaviour is undetermined.

Note 2: On port pin P0.25 (when configured as general purpose input pin), leakage current increases when the input voltage is Vi ≥ Vdd I/O + 0.5 v. Care must be taken to limit the current to less than 4 mA by using a series limiting resistor.