Document identifier: MC56F81xxx_0N91Z
Rev. 1, 6/2024

MC56F81xxx_0N91Z

Mask Set Errata

Mask Set Errata for Mask 0N91Z

Revision History

This report applies to mask 0N91Z for these products:

- MC56F81xxx

Table 1. Revision History

Revision	Date	Significant Changes
1	6/2024	The following errata were added. • ERR052089 • ERR052090 • ERR051176 • ERR051724 • ERR051374 • ERR051989 • ERR051706
0	11/2020	Initial Revision

Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR050527	ROM: After ROM execution and jumping to application, ROM does not restore PIT0 registers to reset values
ERR050631	QDC: A possible speed measurement issue when CTRL3[PMEN]=1
ERR051176	SOC: eDMA does not work as expected when the clock of the trigger source module is less than BUS_2X_CLK in fast mode
ERR051374	PWM fault may work abnormally when the fault signal is very narrow
ERR051706	The DAC output jumps to MAXVAL or MINVAL value and lasts two REFRESH clock cycles (instead of one) in the first waveform period after an active SYNC_IN signal occurs with CTRL0[ONESHOT]=0 and CTRL0[AUTO]=1 in triangle waveform mode
ERR051724	DAC output can’t reach MAXVAL or MINVAL in automatic mode when CTRL0[ONESHOT] = 1
ERR051989	PWM: output may be abnormal when the value of phase delay register is reduced from a non-zero value to 0.
ERR052089	Output signals of peripherals with BUS_2X_CLK may not be correctly recognized by peripherals with BUS_CLK
ERR052090	CPU may malfunction after a COP reset, when the chip is in the fast mode and booting from Flash

Known Errata

ERR050527: ROM: After ROM execution and jumping to application, ROM does not restore PIT0 registers to reset values

Description

When jumping from ROM to application, it is expected to restore all registers (used by ROM) to reset values. However, PIT0 registers PIT0_CTRL, PIT0_CNTR_L and PIT0_CNTR_H are not restored to their reset values.

Workaround

Set 0x0000 to PIT0_CTRL at the beginning of user's application. Since PIT0_CTRL[CNT_EN] bit is cleared, the counter registers PIT0_CNTR_L and PIT0_CNTR_H returns to 0x0000 value automatically.

ERR050631: QDC: A possible speed measurement issue when CTRL3[PMEN]=1

Description

When CTRL3[PMEN]=1, and reading POSD occurs simultaneously with any edge of phase A or phase B signal, the captured position difference value in POSDH register may not match the time period captured in POSDPERH register, which causes inaccuracy in speed measurement.

Workaround

This issue is caused by the fact that the edge of phase A and phase B are delayed 3 QDC clock cycles and then they are used to drive position counter. When reading POSD occurs simultaneously with the edge of phase A or phase B, the captured time period in POSDPERH is correct, but position counter is not increased or decreased yet, so the captured position difference value in POSDH is one count less or more than the correct value depending on the direction. To avoid such an issue, follow the steps below to get a correct position difference value:

1. Read POSD register to trigger capture of position difference and time period between each reading of POSD. Now the position difference is captured into POSDH (inaccurate value), and time period is captured into POSDPERH (accurate value).

2. Read LPOS register after 3 QDC clock cycles. Make sure it is exactly 3 QDC clock cycles between reading POSD in step 1 and reading LPOS in this step.

3. Store the value of LPOSH and UPOSH into a 32bit variable, such as u32PosCnt. Another variable u32PosCnt_1 is used to store LPOSH and UPOSH value of last time.

4. Define variable u32PosDiff = u32PosCnt- u32PosCnt_1. Now u32PosDiff represents the accurate position difference. Use u32PosDiff and the value in POSDPERH to calculate speed.

5. Update u32PosCnt_1 with the value of u32PosCnt.

Note: repeat these steps each time the speed is calculated.

ERR051176: SOC: eDMA does not work as expected when the clock of the trigger source module is less than BUS_2X_CLK in fast mode

Description

When the chip is configured in the fast mode (where CPU operates at 2x bus frequency), and the peripheral that generate the DMA request operates at 1x bus frequency, the eDMA transfer may be executed multiple times with one trigger due to the signal used to clear the DMA request misaligns to the bus clock.

Workaround

The workaround is to clear the eDMA request flag manually, as the following steps.

1. Configure the source triggered eDMA channel to transfer the request flag clear message.

2. Enable channel link in both minor loop and major loop by setting CITER_ELINKYES[ELINK] and CSR[MAJORELINK], and configure the linked channel number via CITER_ELINKYES[LINKCH] and CSR[MAJORLINKCH].

3. Configure the linked eDMA channel to transfer the message that you want to move.

For example: ADC EOSI0 triggers eDMA to transfer ADC_RSLT0 and ADC_RSLT1 to memory and calculate the average after ten samples.

1) Enable eDMA channel0 which is triggered by ADC EOSI0 via configuring DMAMUX_CHCFG0, and configure eDMA channel0 to clear the EOSI0 flag by transferring a variable contained constant 0x800 to ADC_STAT.

2) Enable channel link of eDMA channel0 to trigger eDMA channel1 after the completion of transfer.

3) Configure eDMA channel1 to transfer ADC_RSLT0 and ADC_RSLT1 to memory.

ERR051374: PWM fault may work abnormally when the fault signal is very narrow

Description

If the fault signal pulse width is narrower than a certain threshold, the protected PWM channels may generate a glitch, which occurs after the PWM channel outputs become inactive.

Workaround

(1) When FCTRL2[NOCOMB] = 0, FFILT [GSTR]= 0, and FFILT[FILT_PER]=0, pulse width of fault signals must be larger than 6 PWM clock periods, otherwise a glitch may be generated on the protected PWM channels.

(2) When FCTRL2[NOCOMB] = 0, FFILT [GSTR]= 1, and FFILT[FILT_PER]=0, pulse width of fault signals must be larger than 3 PWM clock periods, otherwise a glitch may be generated on the protected PWM channels.

(3) When FCTRL2[NOCOMB] = 0, FFILT [GSTR]= 1, and FFILT[FILT_PER] has non-zero values, pulse width of fault signals must be larger than FILT_PER*(FILT_CNT+3)+6 PWM clock periods, otherwise a glitch may be generated on the protected PWM channels.

(4) When FCTRL2[NOCOMB] = 0, FFILT [GSTR]= 0, and FFILT[FILT_PER] has non-zero values, pulse width of fault signals must be larger than FILT_PER*(FILT_CNT+3)+9 PWM clock periods, otherwise a glitch may be generated on the protected PWM channels.

ERR051706: The DAC output jumps to MAXVAL or MINVAL value and lasts two REFRESH clock cycles (instead of one) in the first waveform period after an active SYNC_IN signal occurs with CTRL0[ONESHOT]=0 and CTRL0[AUTO]=1 in triangle waveform mode

Description

When DAC is configured to output a triangle waveform (CTRL0[ONESHOT]=0, CTRL0[AUTO]=1, and CTRL0[SYNC_EN]=1), depending on CTRL0[UP] and CTRL0[DOWN] initialization sequence:

1. When CTRL0[UP] is set first, then CTRL0[DOWN] is set in the initialization: DAC output goes down first and then goes up. If an active SYNC_IN signal occurs when DAC output is ramping up, DAC output by design is set to the updated MAXVAL value and a new periodic triangle waveform is generated. In this situation, at the beginning of the first waveform period after SYNC_IN signal occurs, DAC output stays at updated MAXVAL for two REFRESH clock cycles instead of one. There's no such issue if an active SYNC_IN signal occurs when DAC output is ramping down in this case. See the illustration below.

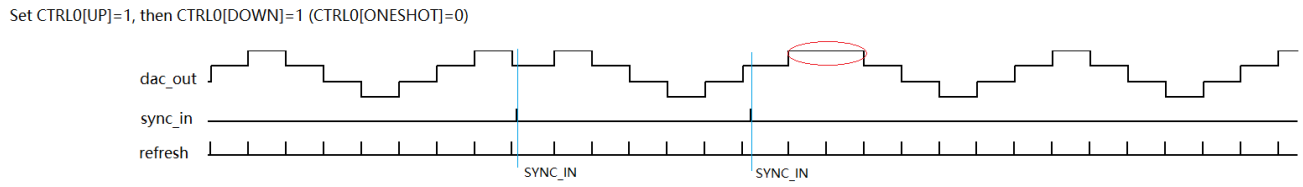

Figure 1. "UP is set and then DOWN is set"

2. When CTRL0[DOWN] is set first, then CTRL0[UP] is set (or DOWN and UP are set simultaneously) in the initialization: DAC output goes up first and then goes down. If an active SYNC_IN signal occurs when DAC output is ramping down, DAC output by design is set to the updated MINVAL value and a new periodic triangle waveform is generated. In this situation, at the beginning of the first waveform period after SYNC_IN signal occurs, DAC output stays at updated MINVAL for two REFRESH clock cycles instead of one. There's no such issue if an active SYNC_IN signal occurs when DAC output is ramping up in this case. See the illustration below.

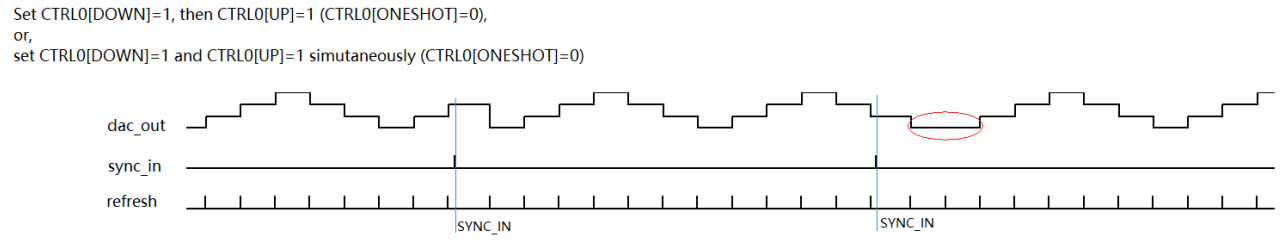

Figure 2. "DOWN is set and then UP is set"

Workaround

No workaround.

ERR051724: DAC output can't reach MAXVAL or MINVAL in automatic mode when CTRL0[ONESHOT] = 1

Description

When CTRL0[AUTO]=1, CTRL0[ONESHOT]=1, and CTRL0[SYNC_EN]=1, an active signal on SYNC_IN input triggers DAC to start the waveform output. The waveform depends on whether CTRL0[DOWN] or CTRL0[UP] is set.

1) When DAC output is in ramping up mode (CTRL0[UP]=1, CTRL0[DOWN]=0), maximum DAC output cannot reach to MAXVAL but being equal or greater than MAXVAL-STEP, depending on STEP value.

2) When DAC output is in ramping down mode (CTRL0[UP]=0, CTRL0[DOWN]=1), minimum DAC output cannot reach to MINVAL but being equal or less than MINVAL+STEP, depending on STEP value.

Workaround

This workaround is to set a value at least one LSB larger than the desired to MAXVAL register when DAC runs in ramping up mode or set a value at least one LSB smaller than the desired to MINVAL register when DAC runs in ramping down mode.

For example, when CTRL0[UP]=1, CTRL0[DOWN]=0, MINVAL = 5, STEP = 200, and MAXVAL=805, DAC final output stays at 605 instead of 805. If the workaround is to set a value larger than the desired to MAXVAL, such as setting 806 to MAXVAL in this case, DAC output will be 805. When CTRL0[UP]=0, CTRL0[DOWN]=1, MINVAL = 5, STEP = 200, and MAXVAL=805, DAC final output stays at 205 instead of 5. If the workaround is to set a value smaller than the desired to MINVAL, such as setting 4 to MINVAL in this case, DAC output will be 5.

However, when the desired end value is 4095 in ramping up or 0 in ramping down mode, DAC output never reaches it.

ERR051989: PWM: output may be abnormal when the value of phase delay register is reduced from a non-zero value to 0.

Description

When the value of the SMxPHASEDLY register is reduced from a non-zero value to 0 and the SMxCTRL2[RELOAD_SEL]=1, the submodule x may output an unexpected wide PWM pulse (x=1,2,3).

Workaround

The minimum value of the SMxPHASEDLY register should be set as 1 in this process. To realize no phase delay between the submodule 0 and submodule x in this process, set the SMxPHASEDLY=1, SMxINIT=SM0INIT–1, SMxVALy=SM0VALy–1 (x=1,2,3, y=0,1,2,3,4,5).

ERR052089: Output signals of peripherals with BUS_2X_CLK may not be correctly recognized by peripherals with BUS_CLK

Description

When the output signal of a peripheral clocked by BUS_2X_CLK, which has a width of only 1 clock cycle, feeds to a peripheral clocked by BUS_CLK, it may not be recognized by that peripheral. For example, when PWM module works at BUS_2X_CLK (which is twice bus clock in fast mode by setting SIM_PCR[PWM_CR]), and its PWM_OUT_TRIG signal is connected with one of QTimer inputs through XBAR, it’s possible that some PWM_OUT_TRIG signals are missed by QTimer when QTimer works at BUS_CLK.

Workaround

Use the same clock for peripherals that are connected together.

ERR052090: CPU may malfunction after a COP reset, when the chip is in the fast mode and booting from Flash

Description

When the chip is configured in the fast mode (where CPU operates at 2x bus frequency), and the boot option is booting from Flash, the CPU may malfunction after a COP reset.

Workaround

Configure the chip to boot from ROM by setting FOPT[7:6] to 2’b11 and SIM_BOOT_MODE_OVERRIDE[BOOT_OVERRIDE] to 2’b00. If the bootloader is not needed, make sure the following three conditions are met to minimize the impact on application: 1) BCA starts with tag “kcfg”. 2) Enable direct boot by setting bootflag to 0xFE in BCA. 3) Disable peripheral and pin initialization by setting enablePeripherals to 0x00 in BCA.

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Date of release: 6/2024
Document identifier: MC56F81xxx_0N91Z