MOTOROLA

Chip Errata

68349 32-Bit Integrated Processor

1F13C & 2F13C - 5/23/96

This errata list applies to the following 68349 mask sets:

Mask	Processing Geometry	Part Number Suffix
1F13C	0.8u	"A"
2F13C	0.8u	"A"

The mask set for each part is encoded into the device topside markings - for example, the following markings would indicate a device from the 1F13C mask, manufactured in the 3rd week of 1995:

```
MC68349FT16A
   1F13C
  QEAQ9503
```

CPU32+:

1. **Early Assertion of RMC:** Execution of an RMC instruction may cause the RMC pin to assert one bus cycle before the RMC cycle on a 16 bit data bus or two bus cycles early on an 8 bit data bus under certain conditions.

2. **System Clock Minimum Frequency**: The minimum operating frequency for all clock modes is 100kHz.

ICACHE:

1. **RMC and DMA Arbitration:** When the DMA is arbitrating for the internal bus (eg - external DREQ asserted) while the CPU is executing an RMC type instruction (ie - TAS) and the cache is enabled, the part will lock up.
   Workaround:
   1) Disable the cache before executing any TAS instructions, then enable the cache after the TAS is completed.

2. **Incorrect bytes of data cached:** Byte size accesses to memory using PC relative addressing may cache incorrect data. When using PC relative addressing, bytes of data can be cached because the function codes have the value for program space on them. However, this data may be cached incorrectly if it is accessed as a byte. Word and Long Word accesses will be cached correctly. Since all instructions have lengths of Word and Long Word, they will be cached correctly.
   Workaround:
   1) Do not use instructions with PC relative addressing that will access bytes of memory. (e.g. BTST.B D1,$10000(PC,D3))
   2) Do not use the Icache.

SIM:

1. **SIM LOC:** Loss of Crystal without Limp Mode — If a loss of crystal occurs while the VCO is set to a low operating frequency (131 KHz), the part may lock up and not enter limp mode.

2. **External Clock with VCO mode:** When using external clock with VCO mode, with an XFC capacitor in the 0.01-0.1uF range, the SIM may not reliably detect VCO lock on powerup. As a result, the part never releases RESET even though the EXTAL input clock and CLKOUT are in phase.

Workaround: Use a smaller XFC capacitor - for frequencies > 1MHz start with a capacitance value of 10000pf/F_MHz. Example: for 16.0MHz the recommended XFC capacitance is approximately = 10000pf/16.0 = 625pf. An external POR circuit should be used for all external clock applications to guarantee RESET remains asserted until after VCC stabilizes.
For an external reset after POR, the SLOCK bit may not be set. This is only a problem with the assertion of the SLOCK lock indication - the VCO and CLKOUT remain phase locked to the input clock both during and after the external reset.

3. **LPSTOP and External Clock with VCO:** When using external clock with VCO mode, the CPU will not reliably exit LPSTOP if the SYNCR is programmed to turn off the VCO when in LPSTOP.
Workaround: Program the SYNCR to enable the VCO in LPSTOP.

4. **Autovectored IACK and BR**: If BR is asserted during an autovectored IACK cycle, AS will negate 1/2 clock early.
Workaround: Decode the IACK address range (A19 & FC2 & FC1 & FC0 & !AS) and use the resulting signal to force BR high during IACK cycles.

5. **Show Cycles and BR**: If show cycles and external arbitration are enabled, and BR is asserted immediately before the clock edge from which DS asserts for a show cycle, the show cycle will be truncated. The data bus drive time for the show cycle will overlap the front end of the alternate master bus tenure by one clock (data will tristate from the clock falling edge one clock after the falling edge BG asserts from).
Workarounds: 1) Disable show cycles when alternate master bus activity is possible. 2) Delay BG assertion to the system by one clock, or delay the alternate master from driving the data bus for one clock after BG asserts.

DMA:

1. **DMA DONEx Input:** In dual-address mode, if DONEx is asserted by an external device to stop the channel, only the read portion of the last transfer will complete.

   Workaround: Instead of asserting DONEx to stop the channel and cause the DMA to generate an interrupt, assert an interrupt directly on one of the 68349's IRQx inputs. The interrupt sevice routine can then explicitly stop the channel by clearing the start bit in the channel's DMACCR register.

2. **DMA Bus Error:** If the last transfer of a DMA bus tenure is terminated with a bus error, the following CPU bus cycle may not be internally terminated by the SIM, or may be bus errored. A DMA bus tenure ends when the BTC count decrements to 0, external DONE asserts, or a pending interrupt forces the channel off the bus.

General:

1. **JTAG:** For 5V product (MC68349FT16A and -25A), if a large number of outputs are simultaneouly updated from all 1's to all 0's during the EXTEST instruction, the "ab.ctl" control bit's value may be toggled. This failure is sensitive to higher VDD levels. This errata does not apply to 3V product (MC68349FT16VA).

Notes:

1. As of the 1F13C mask set, the TDICL(min.) specification #27 for 3V product (MC68349FT16VA) has been changed from 5ns (min.) to 8ns (min.). Refer to PCN-94-R00229.

2. Serial Module Clocking: The serial module synchronization mechanism has been changed beginning with the F13C mask set to relax CPU clock frequency restrictions when using the internal baud rate generator. See the attached description for additional information.

Serial Module Clocking Change
Preliminary Information

Note: This document contains preliminary information on a functional improvement for the serial module implemented in the 68349 beginning with the F13C mask. The relaxed clock specifications shown are preliminary, and subject to change.

Change description:
The serial module internal clock synchronization has been revised to relax CLKOUT minimum frequency requirements when using the internal baud rate generators. The revised CLKOUT requirements are a relaxation of the current specifications - no change to existing designs will be required to accomodate this feature.

Previously, a minimum 8.3MHz CLKOUT frequency was required to use the internal baud rate generators with the default 3.6864MHz serial crystal. In the new serial module, the serial clock synchronization has been modified to allow the minimum CLKOUT frequency to be scaled depending on the maximum baud rate selected. Operation and specifications for external clocking via SCLK are not affected by this change.

Table 1 below shows the resulting minimum CLKOUT frequency for each programmable baud rate. Note that applications using the VCO clock modes - crystal and external clock with VCO - are restricted to a 131KHz minimum CLKOUT frequency. An errata exists which also limits CLKOUT to 100KHz for external clock without VCO mode; refer to the silicon errata for each part.

baud rate	CLKOUT Fmin	baud rate	CLKOUT Fmin
50	3250Hz*	1800	116kHz*
75	4850Hz*	2000	129kHz*
110	7090Hz*	2400	154kHz
134.5	8660Hz*	4800	309kHz
150	9650Hz*	7200	465kHz
200	12.9kHz*	9600	621kHz
300	19.3kHz*	19200	1.26MHz
600	38.5kHz*	38400	2.56MHz
1050	67.3kHz*	76800	8.29MHz
1200	76.9kHz*		

*Note: See text for other minimum system frequency considerations

Table 1: Minimum CLKOUT Frequency vs. Baud Rate

The minimum CLKOUT frequency is calculated using the following formula:

```
CLKOUT(min) = 1/((1/(baud_rate*sample_rate)-Tsetup-Thold)/2)
            = (50-38400 baud):  1/((1/(baud_rate*32)-30ns)/2)
                    or
              (76.8K baud):     1/((1/(baud_rate*48)-30ns)/2)
Tsetup+Thold = 30ns
Sample_rate = 48 for 76.8Kbaud, 32 for others
```

Note that with this revision, replacing the serial crystal with a lower subfrequency (1.8432MHz for example) no longer affects the minimum CLKOUT frequency for a specific baud rate, since the selected baud clock is now synchronized. Also, the logic for the CTSx inputs uses the 1200baud clock as a sample clock - CLKOUT Fmin should be kept above 76.9KHz to avoid affecting CTSx sampling.

- end -