

MCXC_x41_x42_1N87M

Mask Set Errata



Mask Set Errata for Mask 1N87M

Revision History

This report applies to mask 1N87M for these products:

- MCXC141VFM
- MCXC141VLH
- MCXC242VLH
- MCXC142VFM
- MCXC242VFM

Table 1. Revision History

Revision	Date	Significant Changes
1.0	4/2024	Initial Revision

Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR002580	UART: Start bit sampling not compliant with LIN 2.1 specification
ERR003863	ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage
ERR008594	ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM
ERR008595	ROM: ROM read memory command may read the incorrect data back from flash in some cases
ERR008992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Known Errata

ERR002580: UART: Start bit sampling not compliant with LIN 2.1 specification

Description

The LIN 2.1 specification states that start bits should be checked at sample 7, 8, 9, and 10. The UART module checks the start bit at samples 3, 5, and 7 instead.

Workaround

Start bits longer than 5/16 of a bit time are guaranteed to be recognized. Start bits shorter than this should not be used with this version of the UART because they might not be recognized.

ERR003863: ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage

Description

In 16-bit differential mode, the ADC may result in a conversion error when the input voltage on the plus-side of the differential pair (DPx) exceeds approximately $(VREFH * 31/32)$. Other modes are unaffected.

Workaround

To avoid a conversion error near positive full-scale in this mode, do not allow the input voltage on the plus-side of the differential pair (DPx) to exceed $(VREFH * 31/32)$.

ERR008594: ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM

Description

When the MCU boots from ROM, then the I2C0_A1 register will not hold the reset default value (i.e. 0x00) from the ROM boot.

Workaround

Re-initialize the I2C0_A1 register when booting from ROM and when I2C0 is used by applications.

ERR008595: ROM: ROM read memory command may read the incorrect data back from flash in some cases

Description

When using the ROM Read Memory command to read the same flash address twice, if in the middle of the two consecutive reads, the flash address space content is changed by either a flash erasing or programming command, the second Read Memory command does not return the correct value in flash, and instead returns the same value as the first read. The root cause is that the flash cache is not disabled and retains the previous content of the flash.

Workaround

Use one of two options:

- 1) Avoid continuous read of the same flash address space twice
- 2) Invalidate flash cache before second read of the same flash address

ERR008992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Description

Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

Workaround

There are two workarounds:

- 1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.
- 2) Assert NMI signal for longer than 16 bus clock cycles.

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