Advance Information

MPC185HWRM
AC Timing PCN
Explanation

Rev 0.0 4/2004

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Detailed Description and Projected Impact:

Previous revisions of the PPC185 had an internal noise sensitivity which caused the internal PLL to lose synchronization, and immediately lock up. This PLL lock up generally leads to the host CPU generating a Machine Check Error, and the board on which the 185 is operating to lock up as well. To address this PLL errata, both the package and the silicon of the PPC185 were redesigned to eliminate noise sensitivity. The first silicon to incorporate these changes is the PPC185VFB.

Initial testing determined that the PPC185VFB PLL no longer exhibited the PLL Lock Up errata, and the device was made available for customer orders. Recent testing has determined that the PPC185VFB's PLL is still affected by worst case switching noise, with the noise manifesting itself as PLL jitter. This jitter can be reduced by running the MPC185's PLL at 1.8v (the PLL has its own Vdd, APLL), however the PLL voltage must be tightly controlled (+/-2.5%) to minimize PLL noise sensitivity while meeting long term reliability requirements.

With the higher PLL voltage, PLL jitter is reduced, but not eliminated, and because this jitter can have a positive or negative effect on timing on each clock edge, the worst case jitter can cause timing failures in boards not designed to account for it. The worst case jitter in 3.3V systems is 1.9ns and in 2.5V systems is 0.85ns.

As a consequence of the 185's PLL jitter, Motorola is issuing the following revised 185 AC timings. These timings indicate a new maximum operating frequency of 66MHz in PowerQUICC II systems. It is also recommended that for PowerQUICC II systems, 'PLL Range' - pin F15, should be connected to Ovdd, indicating that the PLL is operating in the 33-66MHz range.

MPC185 users are requested to contact their Motorola sales/FAE organization to schedule calls with the 185 Product Team to discuss the impact of this errata on their programs.

AC Timing Characteristics

Table 1 shows the AC timing specifications for use with a PowerQUICC II. All timings assume a 40-pF load.

Table 1. AC Electrical Characteristics - PowerQUICC II

Condition	Name	Min	Max	Unit
Power supply voltage—Core	V_{DD}	1.45	1.65	V
Power supply voltage—I/O	V_{DDQ}	2.3	3.2	V
Power supply voltage—PLL	V_{PLL}	1.75	1.85	V
Clock frequency	F_{clock}	—	66	MHz
Clock cycle time	t_{KHKH}	15.15	—	nS
Clock-to-signal valid delay	t_{KHQV}	—	7.4	nS
Clock-to-signal hold	t_{KHQX}	0	—	
Input setup time to clock-bused signals	t_{DVKH}	3.7	—	nS
Input hold time clock	t_{KHDX}	2.2	—	nS

Table 2 shows the AC timing specifications for use with an MPC107 or other 60x bridge/memory controller. All timings assume a 15-pF load.

Table 2. AC Electrical Characteristics - 60x Bridge/Memory Controller

Condition	Name	Min	Max	Unit
Power supply voltage—Core	V_{DD}	1.45	1.65	V
Power supply voltage—I/O	V_{DDQ}	2.3	2.6	V
Power supply voltage—PLL	V_{PLL}	1.75	1.85	V
Clock frequency	F_{clock}	—	100	MHz
Clock cycle time	t_{KHKH}	10	—	nS
Clock-to-signal valid delay	t_{KHQV}	—	5.2	nS
Clock-to-signal hold	t_{KHQX}	0	—	
Input setup time to clock-bused signals	t_{DVKH}	2.7	—	nS
Input hold time clock	t_{KHDX}	0.95	—	nS