Device Errata
MPC821

Silicon Revision A.2 -- Mask Set 2F84C & 3F84C

August 13, 1997 (Version - 2)

These erratum are valid on Revision A.2 silicon. Please note that any errata listed in this document applies to A revision of the silicon, unless otherwise stated. There are errata that carry over from the Revision 0.x and/or A.1 silicon and are renumbered here along with the Rev 0.x errata number in parenthesis [i.e., (CPU15)]. Those errata that are scheduled to be fixed in the next revision of the silicon are so marked. *New errata or changes to this document have been italicized.*

CPU Errata

CPU1 (CPU15). Bus Error unsupported by the Data Cache burst.

The Data Cache does not support a bus error which might occur on the 2nd or 3rd data beat of a burst. (burt_232)
Workaround: Avoid using bus error in this case.

CPU2. Incorrect Data Breakpoint Detection on Store Instructions.

When a breakpoint on data occurs with size elements of byte or half-word is programmed for store instructions, the following erroneous scenarios might happen:

1.) Breakpoint might be detected when it should not.
2.) Breakpoint might not be detected when it should.

Either of these two cases may occur if the data that is programmed to be detected matches some other portion of the register that is currently stored to memory by the store byte or store half-word instruction.
Examples:
A.) Assume that the user has programmed a byte data breakpoint on store instruction and is looking for the byte element: 0x55. Assume that register R1 has the value: 0x00080000, R10 has the value: 0x55443322 and the following store instruction is performed:

```
stb R10,0x3(R1)
```

What occurs is that byte 0x22 from R10 is stored to address 0x00080003, and this should not generate a breakpoint since 0x22 does not equal 0x55, BUT, in some cases it can and does (in this scenario, R10 does include the data 0x55). The result is a breakpoint is executed when it shouldn't.

B) Assume that in the above case the user is programming for byte element of 0x22, then it might happen that a breakpoint condition will not be detected, although it should.

CPU2. (cont.)

NOTE: These fault cases depend on the previous Load-Store instruction address. If the previous Load-Store instruction address's LSB is different from the current instruction address's LSB, then incorrect breakpoint detection might occur. (burt_246) **Fixed in revision B.**
Workaround:. none.

CPU3. Program Trace Mechanism Error.

In the following case, there is an error in the program trace mechanism.

0x00004ff0: divw. r25,r27,r26
0x00004ff4: divw. r28,r27,r26
0x00004ff8: unimplemented
0x00004ffc: b 0x00005010
and where: 0x00005010 belongs to a page where a page fault occurs.

The divide takes a relatively long time so the instruction queue gets filled with the unimplemented instruction, the branch and the branch target (page fault). When the sequencer takes the unimplemented instruction, it releases the fetch (that was blocked by the mmu error) and this causes the queue to get another instruction in addition to the first page fault. Because the second fault is sequential to the branch target, it is not reported by the queue flush (VF). This causes an incorrect value to be present in the VF flush information when the unimplemented exception occurs. (burt_251) **Fixed in revision B.**

Workaround:. none.

CPU4. Incorrect Value Used for POW Bit of MSR Register .

The value of the bit POW in the MSR register was taken with opposite polarity by the clock control logic. Correct operation of the logic will assure that: if PRQEN in the SCCR register is ('1'), the system clock will switch/remain in high frequency as long as POW bit in the MSR register is reset ('0'). In order to allow the system to switch to "low" frequency the POW bit should have been previously set ('1'). For this errata, if the source of an interrupt request is reset immediately after jumping to the interrupt handler , the clock will continue to run in high frequency since the POW bit is reset ('0') any time that an interrupt service routine is run by the processor (burt_268) **Fixed in revision B.**
Workaround:. Reset the source of the interrupt request BEFORE the RFI instruction is executed; or manipulate the CSRC bit in the PLPRCR register such that it is reset when entering the Interrupt software routine and set before the RFI instruction is executed.

CPU5. Instruction Cache LRU Mechanism Flawed.

The I-Cache Least Recently Used mechanism is flawed in such a way as to reduce the hit ratio in the Instruction Cache and effect performance 5 to 30 percent. The I-Cache does not write the data to the cache according to the least recently used (LRU algorithm but according to the most recently used (MRU) algorithm. (burt_358) **Fixed in revision B.**
Workaround:. None.

SIU Errata

SIU1 (SIU10). Address Output During Showcycles Could Be In Error.

This errata was erroneouslly included in Revision 0 of the errata and in fact does not exist on the A.2 and later silicon.

SIU2. Data Show Cycles Hang Condition.

If the DSHW bit in the SIUMCR register is set in order to allow Data Show Cycles to take place in the external bus, and the CPM/LCD Interface/SDMA initiates a DMA transfer to/from an internal address (for example the Dual Port RAM), the chip will hang. (burt_269) **Fixed in revision B.**
Workaround: If DMA accesses are initiated to internal locations, reset the DSHW bit.

CPM Errata

CPM1. Microcode Bug In Async HDLC & IrDA Protocol.

If the first character received of a new Buffer Descriptor (BD) is either an unmapped (discardable) control character or if it is the Control Escape character ($7d), erroneous operation will result. (burt_236) **Fixed in revision B.**

Workaround: Download and use the microcode patch that is available from our World Wide Web page at [http://www.mot.com/SPS/ADC/pps] There are two files located in the Engineers Toolbox that can be used with the MPC8Bug along with our 821ADS board to download to the MPC821. One is called 'ahdlc.rev0.srx' and applies to all rev 0.x silicon. The other file is called 'ahdlc.revA.srx' and applies to all revision A silicon. To load the micro code use the following MPC8Bug debugger commands:

```
rms cpm rccr 0
rms cpm rctrl 806c
load ahdlc.rev*.srx      (where * is either a '0' or an 'A', depending on revision of silicon.)
rms cpm rccr 1
```

CPM2. SCL I^2C Receive Problem in Arbitration-Lost state.

If the MPC821 I^2Cmaster transmitter loses arbitration to another I^2C master which is transmitting to the MPC821, the MPC821 receiver will not accept the message (address byte not acknowledged). (burt_238) **Fixed in revision B.**

Workaround: Ensure that the other master software performs a retry operation on such failed cycles or avoid multimaster I^2C operation.

CPM3. Concurrent Operation of Ethernet & I^2C or SPI Has Overlapping Parameter RAM Tables

When concurrent operation of the the Ethernet protocol and either I^2C or SPI is set up and used at the same time, there is an overlap in the parameter RAM. (burt_2xx)

Workaround: There is microcode available that moves the I^2C/SPI parameter RAM entries to another location in the dual port RAM. Download the description of the change and the object code file from the website at (http://www.mot.com/SPS/ADC/pps/_subpgs/_etoolbox/8XX/i2c_spi.html). This package is called MPC8XX I^2C/SPI Microcode Package.

General Errata

G1 PLL Fails to lock under certain power rail sequencing.

Fixed in this Revision (A.2); shown here as a place holder for reference and correlation to A.1 errata.

G2. Core Operation Is Limited to 3.0 Volt Minimum.

The current versions of the 821 silicon are only tested and verified at 3.0V to 3.6V power. Because of this, low voltage operation (@2.2V) cannot be used for powering the core.

Workaround: None. To be tested and verified in this or future silicon.

G3. Termination of Open Drain and Active Pins.

All open drain pins and active pullup pins will drain high current when the input voltage to them is greater than VDDH. (burt_266) **Fixed in revision B.**

Workaround: Connect the external pullup resistor on these pins to the VDDH power supply.

G4. Limited Buffer Strength Control for the CLKOUT Signal.

The MPC821 capability to change the strength of the output buffer that drives the CLKOUT signal is not functional. The strength is either full strength (COM = 00. or COM = 01) or disabled (COM = 11). (burt_267) **Fixed in revision B.**

Workaround: Use full-strength-only application.

G5. ESD Breakdown Voltage for XFC Pin Less Than Motorola Imposed Requirements.

The XFC pin (T2) of the A.2 (2F84C & 3F84C) version of the 821 silicon fails Motorola's XC qualification of 1K Volt for the ElectroStatic Discharge (ESD) breakdown voltage test. The maximum ESD voltage that can be applied to this pin on this silicon without damage is 750 Volts.

Workaround: Ensure devices on not exposed to greater than 750 volts of electrolstatic discharge.

G6. Higher Than Expected Keep Alive Power (KAPWR) Current When Main Power (VDDH & VDDL) Is Removed.

There are four nodes within the 821 that are floating when VDDH and VDDL power is not supplied to the device. When this condition occurs, which is typical in a Power Down Mode, the current drain on the Keep-Alive Power rail is greater than expected. (10 - 20 mA versus 10 µA) ***Fixed in revision B.2.***

Workaround: Provide adequate current source for KAPWR pin in Power Down Mode.

General Documentation Errata Associated with Silicon Operation

The following items reflect operation of the MPC821 and how this operation may be currently misrepresented in the MPC821 User's Manual (MPC821UM/AD). Please refer to the sections mentioned, in the UM, for clarification and/or replacement by the following information.

DOC1. Cache Inhibit Operation.

In some cases, the last instruction executed from a certain page gets the caching inhibited attribute of the NEXT page when the page change occurs between the time the fetch request was issued to the Instruction Cache and the time the Instruction Cache delivers the instruction to the sequencer. Since Instruction Cache inhibit is used only for performance reasons (mostly for not caching very fast memories or pages that include non real-time programs), the performance effect of this feature is negligible. See Section 9, Instruction Cache. (burt_237)

DOC2. DAR and DSISR Updating with Debug Counter Operation.

If a load/store breakpoint occurs as a result of debug counter expiration when one of the following three interrupts occur, Machine Check interrupt due to an error in a load/store cycle, Data Storage interrupt, and Alignment interrupt; the DAR & DSISR is set to the effective address associated with the interrupting instruction. In some cases, when a load/store breakpoint occurs due to one of the debug counters expiration; just before one of the above interrupts occur, the value of the DAR & DSISR is changed. Although the interrupt is after the breakpoint; and, therefore should be ignored by the processor, the DAR and DSISR are updated. The value of the DAR & DSISR is normally used by the software inside these interrupt routines and therefore this anomaly may influence program flow only if these interrupts are nested one inside the other and load/store breakpoint is used inside one of these interrupt routines. See Section 6.6.13, Core, and Section 19, Development Support.

DOC3. Ethernet Is Only Supported on SCC1.

All references to Ethernet support on SCC2 is in error. The MPC821 only supports the Ethernet protocol on SCC1. Disregard all references to Ethernet on SCC2 in Section 16 of the MPC821 User's Manual.