# MPC821 Revison Changes

The following is a summary of the changes between the different MPC821 silicon revisons that have been shipped to our customers.

## REV 0.2 to REV 0.3 Changes

The only change between these two revisions is in the sense amplifier cell of the instruction cache. This change has no logic influence, it should only solve the high VDD sensitivity of this cell. The change was done only by changing the connectivity between devices inside the cell. This cell is instanciated 128 times inside the design.



## REV 0.3 to REV A Changes

Revision A of the MPC821 was enhanced by the inclusion the following new features:

**Memory Controller**

• The Memory Controller of the MPC821 supports External Masters' accesses to the memory devices controlled by this interface.

• The Memory Controller was enhanced in a way that it is able to output the GPL5x line at the falling edge of the GCLK1 in the 1st clock cycle of the access when it is controlled by the UPMx.

• An additional parameter was included on the Option Registers of the Memory Controller when the access is controlled by the GPCM. It is called EHTR (Extended Hold Time on Read Accesses) and it is intended to be used by devices that require a long disconnection time from the Data Bus on read accesses.

**SIU**

• The behavior of the Real Time Clock was modified in a way that the PORESET assertion does not affect its function. The PORESET will not reset the counter. A slight modification relative to the previous revision is that after PORESET, the Real Time Clock associated registers will be locked by the "KAPWR Lock mechanism".

## General Bus Interface

• The MPC821 is able to run internal at twice the frequency of operation of the External Bus. This feature is controlled by a new field called EBDF (External Bus Division Factor) in the SCCR register.

• The MPC821 supports a new bus termination -RETRY-. By means of this signal, the external slave indicates to the MPC821 to relinquish the bus ownership, enabling the control of the bus by an alternate masters.

## Reset

• The MPC821 requirement of assertion time of PORESET was reduced considerably. It does not have to be asserted until the internal PLL is locked.

## LCD Interface

• The MPC821 now supports 256 colors.

• The Programming Model was slightly modified:
-256 entries color map added (also a new address in the Dual Port RAM)
-Exception (Underrun, Bus Error) Interrupt Enable bit added
-The BNUM (Burst Number) bit field was extended by one bit.