MSC8113 Device Errata for Mask 2K98M

ID Number	Errata

ENET1	**Date Published:** 1/16/2009
	Description: The Ethernet controller Rx FIFO can encounter an overflow situation due to a system busy condition caused by heavy accesses to SDRAM memory from competing devices and the Ethernet controller. Such conditions can increase the time required to access the memory, which increases the possibility of an overflow condition due to a heavy line load. Note that a system busy condition is not due to a lack of Rx buffers as indicated by the IEVENT[BSY] bit or a GRS condition indicated by the IEVENT[GRSC] bit. The symptom is that the receiver may drop frames but not indicate a dropped frame condition. In some cases, the receiver may hang. When the receiver enters a hung state, all incoming frames are dropped and the RDRP register logs them as dropped frames. Only an external HRESET can make the Ethernet controller exit this condition.
	Module(s) Affected: Ethernet controller.
	Impact: Minimal.
	Workaround: Use either of the following options to avoid this condition:
	1. Change the SIU priorities in the PPC_ALRH and PPC_ALRL registers so that all Ethernet priorities on the System Bus are higher than the SC140 cores. When using the CodeWarrior® debugger, this is done by changing the values of the PPC_ALRH and PPC_ALRL in the 8122ADS_DSI32_Slave_Init.cfg file to the following:
	`writemem32 0x1471002c 0xdeaf5478 # PPC_ALRH #ETH low and me PRI > SC140 PRI`
	`writemem32 0x14710030 0x9bc36012 # PPC_ALRL`
	When not using the debugger, the registers must be updated by software code running from internal memory while only one core is active and the DMA controller is not active.
	2. Move the Ethernet buffers to M2 memory.
	Fix Plan: None.
	System Number: None

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Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
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www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 010 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
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