Mask Set Errata for Mask 2M62B

Introduction

This report applies to mask 2M62B for these products:

- MC68HC908QB8
- MC68HC908QB4
- MC68HC908QY8

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. All standard devices are marked with a mask set number and a date code.

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0301" indicates the first week of the year 2003.

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

SE111-RSTEN: CONFIG2 Register Bit RSTEN Is Cleared by an LVI Reset

Description: The RST pin functionality is enabled in the CONFIG2 register by RSTEN. In the data sheet, this bit is described to be unaffected by all resets other than a power-on reset (POR).

RSTEN in the CONFIG2 register is cleared by an LVI reset only. This behavior prevents the RST pin from driving low during an LVI reset when the RST function is enabled.

The MCU will perform an internal reset as expected. All other reset sources will drive the RST pin low during an internal reset if the RST function is enabled. This is a known issue and will be fixed on subsequent masks.

Workaround: RSTEN must be configured by application code after an LVI reset has occurred. This ensures that the RST pin is configured as expected.

If necessary, an indication of LVI reset can be forced in user code by monitoring the LVI bit in SRS and immediately driving PTA3 low for any number of cycles during program startup. The CONFIG registers can then be written to enable the RST function. Note that this may cause an extra apparent reset low signal because the LVI bit in SRS is typically set during power-up.

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