LAYERSCAPE LS2048A AND LS2088A COMMUNICATIONS PROCESSORS

The Layerscape LS2 family of communications processors delivers unprecedented performance and integration for the smarter, more capable networks of tomorrow.

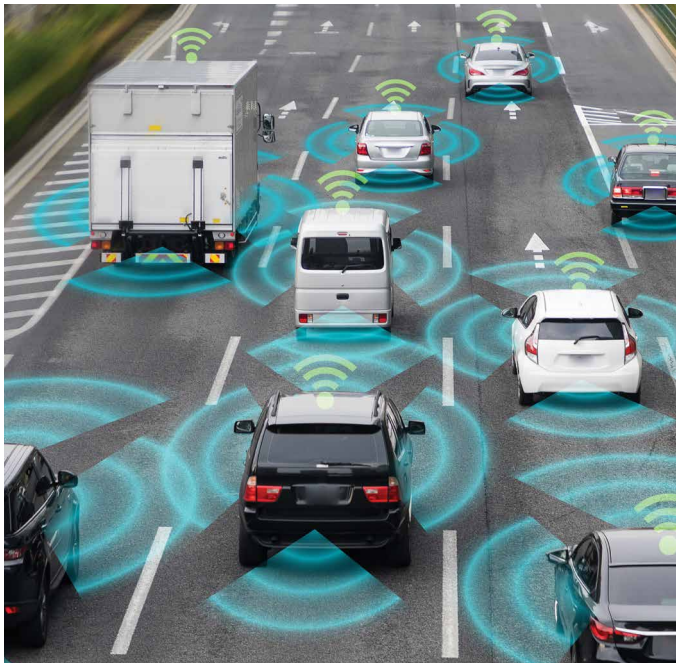
TARGET APPLICATIONS

- Enterprise routing
- Wireless access
- Datacenter processing
- Military and aerospace
- SDN/OpenFlow switching
- NFV solutions

The Layerscape LS2048A and LS2088A multicore processors combine four and eight Arm® Cortex®-A72 cores, respectively, with the advanced, high-performance datapath and network peripheral interfaces required for networking, telecom/datacom, wireless infrastructure, military and aerospace applications.

The LS2 family includes our second-generation Data Path Acceleration Architecture (DPAA2). DPAA2 provides the infrastructure required to support simplified and secure networking interface and accelerator sharing by multiple general-purpose CPU cores. It also provides a range of powerful acceleration engines to off-load software running on the CPUs.

A powerful software toolkit supports the Arm general-purpose processors and DPAA2 with a higher level of hardware abstraction to help make software development quick and simple. This combination balances ease-of-use with high-performance processing in a Linux® environment that is familiar to any software programmer. Customers can fully exploit the underlying hardware and easily adapt to network changes for real-time "soft" control over the network.



SOFTWARE TOOLKIT

We have significant and increasing global investment in software for the embedded marketplace. Our software development kit (SDK) delivers foundational technologies (e.g., user space, fast path, virtualization) that are continuously "upstreamed" to support the networking portfolio. With decades of commercial Arm software tooling, operating system development and delivery, we continue to be a strong supporter of open-source and industry software consortia, including Linaro and the Linux Foundation.

UNPARALLELED INTEGRATION

Layerscape LS2 family processors integrate up to eight (8) 10/2.5/1 Gbit/s and eight 2.5/1 Gbit/s Ethernet interfaces with L2 switching capability with PCIe® controllers (supporting SR-IOV) and next-generation SATAIII and USB3 controllers. The next-generation datapath is complemented with high-performance acceleration, including security and trust, pattern matching and data compression.

NETWORKING PERFORMANCE

The LS2 processors contain an advanced I/O processor that offloads the general-purpose Cortex-A72 cores with in-line or fully autonomous networking functions, involving complex look-ups, header manipulations, and even encapsulations and encryption. A dedicated datapath memory controller is available to support lookup acceleration and packet processing needs.

The next-generation datapath also provides necessary and proven acceleration such as crypto acceleration, Pattern Match/RegEx and data compression engine.

DPAA2 also now integrates L2 switching, allowing the LS2 processors' eight 10 Gbit/s Ethernet and eight 1/2.5 Gbit/s Ethernet ports to be configured as an 88 Gbit/s L2 switch.

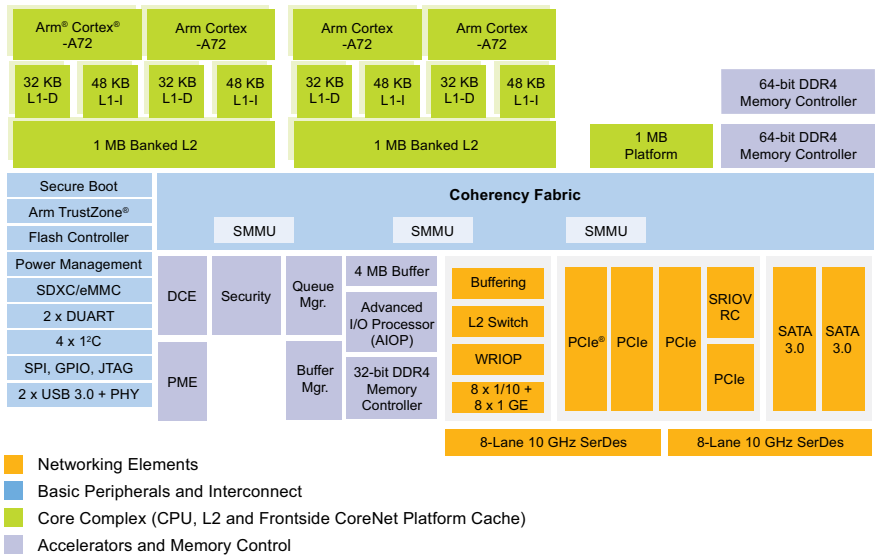
COMPLETE ENABLEMENT, RICH ECOSYSTEM

The LS2 family includes a comprehensive ecosystem to ensure that ease-of-use is first priority.

The complete offering includes:

- APIs that are compliant with industry-standard consortiums, including DPDK
- Management software that takes care of setup, initialization and teardown of interfaces, accelerators and networking functions
- Performance-optimized functional datapath libraries
- Commercial-grade application kits for time-efficient networking application deployment
- Tools (e.g., accelerators, debug) to help you spend your time creating value-added software
- Powerful combination of NXP and Arm ecosystems forexceptional support
- Open-source software, available upstream for all customers to leverage

LS2088A PROCESSOR BLOCK DIAGRAM



LAYERSCAPE LS2 FAMILY FEATURES

Up to Eight Cores Built on Arm® Architecture	8 x Cortex®-A72 CPUs, 64-bit, 2.1 GHz, clusters of two cores sharing 1 MB L2 cache 1 MB L3 cache and 4 MB of cache component memory
Hierarchical Interconnect Fabric	Coherency fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation
DDR Controllers	Two 64-bit DDR4 SDRAM memory controllers with ECC and interleaving support, up to 2.1 GT/s One secondary 32-bit DDR4 memory controller for the datapath, up to 1.6 GT/s
Accelerated Packet Processing	Advanced I/O processor, up to 20 Gbit/s complex packet processing 20 Gbit/s SEC crypto acceleration 10 Gbit/s pattern matching engine 20 Gbit/s data compression engine
Express Packet I/O	Supports 1 x 8, 4 x 4, 4 x 2, 4 x 1 PCIe® Gen 3 controllers SR-IOV support, root complex 2 x SATA 3.0, 2 x USB 3.0 with PHY
Network I/O	Wire rate I/O processor, with hardware parsing, classification, and policing, featuring: • Eight 1/2.5/10 GbE + eight 1/2.5 GbE • L2 switching on the Ethernet interface • XAUI/XFI/KR and SGMII • MACSec on up to four 1/10 GbE
Virtualization	Support for hardware virtualization and partitioning enforcement

LAYERSCAPE LS2 FAMILY COMPARISON CHART

	LS2088A	LS2048A
Cores	8	4
Arm® Cortex®-A72, up to 2.1 GHz/L2 Cache (MB)	8/4	4/2
Advanced I/O Processor	20 Gbit/s	
L2 Switch	88 Gbit/s	

www.nxp.com/Layerscape

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