# AN12030

## TEA19031AxT secondary-side SMPS controller

Rev. 1 — 5 October 2017 Application note

**Document information**

| Information | Content |
|---|---|
| Keywords | TEA19031, SMPS controller, USB-PD, USB Type C |
| Abstract | The TEA19031 is a secondary side SMPS controller with embedded CoolFlux Digital Signal Processor that supports the USB Power Delivery 2.0 (USB-PD) protocol via a USB Type-C cable connection. |

## Revision history

| Rev | Date | Description |
|---|---|---|
| v.1 | 20171005 | first issue |

# 1 Introduction

The TEA19031 is a secondary side SMPS controller with embedded CoolFlux Digital Signal Processor that supports the USB Power Delivery 2.0 (USB-PD) protocol via a USB Type-C cable connection (Ref. 1). Figure 1 shows a typical application diagram. Table 1 provides details about pinning functionality. The TEA19031 forms a link between a connected consumer device and a primary side residing control IC like the TEA193x (Ref. 4). With an optional synchronous rectifier driver like the TEA199x (Ref. 5), the TEA19031 operates the power converter. For communication with the consumer device, Biphase Mark Coding (BMC) is applied on the Type-C connector CC1 and CC2 lines. Five USB-PD Power Data Objects (PDOs) are supported.

Resulting control and protection information is directed to the primary side controller by adjusting the optocoupler current. Consumer devices requiring output currents exceeding 3 A must either use a captive cable or apply USB-PD e-marking. The TEA19031 does not support the $V_{CONN}$ mechanism, which supplies powered cables.

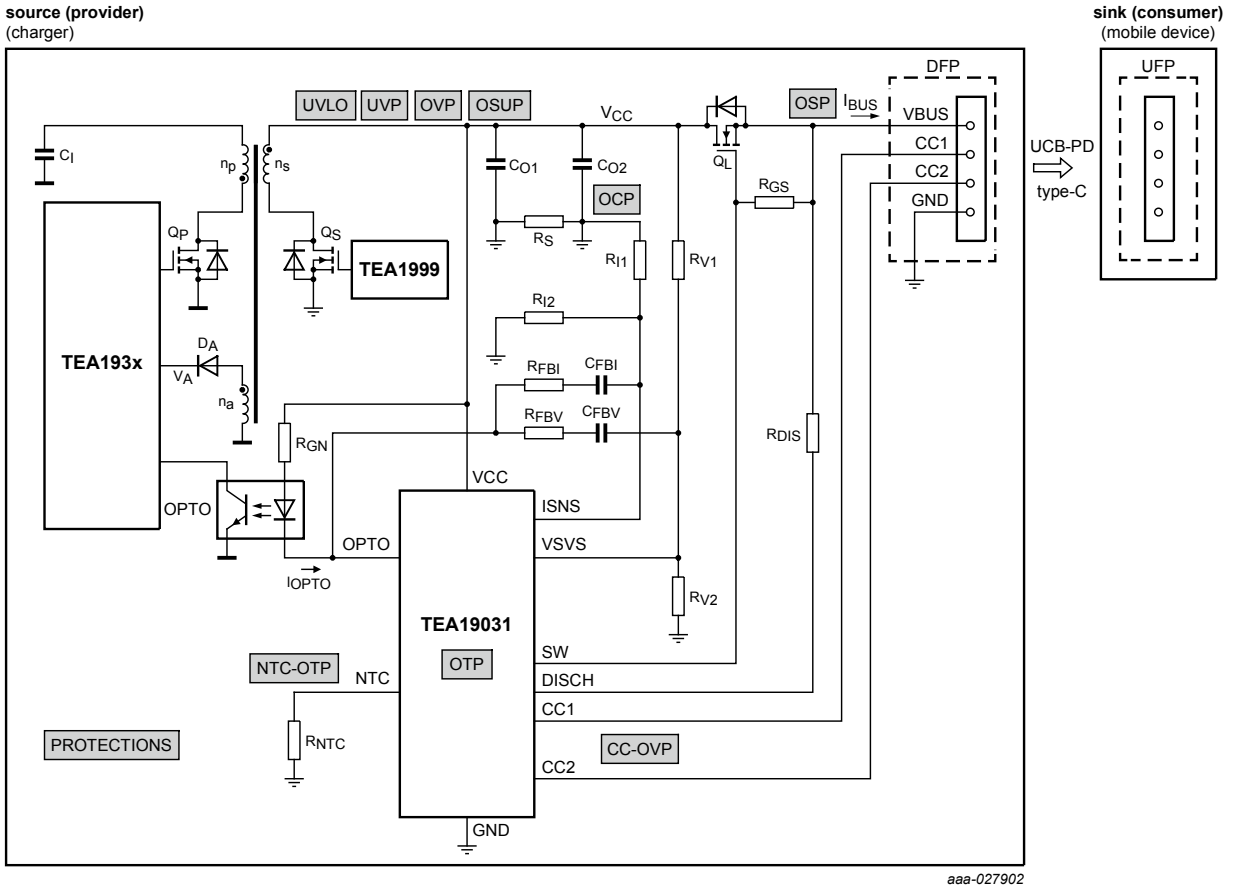



**Figure 1. TEA19031 application diagram**

**Table 1. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| VCC | 1 | Supply voltage for TEA19031 with internal 20 mA current sink[1] |
| OPTO | 2 | Optocoupler driver to send control information to primary side power converter controller |
| NTC | 3 | External NTC temperature measurement |
| ISNS | 4 | Current sense error amplifier input terminal |
| VSNS | 5 | Voltage sense error amplifier input terminal |
| CC2 | 6 | Type-C CC2 detection and USB-PD communication |
| CC1 | 7 | Type-C CC1 detection and USB-PD communication |
| DISCH | 8 | VBUS fast discharge switch and additional internal 1 mA current sink[2] |
| GND | 9 | ground |
| SW | 10 | Load switch (NMOS) driver derived from internally generated boost voltage[3] |

[1] Active when required for VCC-down regulation (discharge) and overshoot limitation.
[2] Active when both the load switch (QL) and the internal DISCH discharge switch are off.
[3] $R_{GS}$ must be at least 1 MΩ.

A multitude of settings is available, making the TEA19031a versatile device. Table 2 shows an overview of the available TEA19031 variants with their detailed settings. Each variant targets a specific application power level.

**Table 2. TEA19031 variant settings**

| Symbol | Description | AG (18 W) | AD (27 W) | AE (45 W) | AF (60 W) | AM | AO |
|---|---|---|---|---|---|---|---|
| $V_{PDO0}$[1] | PDO0 voltage vSafe5V (default) | 5 V | 5 V | 5 V | 5 V | 5 V | 5 V |
| $I_{PDO0}$ | Maximum current for PDO0 | 3 A | 3 A | 3 A | 3 A | 3 A | 3 A |
| $V_{PDO1}$ | PDO1 voltage | 5 V | 5 V | 5 V | 5 V | 5 V | 5 V |
| $I_{PDO1}$ | Maximum current for PDO1 | 3 A | 3 A | 3 A | 3 A | 3 A | 3 A |
| $V_{PDO2}$ | PDO2 voltage | 6 V | 6 V | 9 V | 9 V | 9 V | 9 V |
| $I_{PDO2}$ | Maximum current for PDO2 | 2.9 A | 3 A | 3 A | 3 A | 2.49 A | 3 A |
| $V_{PDO3}$ | PDO3 voltage | 7 V | 7 V | 12 V | 12 V | 12 V | 15 V |
| $I_{PDO3}$ | Maximum current for PDO3 | 2.5 A | 3 A | 3 A | 3 A | 3 A | 3 A |
| $V_{PDO4}$ | PDO4 voltage | 8 V | 9 V | 15 V | 15 V | 15 V | 19 V |
| $I_{PDO4}$ | Maximum current for PDO4 | 2.2 A | 3 A | 3 A | 3 A | 2 A | 3 A |
| $V_{PDO5}$ | PDO5 voltage | 9 V | - | 20 V | 20 V | - | 20 V |
| $I_{PDO5}$ | Maximum current for PDO5 | 2 A | - | 2.3 A | 3 A | - | 3.26 A |
| $K_{comp}$ | cable compensation | 117 mV/A | 117 mV/A | 67 mV/A | 67 mV/A | 67 mV/A | 67 mV/A |
| $K_{Vdiv}$ | voltage sense resistive divider ratio | 1/5.478 | 1/5.478 | 1/8.325 | 1/8.325 | 1/8.325 | 1/8.325 |
| $R_s$ | current sense resistor value | 5 mΩ | 5 mΩ | 10 mΩ | 10 mΩ | 10 mΩ | 10 mΩ |
| CC-OCP | current limiting mode | CC | CC | OCP | OCP | CC | OCP |
| $I_{lim}$ | limiting current (OCP and CC) | 110 % | 110 % | 120 % | 120 % | 120 % | 120 % |

| Symbol | Description | AG (18 W) | AD (27 W) | AE (45 W) | AF (60 W) | AM | AO |
|---|---|---|---|---|---|---|---|
| $V_{ovp}$ | OVP level | 120 % | 120 % | 120 % | 120 % | 125 % | 120 % |
| NTC | NTC protection | NTC-OCP | NTC-OCP | NTC | NTC | - | - |

[1] In addition to the default vSafe5V (VPDO0), five selectable USB-PD PDOs are available

## 2 USB-PD application

A TEA19031 based application in USB-PD terms consists of a single source (provider) being a mains connected charger and a single sink (consumer) being a mobile device. During start-up, the TEA19031 defaults the VCC converter output voltage to vSafe5V (5 V typical). It limits the current to a fixed maximum of 3 A.

After establishing a valid attach detection, the TEA19031 starts USB-PD contract negotiations by advertising its power capabilities regarding the five PDOs. The consumer responds by requesting one particular PDO. When the TEA19031 in turn accepts this request, the contract is established. It remains in place until the consumer is detached, a hard reset occurs, or the source is unable to maintain its power level.

# 3 Establishing a type-C connection

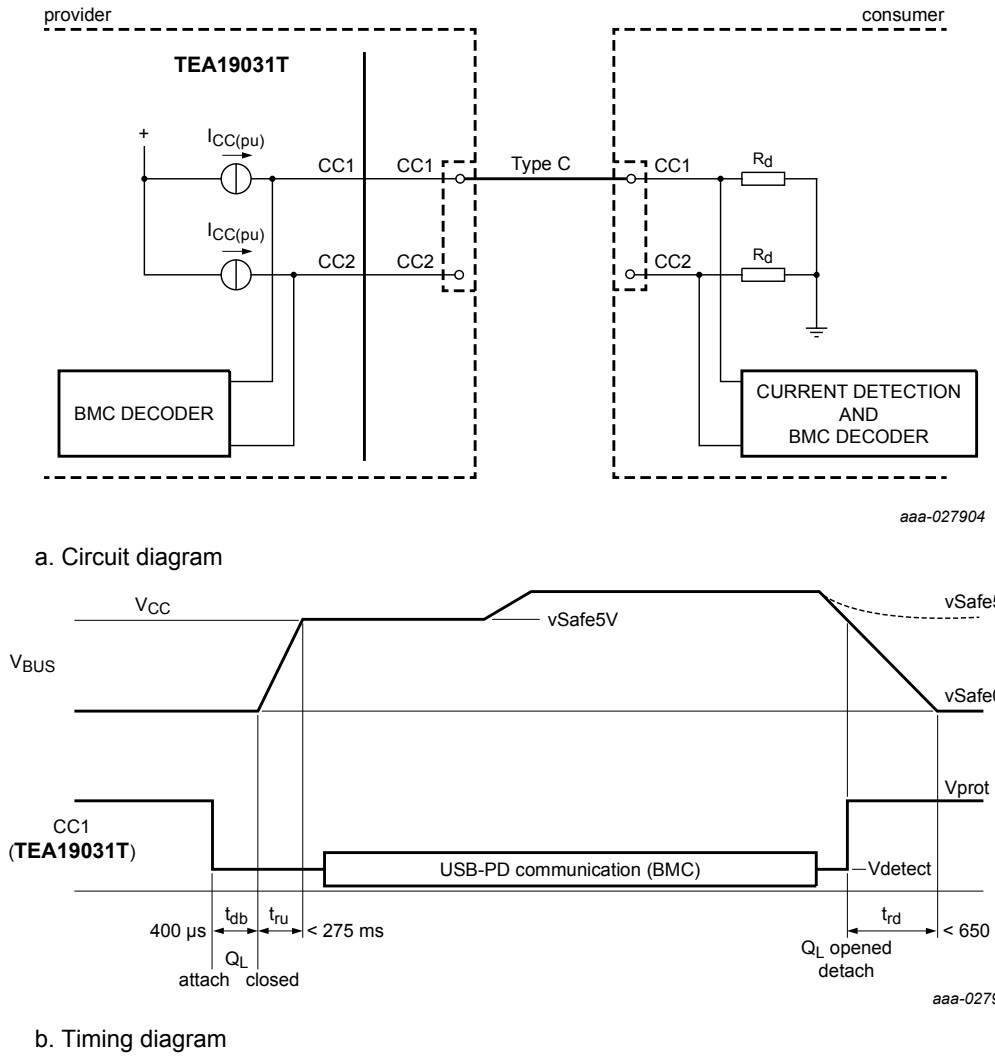



**Figure 2. Attach and detach configuration**

Equipped with 330 µA pull-up current sources $I_{CC(pu)}$ for each of both CC pins, the TEA19031 advertises the default current capability of the converter at 3 A. A consumer with the appropriate termination resistor $R_d$ (Ref. 2) connected to both CC lines can detect this current capability. At the same time, the TEA19031 detects the attach of a consumer. Figure 2 shows a possible configuration in which the CC1 pin is used by both provider and consumer. Alternatively the CC2 pin can be used.

A typical attach and detach sequence starts with both the provider and consumer being unattached. Load switch $Q_L$ is open and the TEA19031 is waiting to detect the presence of a consumer. Detection starts when a consumer with a pull-down resistor $R_d$ of 5.1 kΩ or 1.1 V voltage clamp is connected to one of the CC lines. Allowing ground offset in the connecting cable, the pull-down resistor or clamp in the consumer must establish a detectable voltage $V_{detect}$ between 0.85 V ($V_{IL}$) and 2.45 V ($V_{IH}$) on one of the CC pins of the TEA19031. After a debounce period $t_{db}$ of 400 µs, but while an attached consumer is still detected, load switch $Q_L$ is closed and $V_{BUS}$ is connected to $V_{CC}$. The internally generated driver voltage on pin SW controls the load switch. This voltage is about 6 V

above $V_{CC}$. Because of the internal 80 kΩ output resistance of pin SW, the gate-source discharge resistor $R_{GS}$ must be at least 1 MΩ. Within 275 ms, the bus voltage must reach its vSafe5V level such that reliable USB-PD communication can commence. The consumer is now powered. The connected operating state lasts until the TEA19031 detects a detach. Load switch $Q_L$ opens immediately after detecting a detach and the internal switch connected to DISCH discharges $V_{bus}$ through external resistor $R_{DISCH}$. The $V_{bus}$ voltage level must return to vSafe0V within 650 ms which puts certain design constraints on resistor $R_{DIS}$ and any capacitance connected to $V_{bus}$. At the same time, the TEA19031 ensures that the $V_{CC}$ level returns to vSafe5V by activating the internal current sink of 20 mA connected to VCC.

As specified in the USB Type-C standard, alternative connection states may be present. Table 3 gives an overview of the various connection states and the correspondingTEA19031 response. In all cases where a sink or Debug Accessory Mode is connected, an attach is detected.

**Table 3. USB Type-C connection states and TEA19031 response**

| State | CC1 connection | CC2 connection | TEA19031 response |
|---|---|---|---|
| nothing attached | open | open | no attach |
| sink attached | $R_d$[1] | open | attach |
| | open | $R_d$[1] | attach |
| powered cable without sink attached | $R_a$[2] | open | no attach |
| | open | $R_a$[2] | no attach |
| powered cable with sink attached | $R_d$[1] | $R_a$[2] | attach |
| | $R_a$[2] | $R_d$[1] | attach |
| debug accessory mode attached | $R_d$[1] | $R_d$[1] | attach |
| audio adapter accessory mode attached | $R_a$[2] | $R_a$[2] | |

[1] $R_d$ = 5.1 kΩ nominal (alternatively a 1.1 V voltage clamp can be applied) (Ref. 2)
[2] $R_a$ = 1 kΩ nominal (Ref. 2)

# 4 USB-PD communication

The TEA19031 supports the USB-PD 2.0 standard. The following sections are a limited extraction of the USB-PD standard. However, they never prevail over the USB-PD standard (Ref. 1).

## 4.1 Data packets and signaling

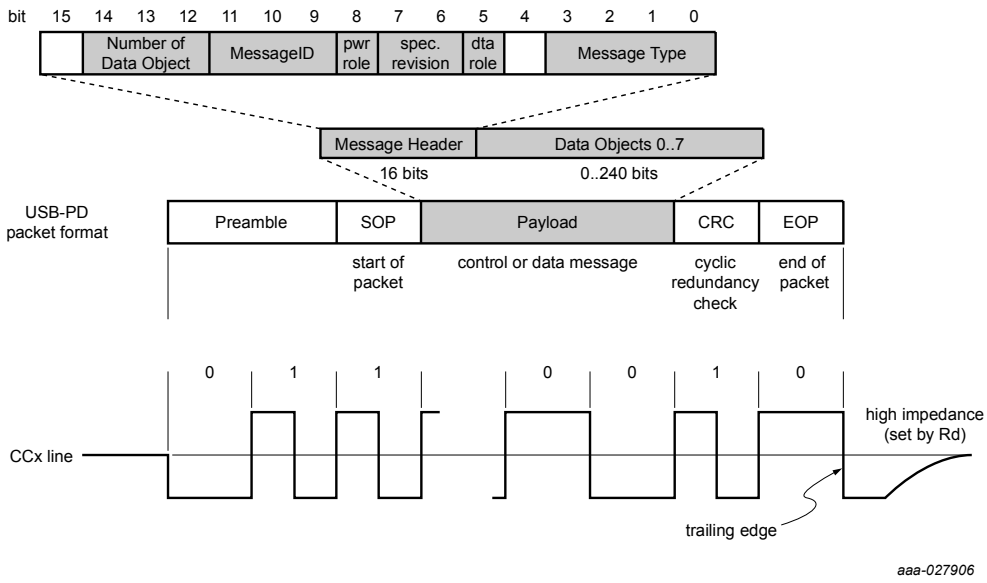



**Figure 3. Data packets and signaling**

Figure 3 shows the USB-PD messages. They are defined as coded packets that start with a preamble to prepare the receiver for receiving data. The preamble is followed with a Start Of Package (SOP), the actual payload, Cyclic Redundancy Check (CRC) error correction information, and finally an End Of Package (EOP). Two kinds of packet payloads are available:

- Control message:
  The payload contains only a message header in which the number of data objects (bits 14 to 12) is zero. The MessageType (bits 3 to 0) identifies the message.
- Data message:
  The payload contains a message header. It is followed by one of up to seven data objects; now the number of data objects is non-zero.

Table 4 summarizes the supported USB-PD 2.0 messages. When the TEA19031 receives an unidentified message, it responds with the reject message.

**Table 4. USB-PD 2.0 supported messages**

| MessageType | Packet payload | Send (S)/ Receive (R)[1] | Description |
|---|---|---|---|
| GoodCRC | control | S/R | acknowledge that the previous message was correctly received |
| Accept | control | S/R | source/sink is able meet the Request message |
| Reject | control | S | source is unable to meet the Request message |
| PS_RDY | control | S | source indicates that its power supply has reached the desired operating condition |
| Get_Source_Cap | control | R | sink requests a Source_Capabilities message |
| Soft_Reset | control | S/R | reset counters to a known state, voltage, and current settings remain unchanged |
| Source_Capabilities | data | S | source exposes power capabilities with PDOs |
| Request | data | R | sink response to Source_Capabilities by selecting one advertised PDO |

[1] TEA19031 (source) perspective

DC-biased Biphase Mark Code (BMC) is used for signaling the information from transmitter to receiver. BMC is self-clocked. It has at least one polarity change per bit cycle.

- 1 = polarity change at half the bit cycle
- 0 = polarity change to the next bit cycle

A packet starts by driving the active CC line to 0. To ensure that the receiver clocks the last bit before releasing the CC line to return to the DC bias level again, a packet ends with a trailing edge. The consumer pull-down resistor $R_d$ sets the DC bias level. It includes any ground offset due to current flowing through the cable.

## 4.2 Power data object contract negotiation

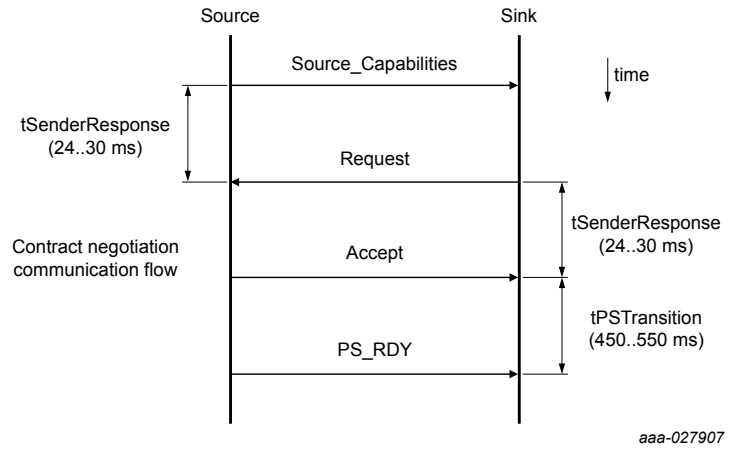



**Figure 4. Contract negotiation communication flow**

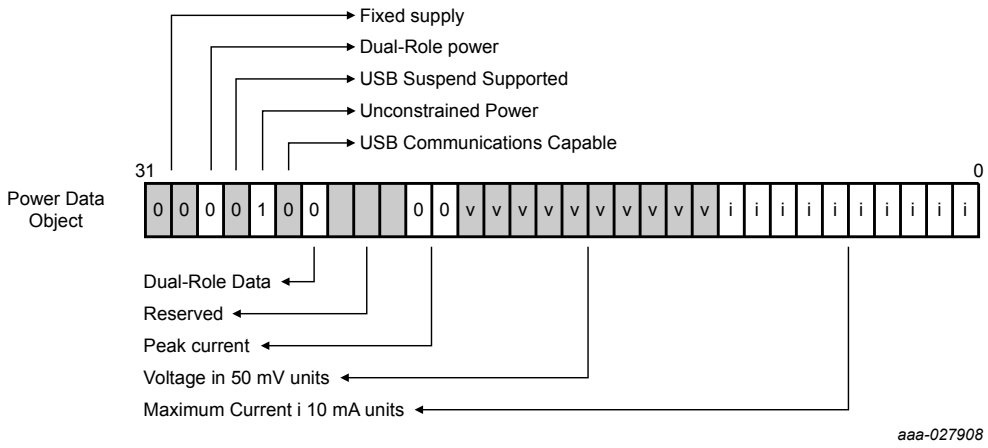



**Figure 5. Power data object structure**

After establishing a valid connection, USB-PD communication can commence. Figure 4 (a) shows the (explicit) contract negotiation communication flow. The source initiates the negotiations by advertising a Source_Capabilities message. This message starts with a message header followed by five distinct and TEA19031-variant dependent PDOs (see Table 2). Each PDO contains generic information combined with the supported voltage and a maximum current level. Next, the sink selects one of the advertised PDOs and returns a Request message to the source. After validation of the Request message, the source sends an Accept message to the sink. The power control settings are changed in alignment with the request. When $V_{bus}$ has stabilized to the newly requested level, the source sends a PS_RDY message to the sink. The contract has been established.

## 4.3 Hard reset

Hard reset is a USB-PD-specific ordered set of bytes recognized by the TEA19031. When detected, the result is that load switch $Q_L$ is opened. To bring the converter output voltage ($V_{CC}$) to vSafe5V, the internal current sink connected to VCC is turned on. The internal switch connected to DISCH and external resistor $R_{DISCH}$ discharges the bus voltage ($V_{bus}$) to vSafe0V for a maximum of 100 ms. Additionally, all internal counters are reset to a known state. To ensure that a new USB-PD communication sequence can start, the connection between producer and consumer remains intact. There is no limit to the number of hard reset attempts.

### 4.3.1 Converter control

In the power converter application (see Figure 1), the TEA19031 applies Constant-Current Constant-Voltage (CCCV) control. Table 2 shows the detailed characteristics. These characteristics depend on the selected variant.

Internally, the voltage and the current reference levels are changed according to the selected PDO. To achieve the desired output voltage and current levels, some external component values have to match certain criteria. For the appropriate output voltage level, the external resistors $R_{V1}$ and $R_{V2}$ must be selected (see Equation 1).

$$K_{Vdiv} = \frac{R_{V2}}{R_{V1} + R_{V2}} \quad (1)$$

Where:

- $K_{Vdiv}$ is the voltage divider ratio (see Table 2)

Recommended values for the compensation network are

- $R_{V1}$ = 160 kΩ to 180 kΩ
- $R_{FBV}$ = 1 kΩ
- $C_{FBV}$ = 3.3 nF

To achieve the best voltage regulation, resistor $R_{V1}$ must be connected as close as possible to the drain of load switch $Q_L$. Any track resistance between the drain and resistor $R_{V1}$ results in a voltage offset. For the same reason, resistor $R_{V2}$ must be connected as close as possible to pin GND of the TEA19031. Figure 6 shows the proper connections for voltage sensing.

# 5 Current sensing and cable compensation

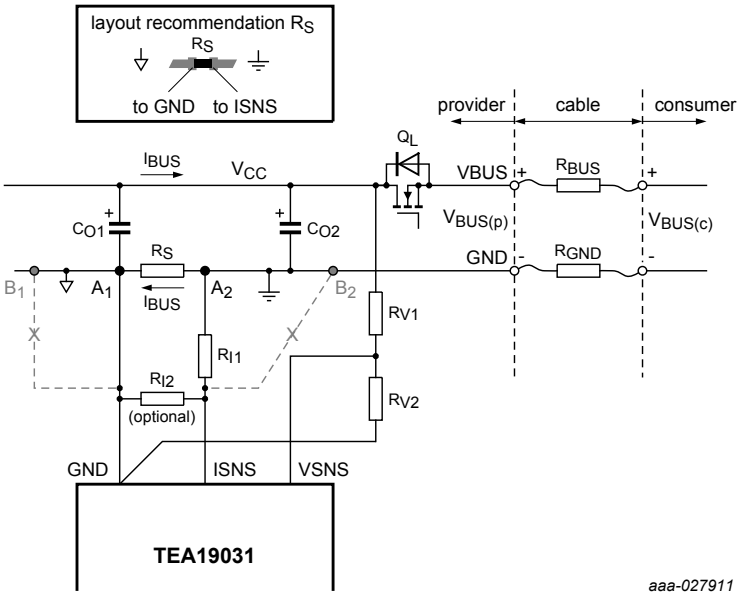



**Figure 6. Voltage sensing and sense resistor tuning with layout connection**

Output current $I_{bus}$ is measured by sensing the voltage drop over sense resistor $R_S$. The required sense resistor value is variant-specific. It can be found in Table 2. For the best sensing, it is important to ensure that the TEA19031 sensing PCB tracks are connected close to the terminals of sense resistor $R_S$. In Figure 6, the A connections are positioned properly. However, the 2 B-connections are positioned poorly. Any voltage drop over the track resistance between the B junctions and the sense resistor terminals introduces measurement errors. The inset shows the recommended layout structure.

An additional resistive divider can be built by adding optional resistor $R_{I2}$. In combination with resistor $R_{I1}$, this divider can be used for adjusting the current measurement.

Recommended values for the compensation network are:

- $R_{I1}$ = 330 Ω
- $R_{FBI}$ = 5 kΩ (not mounted when OCP protection applies)
- $C_{FBI}$ = 100 nF (not mounted when OCP protection applies)

The parasitic resistance of the USB Type-C cable can cause a substantial voltage drop at high currents between the output of the provider and input of the consumer. The variant-dependent cable compensation implemented in the TEA19031 (partly) compensates this voltage drop and the voltage drop over the channel resistance of $Q_L$ and sense resistor $R_S$.

$$V_{bus(c)} = V_{bus(p)} - \left(R_{bus} + R_{GND}\right) \cdot I_{bus} \quad (2)$$
$$= V_{CC} - \left(R_S + R_{QL} + R_{bus} + R_{GND}\right) \cdot I_{bus}$$
$$= V_{PDOx} + K_{comp} \cdot I_{bus} - \left(R_S + R_{QL} + R_{bus} + R_{GND}\right) \cdot I_{bus}$$

Example:

Operating PDO4 of variant AF at a current of 2 A assuming $R_{bus}$ and $R_{GND}$ including:

- Contact resistance of the connector = 55 mΩ
- Channel resistance of $Q_L$ = 2.4 mΩ
- Sense resistor $R_S$ = 10 mΩ

The result is a $V_{bus}$ at the consumer input (see Equation 3).

$$V_{bus(c)} = 15\ V + 67\frac{mV}{A} \cdot 2\ A - \left(10\ m\Omega + 2.4\ m\Omega + 55\ m\Omega + 55\ m\Omega\right) \cdot 2\ A = 14.89\ mV \quad (3)$$

The result would be 14.76 V without cable compensation.

# 6 CCCV operation

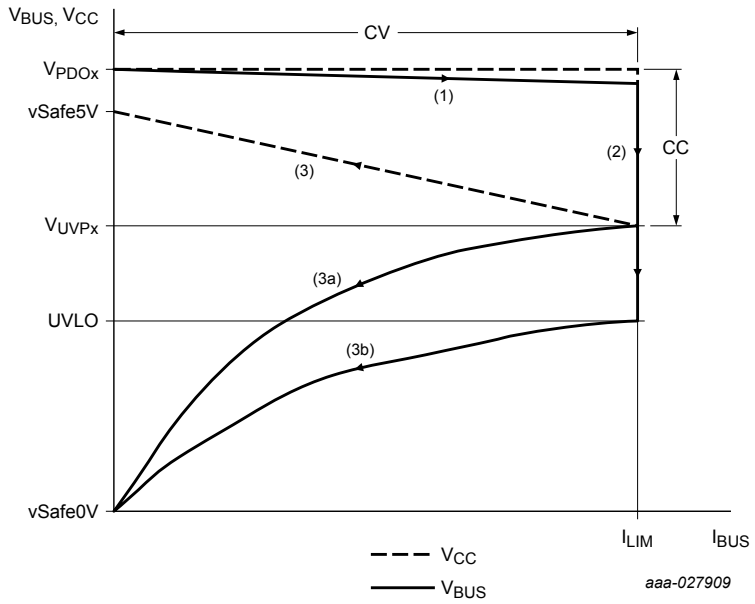



**Figure 7. Constant Current Constant Voltage (CCCV) operation**

Constant Current Constant Voltage (CCCV) operation refers to a control methodology with a behavior shown in Figure 7. In region (1), the output voltage ($V_{CC}$) is regulated to the selected PDO constant voltage level as long as current $I_{BUS}$ drawn by the consumer remains below the selected maximum PDO current ($I_{LIM}$). Depending on the current level, the bus voltage ($V_{bus}$) is slightly lower because of the voltage drop over the internal channel resistance of load switch $Q_L$ and sense resistor $R_S$. If set to the Constant Current (CC) mode (see Section 8.8), the current is limited to the maximum current when reaching this level. The converter operates under the constant current regime (2). The actual converter behavior now depends on the characteristics of the consumer. If the consumer behaves like a resistor or a voltage sink, the TEA19031 can regulate $V_{CC}$ - and so also $V_{bus}$ - to a lower voltage level. The lower voltage level balances the current supplied by the source ($I_{LIM}$) and the current requested by the consumer. This balance can be established as long as the voltage exceeds the UnderVoltage Protection (UVP) or UnderVoltage LockOut (UVLO) level. When the consumer behaves like a current sink, this balance cannot be established. The output voltage immediately drops to the UVP or UVLO level. In either case, load switch $Q_L$ opens and $V_{CC}$ returns to vSafe5V (3). At the same time, $V_{bus}$ returns to vSafe0V (3a or 3b). If the $I_{bus}$ current drops to below $I_{LIM}$ before reaching UVP or UVLO, the bus voltage returns to the constant voltage regime ($V_{PDOx}$).

# 7 Parabolic slope control

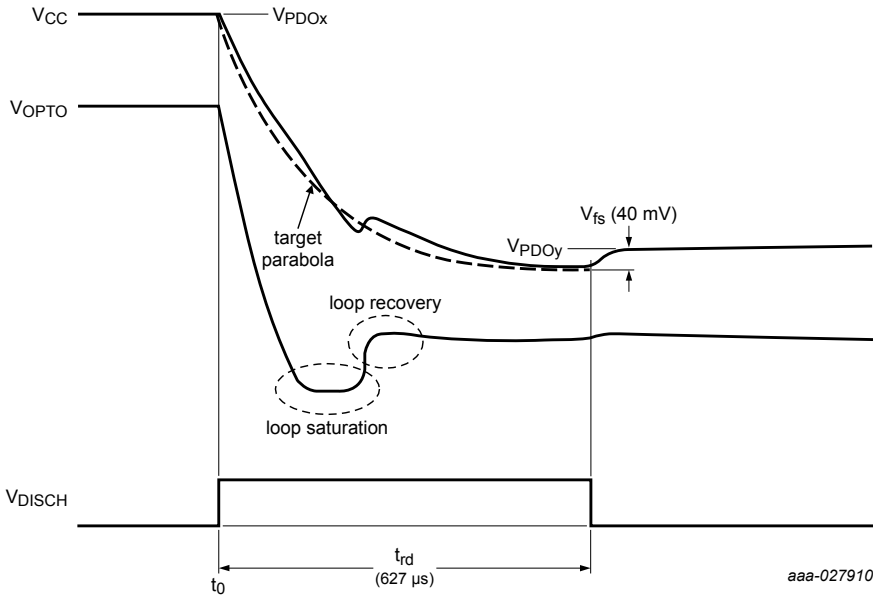



**Figure 8. Parabolic ramp-down slope control**

Changes in PDO selection during USB-PD communication result in new $V_{bus}$ voltage ($V_{PDOx}$) and maximum current ($I_{PDOx}$) settings. The changes in current settings, both up and down, are done in a single step. When the newly requested output voltage level is higher than the currently active one, the TEA19031 changes the set point in a single step. When the primary side controller delivers more power to the output of the converter, the result is a ramp-up. When the new output voltage level is lower than the currently active setting, additional precautions must be taken to ensure that the control loop remains unsaturated at the end of the ramp-down transition period ($t_{rd}$). If not, any load step directly after the transition can result in an undesired output voltage transient.

To provide the best voltage ramp-down, an advanced parabolic ramp-down algorithm (patent pending) is implemented. The internal discharge switch connected to the DISCH pin is activated. When voltage transition is initiated at $t_0$, it provides a discharge current sink. The TEA19031 calculates a parabolic target reference level and regulates the $V_{CC}$ output voltage accordingly. The initial steep slope of the parabola causes the internal voltage error amplifier to saturate. This effect is unavoidable. It results from the external voltage compensation network consisting of $R_{FBV}$, $C_{FBV}$, and $R_{GN}$. The velocity of change in the target parabola slows down progressively and the error amplifier can "catch-up" with the reference level. The best performance is achieved by applying a small 40 mV reference step-up just before reaching the target.

In the ramp-up and ramp-down situations, the TEA19031 sends a PS_RDY signal to the sink immediately after reaching respectively 95 % and 105 % of the new setting. It includes any cable compensation offset described in Section 5.

# 8 Protections

## 8.1 Protections overview

Table 5 gives an overview of all available protections. All protections, except UVP, are implemented in hardware, so they are functional under all conditions, even when the internal TEA19031 digital signal processor stalls. When triggered, a protection causes a safe restart with a 1 s repetition interval or a latched response.

**Table 5. Overview protections**

| Protection | Description | Design | Level | Delay | Response |
|---|---|---|---|---|---|
| UVLO | undervoltage lockout | hardware | $V_{UVLO(f)}$ (2.8 V<br>$V_{UVLO(r)}$ (3.0 V) | 0 µs[2] | restart |
| OSP | output short protection | hardware | see UVLO or UVP | - | restart |
| OVP | overvoltage protection | hardware | $V_{ovp}$[3][4] | 30 µs | restart |
| UVP | undervoltage protection | software | 60 %[3][4] | | |
| OCP | overcurrent protection | hardware | $I_{LIM}$[5] | 25 ms | restart |
| OSUP | open supply protection | hardware | - | 0 µs[2] | -[6] |
| CC-OVP | cc-lines overvoltage protection[7] | hardware | 4.5 V | 10 µs | restart |
| OTP | overtemperature protection (internal) | hardware | 115 °C | 0 µs[2] | latched |
| NTC-OTP | overtemperature protection (external) | hardware | 90 °C | 0 µs[2] | restart |

[1] See Table 2 for variant-specific settings.
[2] Immediate response excluding any internal circuit delay.
[3] As a percentage of the $V_{PDOx}$ level.
[4] PDO0 and PDO1 have no UVP.
[5] As a percentage of the $I_{PDOx}$ level.
[6] $V_{CC}$ supply voltage lost, load switched is opened.
[7] The active CC attach detection line only.

## 8.2 Safe-restart response

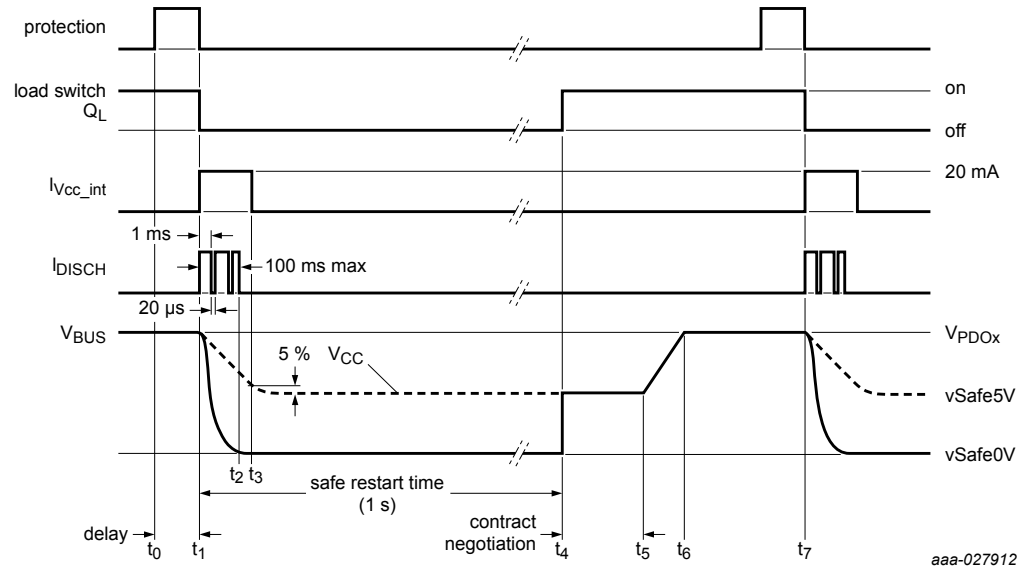



**Figure 9. Safe restart protection timing diagram**

Figure 9 shows the safe-restart-mode timing diagram. In safe restart mode, load switch $Q_L$ is turned off ($t_1$) after the protection is triggered ($t_0$) and expiration of the protection-dependent delay time. The attached consumer is decoupled from the producer. Supported by an internal current sink of typically 20 mA, the TEA19031 error-amplifiers regulate the converter output voltage ($V_{CC}$) to its vSafe5V level (5 V typical; see the USB-specification (Ref. 1)). The internal current sink remains active until $V_{CC}$ has dropped to below a voltage level of 5 % above the typical vSafe5V level ($t_3$). The internal switch connected to DISCH is closed. It draws a discharge current from $V_{bus}$ through resistor $R_{DISCH}$. The voltage on this node drops rapidly. With an interval of 1 ms, the internal DISCH switch opens for a $V_{bus}$ measurement period of 20 µs. During this period, the TEA19031 samples the bus voltage. Resistor $R_{DISCH}$ and any capacitance connected to the DISCH pin must be designed such that the DISCH pin voltage returns to the $V_{bus}$ level within this measurement period. As long as $V_{bus}$ remains above 0.7 V (maximum 100 ms), the DISCH function remains operational. This mechanism ensures that $V_{bus}$ drops to vSafe0V ($t_2$) within the appropriate time in alignment with the USB-PD standard.

When triggered, the safe restart timer is started. All circuits are reinitialized. When the 1 s safe-restart time has elapsed ($t_4$), a new start-up sequence commences. The load switch is closed and the USB-PD contract is negotiated ($t_5$). After reaching the requested $V_{CC}$ level ($t_6$), the converter resumes normal operation. If the fault condition persists, the TEA19031 enters a new protection cycle ($t_7$).

## 8.3 Latched response

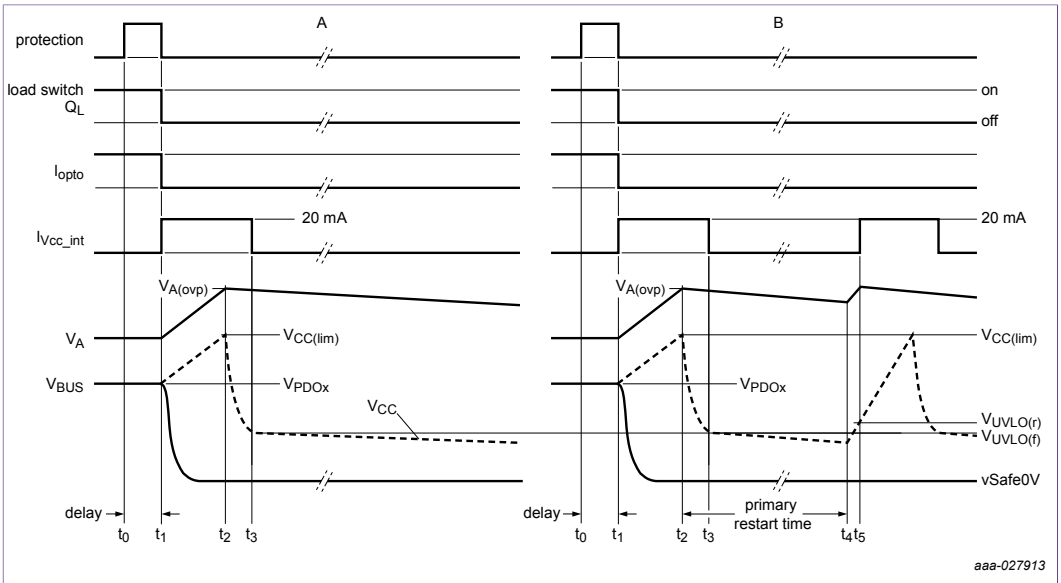



**Figure 10. Latched protection timing diagram, primary side latched (A), and primary side induced safe restart (B)**

When the actual system is programmed to latched response, its behavior depends on the primary-side controller behavior. Depending on the settings of the primary side controller (Ref. 4), the response is a converter latch (see Figure 10 - A) or yet another primary-side induced save restart (see Figure 10 - B. After triggering of the protection ($t_0$) and expiration of the protection-dependent delay time, load switch $Q_L$ is turned off ($t_1$). The attached consumer is decoupled from the producer. An internal current sink current of 20 mA (typical) connected to $V_{CC}$ is activated. At the same time, the optocoupler current is reduced to virtually zero. This zero optocoupler current is an indication for the primary-side controller to increase the amount of power delivered to the output of the converter so $V_{CC}$ increases. The reflected primary-side controller supply voltage ($V_A$) also increase in alignment with the turns ratio of the transformer. the result is that when the controller supply voltage reaches $V_{A(ovp)}$, the overvoltage protection is triggered on the primary side ($t_2$). The primary-side controller stops operation of the converter. $V_{CC}$ gradually drops to below the falling UVLO level ($V_{UVLO(f)}$) because of the TEA19031 internal current sink. If there is a primary-side latched protection, the converter remains off. When a primary-side induced safe restart is programmed, the primary-side controller initiates a new start-up cycle ($t_4$). As soon as $V_{CC}$ crosses the rising UVLO level $V_{UVLO(r)}$, the internal current sink is turned on again ($t_5$). The load switch remains off and the optocoupler current remains zero. This sequence repeats itself continuously. The maximum $V_{CC}$ voltage can be calculated with Equation 4. Load switch $Q_L$ must be able to withstand this $V_{CC(lim)}$ voltage.

$$V_{CC(lim)} = \frac{n_s}{n_a} \cdot V_{A(ovp)} \quad (4)$$

Where:

- If a protection latches the converter $V_{CC(lim)}$ is the maximum VCC voltage
- $n_s$ is the number of secondary turns on the transformer
- $n_a$ is the number of primary-side controller supply turns on the transformer
- $V_{A(ovp)}$ is the OVP level of the primary-side controller supply voltage (Ref. 4)

## 8.4 UnderVoltage LockOut (UVLO)

In order to assure well-defined internal TEA19031 functionality and proper driving of load switch $Q_L$, all circuits are released only when $V_{CC}$ rises above $V_{UVLO(r)}$. A protection is triggered when $V_{CC}$ drops below $V_{UVLO(f)}$ again. This situation can occur when the connected consumer draws too much current $I_{BUS}$ while operating in Constant Current (CC) mode (see Section 8.8). It can also occur when any other protection has triggered a latched response. The protection is implemented in hardware with fixed levels.

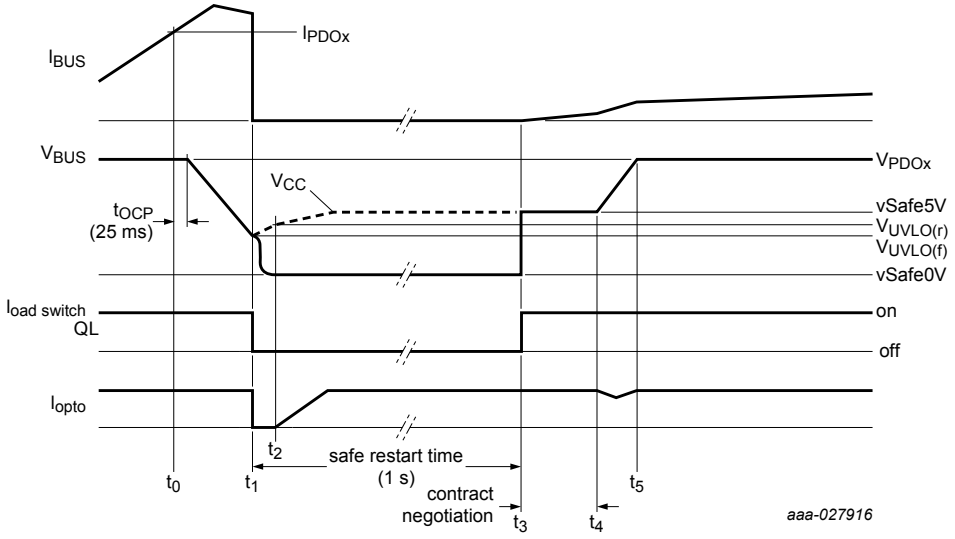



**Figure 11. Overload in CC mode causing a safe restart UVLO**

Figure 11 shows an overload on $V_{bus}$ in CC mode, which causes $V_{CC}$ to drop out of regulation. A safe restart UVLO protection is triggered. The optocoupler current remains constant because of the constant current control action of the TEA19031. $V_{CC}$ continues to drop. When the voltage drops to below $V_{UVLO(f)}$, the load switch is opened immediately. It disconnects the consumer from the converter ($t_1$). With the load disconnected and the primary side delivering full power, $V_{CC}$ increases again. When $V_{CC}$ exceeds $V_{UVLO(r)}$ ($t_2$), the TEA19031 regulates the output voltage to vSafe5V. After the 1 s safe restart time has elapsed, the load switch closes again ($t_3$). The controller awaits new contract negotiations. These negotiations must be concluded ($t_4$) before regulation can continue toward the final $V_{PDOx}$ level ($t_5$). If the overload condition still persists, the converter enters a new safe-restart cycle.

## 8.5 Output Short Protection (OSP)

Short circuit is a special case of overload. UVLO and UVP protect against short circuits. A short circuit can occur during operation or prior to the converter start-up. In both cases, when the load switch is closed, the current drawn from $V_{CC}$ increases rapidly. To endure this condition, the selection of the load switch must handle worst case energy dissipation (see Equation 5) until the switch opens after the UVLO protection is triggered. The PCB tracks must sustain the corresponding high current determined by the total impedance of the load switch channel resistance, sense resistor $R_S$, and any PCB track resistance. Careful layout must ensure that, when the load switch is turned off while carrying this high current, load switch drain does not suffer from an inductive voltage spike. Similarly, a negative voltage may be induced at the source of the load switch. To avoid inductive turn-on of the load switch, which could be detrimental for the converter, this voltage must be restrained.

$$E_{QL(max)} = \frac{1}{2} \cdot C_O \cdot \left(V_{CC(0)}^2 - V_{UVLO(f)}^2\right) \quad (5)$$

Where:

- $E_{QL(max)}$ is the maximum energy to be dissipated in the load switch
- $C_O$ is the total output capacitance connected to $V_{CC}$
- $V_{CC(0)}$ is the $V_{CC}$ voltage when the short circuit happens and equals $V_{PDOx}$

Figure 12 shows a measured waveform of a short-circuit occurrence. The maximum current increases rapidly and a sharp voltage spike can be observed on $V_{CC}$. The source of $Q_L$ ($V_{bus}$) briefly dips to a negative level. However, it does not drop deep enough to turn on the switch again, which is undesired.

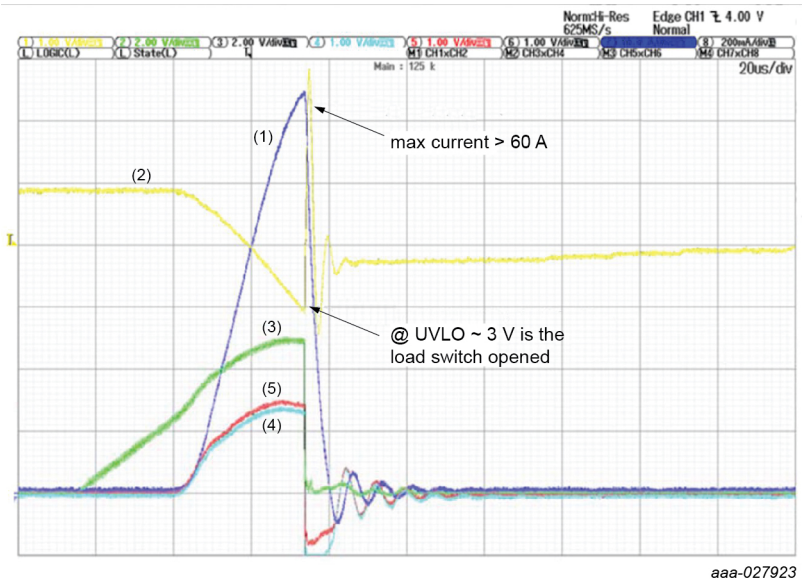



**Figure 12. Output short behavior at start-up**

The TEA19031 pin voltages must never exceed the absolute maximum ratings as specified in the TEA19031 data sheet (Ref. 3).

## 8.6 OverVoltage Protection (OVP)

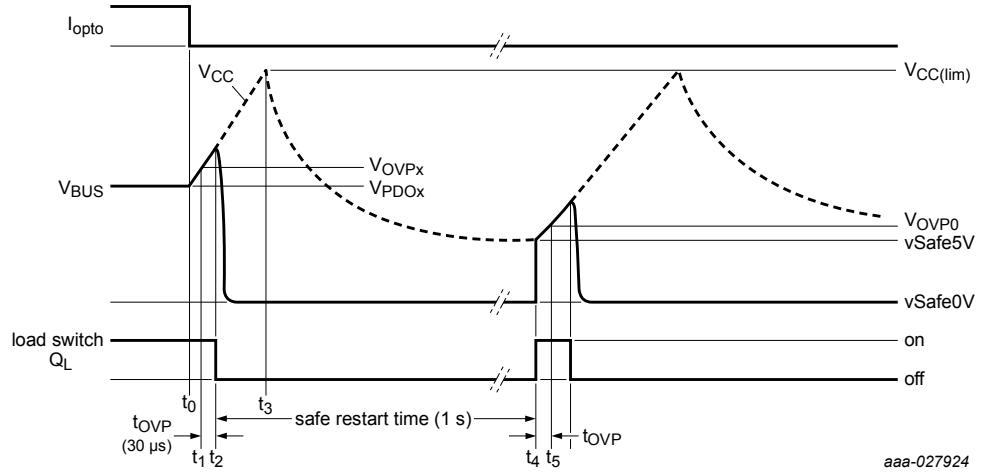



**Figure 13. Optocoupler fault causing a safe-restart OVP**

If the optocoupler feedback path to the primary side controller gets disrupted, the OVP, measured on pin VCC, prevents further damage to the consumer by opening load switch $Q_L$. Figure 13 shows an example of the OVP sequence with safe-restart response.
At $t_0$, the optocoupler unexpectedly seizes to conduct current due to a fault condition. Although $V_{CC}$ and $V_{bus}$ are programmed at $V_{PDOx}$, both voltages start to increase. When $V_{CC}$ reaches the corresponding protection trip level at $V_{OVPx}$ ($t_1$) and after a 30 µs blanking time ($t_{OVP}$; $t_2$), the load switch opens. The bus voltage rapidly drops to vSafe0V. However, $V_{CC}$ increases to $V_{CC(lim)}$ ($t_3$), which depends on the primary OVP voltage (see Equation 4). When the 1 s safe-restart timer has elapsed, a new safe-restart attempt is made. Before any USB-PD communication has taken place, the control and protection levels are reset to $V_{PDO0}$, which is equivalent to vSafe5V. It means that the new OVP trip level is at $V_{OVP}$. It is related to vSafe5V. If the optocoupler fault condition persists, a new safe restart cycle starts at $t_5$.

## 8.7 UnderVoltage Protection (UVP)

When the output voltage drops too much during an overload condition, an additional UVP protection level, measured on pin VCC, can be triggered. For all PDOs except PDO0 and PDO1, this UVP level is at 60 % of the programmed $V_{PDOx}$ level. When $V_{CC}$ reaches UVP, a safe-restart response follows. PDO0 and PDO1 have no UVP. They rely on the UVLO protection.

## 8.8 OverCurrent Protection (OCP)

When the consumer draws a current that exceeds the limiting current level ($I_{lim}$), the TEA19031 allows the power converter to operate in CC mode or to respond with an OCP. The limiting current level is variant-dependent (see Table 2). For details on CC-mode operation and protection, see Section 6 and Section 8.4. Figure 14 shows the timing sequence when OCP is active.

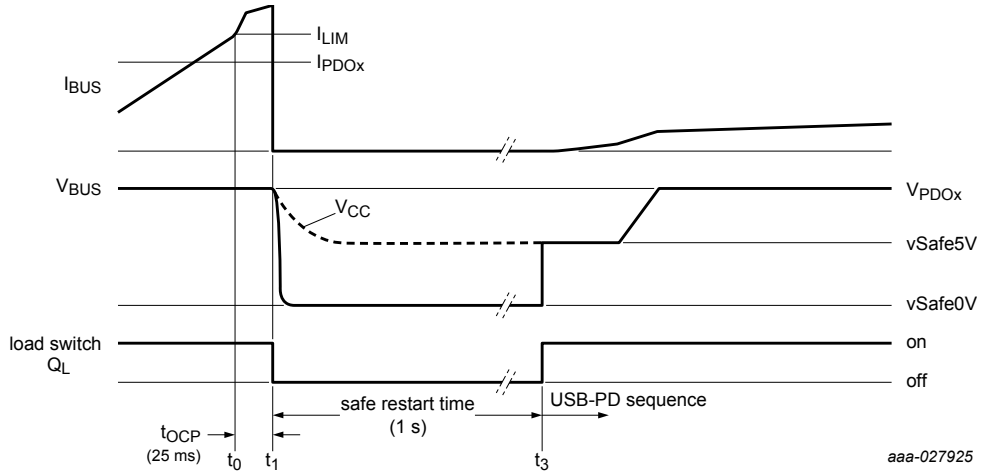



**Figure 14. Overload causing a safe-restart OCP**

When a current exceeding the limiting current ($I_{lim}$) triggers OCP, the protection sequence is initiated ($t_0$). The protection only becomes effective after $t_{OCP}$ (25 ms) at $t_1$. Load switch $Q_L$ is opened. $V_{CC}$ is regulated to the vSafe5V level. $V_{BUS}$ drops to the vSafe0V level. OCP results in a safe restart. So, after the safe-restart timer has elapsed, a new USB-PD initiation cycle commences ($t_3$).

## 8.9 Open-SUpply Protection (OSUP)

To ensure unconditional protection of the consumer, the TEA19031 uses the available voltage on the OPTO pin to turn off load switch $Q_L$ immediately if there is an unexpected supply voltage ($V_{CC}$) failure. When $V_{CC}$ is restored, the controller resumes normal operation.

## 8.10 Internal OverTemperature Protection (OTP)

If the internal TEA19031 temperature exceeds 115 °C, a latched protection is triggered (see Section 8.3).

## 8.11 NTC thermal protection (external OTP)

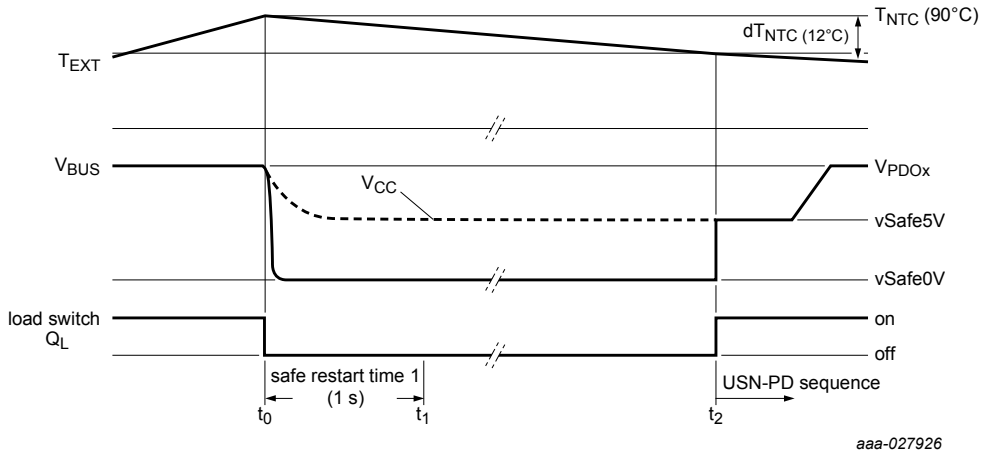



**Figure 15. External OTP via NTC resistor**

In addition to the internal temperature protection, an external temperature protection is available via the NTC pin. A 47 kΩ NTC resistor with a β-constant of 4050 (e.g. EPCOS B57321V2473J060 or Murata NCU18WB473F60RB) must be connected to the NTC pin of the TEA19031. When the external temperature exceeds the NTC-OTP trip level of 90 °C ($t_0$), a safe restart is initiated. When the safe restart timer has elapsed ($t_1$) and while the external temperature remains above 78 °C, the TEA19031 suspends converter start-up. When the external temperature drops to below this lower temperature boundary ($t_2$), the TEA19031 releases the converter for a new USB-PD communication sequence. At this lower temperature level, the NTC value has decreased to about 4 kΩ.

## 8.12 Communication interface protection

Immediately after attach detection, the active CC detection line is overvoltage protected at 4.5 V. When the protection is triggered, a safe-restart cycle is initiated. The second CC line is not protected.

# 9 Application diagram

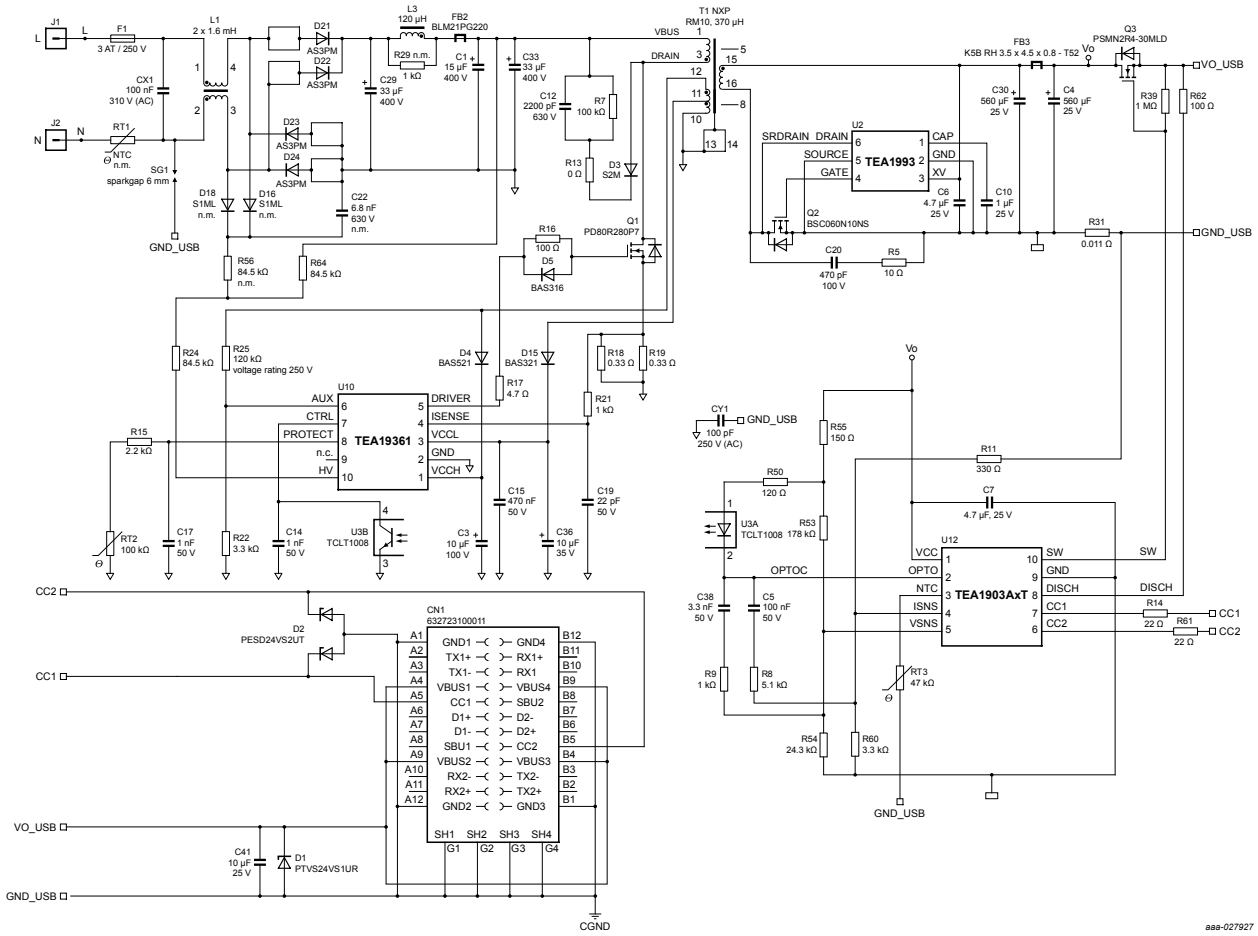
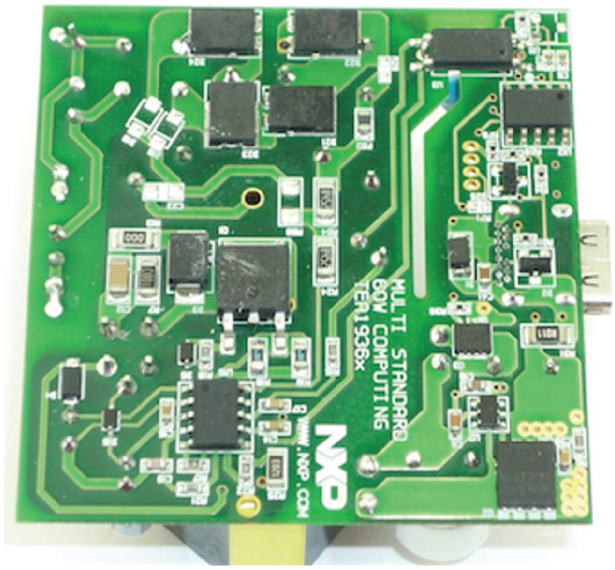



**Figure 16. Circuit diagram of multistandard 60 W computing charging demo board with TEA19031, TEA19361, and TEA1993**

## 10 Printed-Circuit Board (PCB) demo

aaa-027928

a. Top view




aaa-027929

b. bottom view

**Figure 17. Demo PCB of a multistandard 60 W computing charging demo board (50 mm × 50 mm × 25 mm) with TEA19031, TEA19361 and TEA1993**

# 11 Abbreviations

| Acronym | Description |
|---|---|
| BMC | Biphase Mark Code |
| CCM | Constant Current Mode |
| CCCV | Constant-Current Constant-Voltage |
| CC-OVP | CC-lines OverVoltage Protection |
| CRC | Cyclic Redundancy Check |
| DFP | Down-stream Facing Port[1] |
| EOP | End Of Packet |
| NTC | Negative Temperature Coefficient |
| OCP | OverCurrent Protection |
| OSP | Output Short Protection |
| OSUP | Open-SUpply Protection |
| OTP | OverTemperature Protection |
| OVP | OverVoltage Protection |
| PDO | Power Data Object |
| SMPS | Switched-Mode Power Supply |
| SOP | Start Of Packet |
| UFP | Upstream Facing Port[2] |
| USB-PD | USB Power Delivery (Ref. 1) |
| UVLO | UnderVoltage LockOut |
| UVP | UnderVoltage Protection |
| vSafe0V | Safe operating voltage at 0 V[3] |
| vSafe5V | Safe operating voltage at 5 V[4] |

[1] DFP indicates the position of the port in the USB topology, typically corresponding to a USB host root port or hub downstream port as defined in USB Type-C (Ref. 2).
[2] UFP indicates the position of the port in the USB topology, typically a port on a device as defined in USB Type-C (Ref. 2).
[3] 0 V ≤ vSafe0V ≤ 0.8 V.
[4] 4.75 V ≤ vSafe5V ≤ 5.5 V.

# 12 References


1 **USB Power Delivery Specification** Rev. 2.0 Version 1.3; January 12, 2017

2 **USB Type-C Cable and Connector Specification** Revision 1.2; March 25, 2016 and ECNs

3 **TEA19031 data sheet** USB-PD controller for SMPS; 2017, NXP Semiconductors

4 **TEA193x data sheets** GreenChip primary-side control IC; 2016/2017, NXP Semiconductors

5 **TEA199x data sheets** GreenChip synchronous rectifier controller; 2016/2017, NXP Semiconductors

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